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EFFICIENT DESIGN OF PULSE TRIGGERED FLIP-FLOP USING PASS TRANSISTOR LOGIC

Mr. S.Belwin Joel M.E[1]

Assistant professor, Dept. of ECE, James College of Engineering and Technology, Nagercoil, Tamilnadu. [1]

belwinjoel@gmail.com

Abstract: Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption. The performance of the flip-flop is an important element to determine the efficiency of the whole synchronous circuit. In an attempt to reduce power consumption in flip-flops a novel method is presented. An implicit type pulse triggered flip-flop is designed using conditional pulse enhancement scheme. The pulse generation logic use two input AND gate at its discharge path which reduces the circuit complexity and hence the overall area is reduced. Pulses for discharging are generated only when there is a need, so this reduces circuit activity and also provides faster discharge operation. So the extra power consumed can also be eliminated. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors. Transistor sizes are also reduced to provide area and power saving. Power consumption is reduced compared to conventional methods.

Keywords: Flip-flop, AND Gate, PMOS transistor, Power save