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RADIX-4 AND RADIX-8 MULTIPLIER USING VERILOG HDL

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Abstract: Now-a-days the power consumption is the major problem for the electronic devices. So, to design the integrated circuit , to perform the low power , less occupation area and high speed simultaneously. This paper presents to design the high performance parallel radix-4/radix-8 multiplier by using booth algorithm. The structure for design is m x n multiplication .where, m and n reach up to 8 bits. Carry Look ahead Adder is used as the final order to enhance the speed of operation. The design process is done in Verilog HDL and simulation by using model sim simulator (XSE 8.1).

Keywords: Carry look ahead adder, Verilog HDL, Multiplier.