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Implementation of Seven Stage Diode Clamped Multi Stage Inverter

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Abstract - Three phase Seven level Diode Clamped Multilevel Inverter (DCMLI) to simulate various modulating techniques for induction motor load. PWM consists of Phase Disposition strategy, Phase Opposition Disposition strategy and Alternate Phase Opposition Disposition strategy. The Total Harmonic Distortion (THD), VRMS (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK.

I.INTRODUCTION

The basic perception of a multilevel Inverter to achieve higher power is to use a series of power semiconductor switches with several lowerVoltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as theMultiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected [1-4].

II. MULTI LEVEL INVERTER

The Multi-Level inverter has drawn a tremendous interest in power industry. They present an important in reactive power compensation. It may be either to produce a high power, high voltage inverter with Multi level inverter.

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Increasing the number of voltage level without requiring higher rating of individual levels can increase the power rating [5].

The basic concept of a multilevel Inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources [6].

The commutation of the power switches aggregate these multiple dc sources to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only on the rating of the dc voltage sources to which they are connected. Consider a three phase inverter system with DC input voltage. Series connected capacitors constitute the energy tank of the inverter [5-6]. Each capacitor has the same voltage which is given by,

Em = (Voltage input Vdc)/ (m-1)

Where m denotes the number of levels, the term m denotes the number of nodes to which the inverter can be accessible

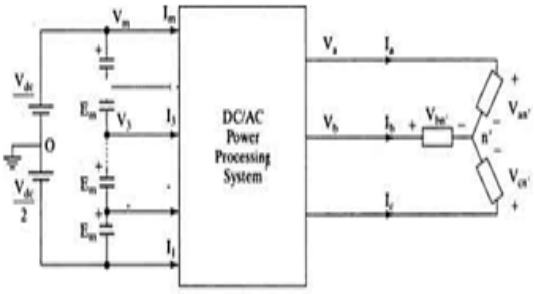

Fig 1: Multi Level Inverter with Series Connected Capacitors

III. DIODE CLAMPED MULTI LEVEL INVERTER

Experimental results for four-, five-, and six-level diode-clamped converters for uses such as static var compensation, variable speed motor drives, and high voltage system interconnections .A three-phase six level diode-clamped inverter is shown in Fig. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is *V*dc, and the voltage stress across each switching device is limited to *V*dc through the clamping diodes. Table lists the output voltage levels

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possible for one phase of the inverter with the negative dc rail voltage $V0$ as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require the other complementary switch to be turned off.

The complementary switch pairs for phase leg *a* are (Sa1, Sa_1), (Sa2, Sa_2), (Sa3, Sa_3), (Sa4, Sa_4), and (Sa5, Sa_5). Table also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg is always adjacent and in series.

For a six-level inverter, a set of five switches should be on at any given time. The line voltage Vab consists of a phase-leg "a" voltage and a phase-leg "b" voltage. The resulting line voltage is a 11-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a $(2m - 1)$-level output line voltage. Although each active switching device is required to block only a voltage level of Vdc, the clamping diodes require different ratings for reverse voltage blocking. Using phase *a* of Fig as an example, when all the lower switches Sa_1 through Sa_5 are turned on, D4 must block four voltage levels, or $4V$dc. Similarly, D3 must block $3V$dc, D2 must block $2V$dc, and D1 must block Vdc. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, Dn will require n diodes in series; consequently, the number of diodes required for each phase would be $(m - 1) \times (m - 2)$.Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter.

One application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line .Another application would be a variable speed drive for high-power medium-voltage (2.4–13.8 kV) motors as proposed .Several authors have proposed for the diode-clamped converter that static var compensation is an additional function

IV. IMPROVED DIODE CLAMPED INVERTER

The power rating of the parallel inverter will now be considered. From Fig the apparent power delivered to the

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electrical system by the parallel inverter can be expressed as,

$$S\,\mathrm{PI} = P\mathrm{L}\,(1 - V\mathrm{L}\,V\mathrm{S}) + jQ\mathrm{L}$$

The power transferred for voltage declines to less than 50% of nominal is predominantly real power, the parallel inverter would have to have an extraordinarily high rating if the conditioner were designed to compensate for such large voltage sags, just like the series inverter. From Fig.1, one can see that for voltage sag to 50% of nominal, the parallel inverter has to draw a current IPI equal to that drawn by the rated load IL. However, unlike the series inverter, the dominant factor in determining the power rating of the parallel inverter is the load power factor if the conditioner is designed to compensate for only marginal voltage sags as shown in Fig. If the design of the universal power conditioner is to compensate for voltage sags to less than 50% of nominal voltage, then Eq. (17.31) should be used to determine the current rating of the parallel inverter. If the design of the conditioner is for marginal voltage sags (to 70% of nominal voltage) and the MUPC will be applied to a customer load that has a power factor of less than 0.9, then the following equation is more suited for calculating the current rating of the parallel inverter's active devices

One common design for the parallel inverter in a universal power conditioner is for the inverter to have a current rating equal to that of the rated load current

V.CHARACTERISTICS OF DIODE CLAMPEDMULTI-LEVEL INVERTER

The multilevel inverter performance operation is compared from the phase disposition strategy (PDPWM)

The rules for Phase disposition strategy for a multilevel inverter are

1. The converter is switched to + Vdc/2 when the sine wave is greater than both upper carrier.
2. The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.
3. The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier
4. The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.

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5. The converter is switched to - Vdc/2 when the sine wave is less than both lower carriers.

VI. SIMULATION RESULTS

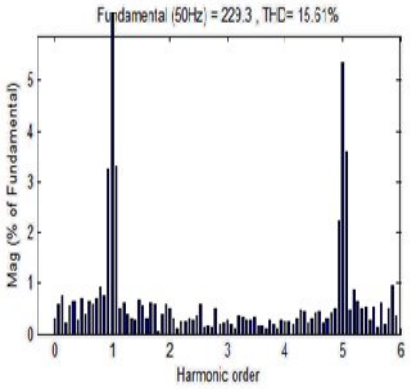

Fig 2: Mag vs Harmonic Order (THD Value)

VII. CONCLUSION

The above work proposes three phase Seven level Diode Clamped Multilevel Inverter (DCMLI) to simulate various modulating techniques for induction motor load. These Pulse Width Modulation (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PSPWM) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. Thus the Total Harmonic Distortion (THD), VRMS (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices.

REFERENCES

1. C.Newton and M.Sumner, " Multi level inverter – A real solution to medium high voltage drives, Inst.Electron, Eng – power Feb 2011
2. T.Maruyuma and M.Kumano, New PWM control for a three level inverter " in proc. Rec. IPEC Feb 2011
3. M.Carpita and S.Teconi, "A novel multi-level inverter PWM technique " , IEEE Trans, Ind Application , Sept/oct 2011
4. J.Chaisson, L.M.Tolbert , K.J, Mckenzie , Z.Du ,"Control of a multi-level inverter using relevant theory,"IEEE Transaction on control systems Technology, Feb 2013
5. J.Wang, Q.We , Y.Li,"Multi level inverter – A survey of topologies , controls and application,"IEEE

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Available online at www.ijartet.com

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Transaction on industrial application, Feb 2014

6. A.Nabae, I.Takahshi and A.Akagi," A new neutral point clamped PWM inverter. ,"IEEE Trans. Ind. Application May 2014