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Design of a Full Adder using PTL and GDI Technique

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Abstract: In this paper an area and power efficient 9T adder design has been presented by hybridizing PTL and GDI techniques. The proposed adder design consists of 5 NMOS and 4 PMOS transistors. A PTL based 5T XOR-XNOR module has been proposed to improve area at 130nm technology. The proposed Hybrid full adder design is based on this area efficient 5T XOR-XNOR module design. Different logic functions can be implemented by only two transistors by using Gate diffusion input (GDI) approach. To improve area and power efficiency a cascade implementation of XOR module has been avoided in the proposed full adder. XOR-XNOR modules outputs act as input to Carry and Sum module which has been implemented by the GDI MUX. GDI approach is suitable for design of high speed, power efficient circuits with improved logic level swing and static power characteristics using a reduced number of transistors as compared to CMOS techniques. Simulations have been performed using tanner tool and Result shows that the proposed adder has an improvement of 62% in power over Existing Parallel Self-timed Adder (PASTA).

Keywords: Recursive adder, CMOS design, Gate Diffusion Input, Pass transistor logic

I. INTRODUCTION

Full adder is a basic building block in the arithmetic unit of digital signal processors and application specific integrated circuits used in various digital electronic devices. In the world of technology the demand of portable devices are increasing day by day. Demand and popularity of these devices depends on the small silicon area, higher speed, longer battery life and reliability. Overall system performance can be affected by enhancing the performance of the full adder circuit used in these systems.

Power and area consumption is a key limitation in many electronic devices such as mobile phone and portable computing systems etc. So far several logic styles have been used to design full adder cell to improve area and power consumption [1]-[4]. Design of full adder by using conventional CMOS design style has been presented. To generate the output transistor level design of CMOS full adder contains total of 14 PMOS and 14 NMOS transistors and two CMOS inverter. All NMOS and PMOS transistors used in this circuit have the same W/L ratio. It is required to adjust the transistor dimensions individually to get optimized time domain performance of the circuit. In [5]-[13] the area and power delay performance of full adder designs by different logic styles have been investigate.

Adders are not only used for arithmetic operation but also necessary to compute virtual physical address in memory fetch operation in all modern computers. Also the adders occupies critical path in key areas of microprocessor, fast adders are prime requirement for the design of fast processing digital system. Many fast adders are available but the design of high speed with low power and less area adders are still challenging. In modern super computers, multiple ALU'S with wide adders and multiple execution core units on the same chip creates thermal hotspots and large temperature gradients. This affects the circuit reliability and increasing the cooling cost of the system. Ideally, adders should have highest performance with least amount of power dissipation and small layout area to minimize unnecessary delays.

With the popularity of portable systems as well as fast growth of power density in integrated circuits, power dissipation becomes main design objectives equal to high performance of the system. For the VLSI designers,

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designing power efficient adders for digital system has become main goal. Generally Ripple Carry Adders are used among all types of adders because of its compact design but it is the slowest adder. CMOS is the most common circuit design style/technique for designing any digital circuit but it dissipates most of the power during transistor switching activity. Here we propose a power efficient Full adder based on Pass Transistor Logic and Gate Diffusion Input circuit design style. Using this design style, power dissipation in adder is reduced by 60% less as compare to PASTA design style. Also it reduces area and propagation delay.

The remainder of this brief is organized as follows. Section II provides architecture and theory of self-timed adder. Section III presents the proposed adder schematic. Sections IV gives the details of circuit design simulation using Tanner tool and then the comparative result with conclusion is explained in section V.

II. DESIGN OF PASTA

In this section, the architecture and theory behind PASTA is presented. The adder first accepts two input operands to perform half additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

A. Architecture of PASTA

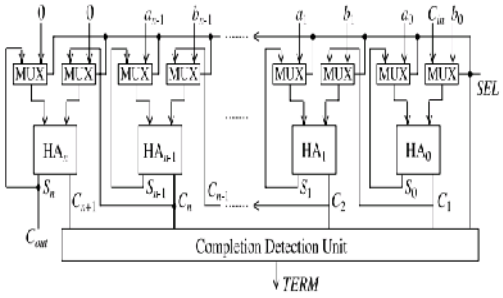

Fig 1: General Block Diagram of PASTA

The general architecture of the adder is shown in Fig.1.The selection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback paths for subsequent iterations using SEL = 1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values [14].

B .State Diagrams

In Fig. 2, two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (C_{i+1}, S_i) pair where C_{i+1}, S_i represents carry out and sum values, respectively from the *i*th bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state *(*11*)* cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (*Ci*) are allowed as many times as needed to complete the recursion. From the definition of fundamental mode circuits, the present design cannot be considered as a fundamental mode circuit as the input– outputs will go through several transitions before producing the final output. It is not a Muller circuit working outside the Fundamental mode either as internally; several transitions will take place, as shown in the state diagram. This is analogous to cyclic sequential circuits where gate delays are utilized to separate individual states.

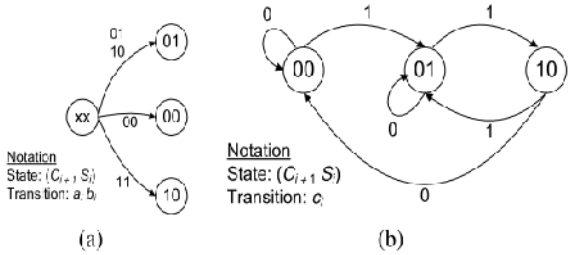

Fig 2: State Diagrams for PASTA (a) Initial Phase (b) Iterative Phase

C. Recursive method for Binary Addition

Let S^i_j, C^j_{i+1} denote the sum and carry, respectively, for i^{th} bit at the j^{th} iteration. The initial condition (j = 0) for addition is formulated as follows:

$$S_i = a_i \oplus b_i \qquad (1)$$

$$C_{i+1} = a_i b_i \qquad (2)$$

The j^{th} iteration for the recursive addition is formulated by

$$S_i^{\,j} = S_i^{\,j-1} \oplus C_{i-1}^{\,j-1} \qquad (3)$$

$$C_i^{\,j} = S_i^{\,j-1} C_{i-1}^{\,j-1} \qquad (4)$$

The recursion is terminated at k^{th} iteration when the following condition is met

$$C_n^{\,k} C_{n-1}^{\,k} \Lambda C_0^{\,k} = 0 \qquad (5)$$

Now, the correctness of the recursive formulation is inductively proved as follows.

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Theorem 1: The recursive formulation of will produce correct sum for any number of bits and will terminate within a finite time.

Proof: We prove the correctness of the algorithm by induction on the required number of iterations for completing the addition (meeting the terminating condition).

Basis: Consider the operand choices for which no carry propagation is required, i.e., $C^0_i = 0$.The proposed formulation will produce the correct result by a single-bit computation time and terminate instantly as (4) is met. Thus, all the single-bit adders will successfully kill or propagate the carries until all carries are zero fulfilling the terminating condition. The mathematical form presented above is valid under the condition that the iterations progress synchronously for all bit levels and the required input and outputs for a specific iteration.

III. PROPOSED ADDER SCHEMATIC

GDI method is based on the use of a simple cell as shown in Fig 3. The basic GDI cell looks like the standard CMOS inverter, but there is an important difference that GDI cell contains 3 inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).

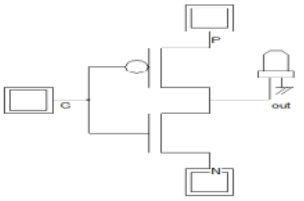

Fig 3: Basic Gate Diffusion Input Cell

No of different logic functions can be implemented by only two transistors by using Gate diffusion input (GDI) approach. GDI approach is suitable for design of high speed, power efficient circuits with improved logic level swing and static power characteristics using a reduced number of transistors as compared to CMOS and PTL techniques[17],[18].

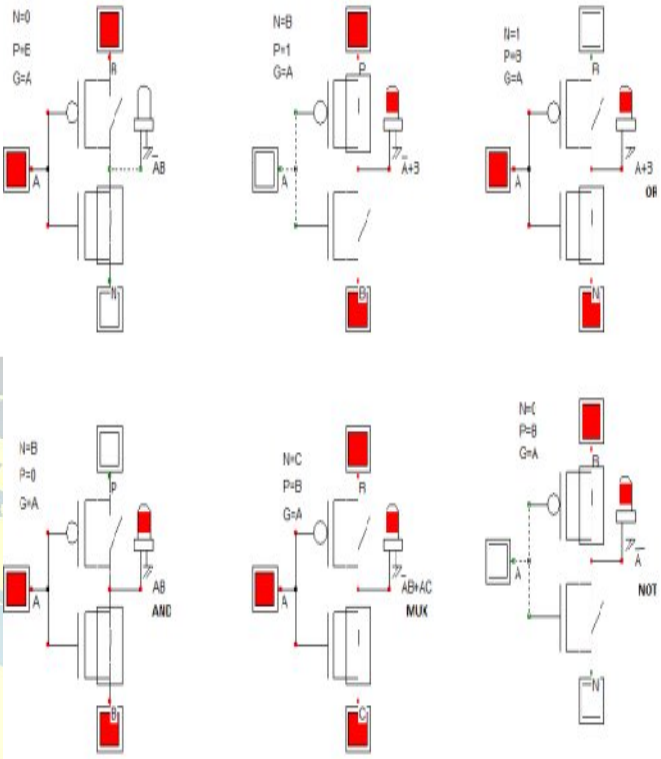

Fig 4: Various Function of Basic GDI Cell

Various logic functions of GDI cell for different input combination is shown in Fig 4. Six different functions can be implemented by GDI cell. Coloured box and output LED is showing high output.

The design of propose full adder consists three modules. Module1 comprises 5T XOR –XNOR module. Module 1 produces two intermediate signals which are passed to the module 2 and module 3 to obtain sum and carry output as shown in Fig 5. Module 2 and 3 are GDI 2x1 MUX with different input and select lines which produce carry and sum output respectively. Module 1 produces two outputs A⊕B and A⊗B. For module 2, A⊕B acts as a select line and A, C as inputs. On the other hand for module 3, C act as a select line and A⊗B and A⊕ B as inputs. Proposed full adder design is hybridized design because two different logic styles have been used to make the full adder. Module 1 has been made by PTL logic and GDI technique has been used for module 2 and 3.

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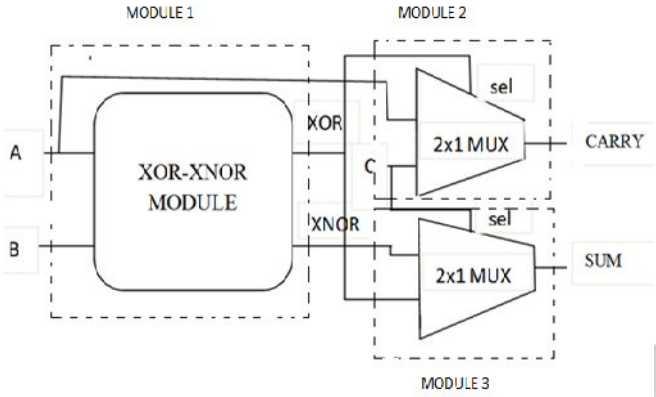

Fig 5: Logic Block Diagram of Proposed Full Adder

Proposed full adder has been implemented by using only 9 transistors i.e. five transistors in module 1 and module 2and 3 has been implemented by using 2T GDI cell. Sum is realized by module 1 and module 3 as per equation 6 and carry is realized by module 1 and module 2 as per equation 7. Module 1 has been implemented by proposed 5T XOR-XNOR module and GDI technique has been used for module 2 and 3. In module 1 a combined XOR-XNOR cell is used to drive the selection lines and, control signal lines of the multiplexer in module 2 and 3. Proposed XOR-XNOR module in Fig 6 has been designed by the PTL logic.

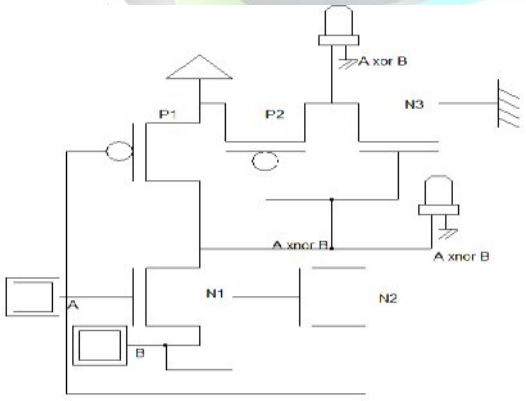

Fig 6: Proposed PTL based XOR-XNOR Module

Proposed design has been made by 3 NMOS and 2 PMOS transistors which provide an area efficient design as compared to previous discussed designs [5], [6], [11], [15], [16].

TABLE 1
ANALYSIS OF PROPOSED XOR-XNOR MODULE

Inputs			MOS Logic State			Output		
A	**B**	**N1**	**N2**	**N3**	**P1**	**P2**	A⊕B	A⊙B
0	0	OFF	OFF	ON	ON	OFF	0	1
0	1	OFF	ON	OFF	ON	ON	1	0
1	0	ON	OFF	OFF	OFF	ON	1	0
1	1	ON	ON	ON	OFF	OFF	0	1

Verification and simulation of the functionality of proposed XOR-XNOR module is first done by using Tanner tool. Outputs of module 1 act as inputs for the module 2 and module 3.It is shown in Fig 7. The logical Boolean expression for module 2 and 3 can be expressed as:

$$SUM = C(A \otimes B) + \overline{C}(A \oplus B) \quad (6)$$

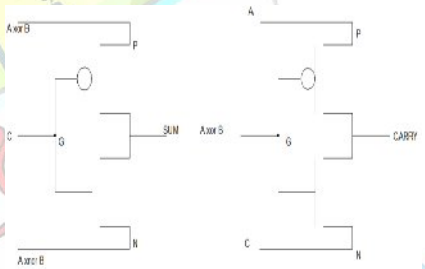

Fig 7: Use of GDI Cell as Module 2 and3

$$CARRY = C(A \oplus B) + A(A \otimes B) \quad (7)$$

Schematic of proposed full adder has been designed as shown in Fig 8 and simulated using Tanner Tool.

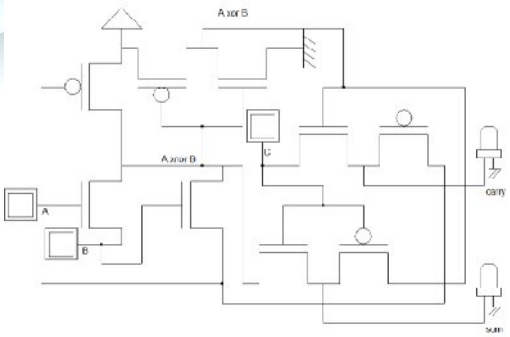

Fig 8: Proposed 9T Hybrid Full Adder Design

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IV. SIMULATION RESULTS

In this section, we present simulation results for hybrid full adder using tanner tool version 13.0.The performance of proposed hybrid full adder has been evaluated in terms of area and power on 130nm technology.

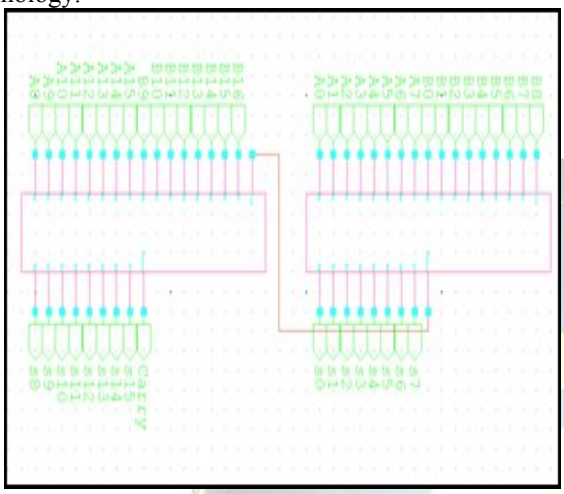

Fig 9: Implementation of 16-bit full Adder based on PTL and GDI technique in Tanner tool

Implementation and timing diagram of 16-bit full Adder based on PTL and GDI technique in Tanner tool is shown in Fig 9 and Fig 10. Proposed full adder has shown improvement in terms of area, power and current as compared to other full adder design. Proposed full adder has shown improvement in terms of area, power and current as compared to other full adder design.

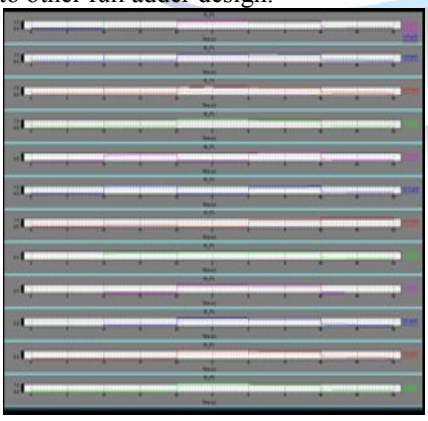

Fig 10: Timing Simulation of Proposed 16-bit Hybrid Full adder

Results show that area consumed by the proposed hybrid adder is 98.5µm2 on 130nm technology. At 1.8V input supply voltage the proposed adder has shown an improvement of 62% in power and 59.85 % in current on 130nm technology as compared to Existing PASTA Design. Result comparison of proposed full adder with PASTA Design has shown in Table-2.

TABLE 2
COMPARISON OF PARAMETERS OF PROPOSED FULL ADDER WITH PASTA DESIGN

PARAMETERS	16-BIT PASTA ADDER	16-BIT PTL AND GDI BASED FULL ADDER
AVERAGE POWER	$5.8240 * 10^{-3}$ W	$3.5979 * 10^{-3}$ W
MAXIMUM POWER	$3.5777 * 10^{-2}$ W at $1.500 * 10^{-5}$ secs	$2.1416 * 10^{-2}$ W at $1.00 * 10^{-5}$ secs
MINIMUM POWER	$3.6648 * 10^{-5}$W at $1.000 * 10^{-5}$ secs	$2.1041 * 10^{-7}$W at$4.000 * 10^{-5}$ secs
POWER DELAY PRODUCT	0.536 µws	0.214 µws
ENERGY DELAY PRODUCT	8.049 pws	2.141pws
STATIC CURRENT	1.9876amps	1.1897amps

V. CONCLUSION

An alternative hybrid full adder design by using PTL based XOR-XNOR module and GDI MUX has been introduced which consist only 9 transistors. Proposed full adder has been implemented by using 5 NMOS and 4 PMOS transistors. A new area efficient XOR-XNOR module has been proposed which is designed by only 5 transistors. Proposed XOR-XNOR model consume 49.7µm2 area at 130nm. Proposed module has been also compared in terms of area from other existing XOR-XNOR modules and proposed XOR-XNOR module has been proven area efficient as compared to other. This XOR-XNOR module has been used as a basic module in proposed hybrid full

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adder. Area and simulation of proposed full adder has been shown on 130nm technology. Area of proposed design is 98.4µm2 on 130nm technology. At 1.8V input supply voltage the proposed adder has shown an improvement of 62% in power and 59.85% in current. Simulation result shows that the power consumption and current is less compared PASTA Design.

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