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High Speed and Reduced Area 16 bit Vedic Multiplier Using Carry Select Adder

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Abstract---. Processors speed depends greatly on the speed of multipliers.This paper gives the novel method of multiplier using vedic mathematics that rediscovered from ancient maths.High speed 16 bit Vedic multiplier architecture which is quite different from the conventional method and vedic multiplier designed using carry select adder is proposed in this paper.Multiplier operation based on Urdhva Tiryakbhayam Sutra which is highly preferred algorithm for multiplication that increases multiplier speed by reduced iteration.

Keywords---Ripple Carry Adder (RCA), Vedic multiplier using RCA and Carry Select Adder (CSLA), Vedic mathematics, Urdhva Tiryakbhyam sutra**.**

I. INTRODUCTION

Ever increasing the demand in enhancing the ability of processors to handle the complex and challenging processes has been resulted in the integration of a number of processor cores into a single chip. Still the load on the processor is not less in generic system. This load is reduced by supplementing the main processor with co-processors, which are designed to work upon specific type of functions like numeric computation, signal processing, graphics etc. In algorithmic and structural levels, numerous multiplication techniques have been developed to enhance the efficiency of the multiplier which concentrates in reducing the partial products and the methods of their addition but the principle behind multiplication remains the same in all cases. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras [3]. Employing these techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area, power etc. Though there are many sutras employed to handle different sets of numeric, exploring each one gives new results. My work has proved the efficiency of Urdhva Triyakbhyam-Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of in termed Urdhvaiate products, eliminates unwanted multiplication steps with zeros. This sutra is to be used to build a high speed power efficient multiplier in the coprocessor. Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors [4]. Vedic Mathematics has a unique technique of calculations based on 16 Sutras [2]. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. Further, the Verilog HDL coding of Urdhva Tiryakbhyam Sutra for 8x8 bit multiplication. Urdhva–Triyakbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise. “Urdhva-Tiryakbhyam” sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently is given by [1]. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work. As an enhancement here I use ripple Carry adder circuit.

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For the purpose of reducing the complexity in multiplication Vedic multiplication is used in this work with the help of reduced Carry Select Adder for addition process. The design of Vedic multiplier consists of only less number of gates thereby reducing the gate count and delay. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. Vedic Mathematics has a unique technique of calculations based on 16 Sutras. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift.

II. VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. The very word „Veda has the derivational meaning i.e. the fountainhead and illimitable storehouse of all knowledge. Vedic mathematics is the name given to the ancient system of mathematics or, to be precise a unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved, be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

A.These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat -If one is in ratio, the other is zero.
2) ChalanaKalanabyham -Differences and similarities.
3) Ekadhikina Purvena- By one more than the previous One.
4) Ekanyunena Purvena -By one less than the previous one.
5) Gunakasamuchyah-Factors of the sum are equal to the sum of factors.
6) Gunitasamuchyah-The product of sum is equal to sum of the product.
7) Nikhilam Navatashcaramam Dashatah -All from 9 and last from 10.
8) Paraavartya Yojayet-Transpose and adjust.
9) Puranapuranabyham -By the completion or noncompletion.
10) Sankalana- vyavakalanabhyam -By addition and by subtraction.
11) Shesanyankena Charamena- The remainders by the last digit.
12) Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
13) Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam -Vertically and crosswise.
15) Vyashtisamanstih -Part and Whole.
16) Yaavadunam- Whatever the extent of its deficiency.

*B.Sub sutras or Corollaries :*Proportionately the remainder remains constant
The first by the first and the last by the last

For 7 the multiplicand is 143

- By osculation
- Lessen by the deficiency
- Whatever the deficiency lessen by that amount and Set up the square of the deficiency
- Last Totalling 10
- Only the last terms
- The sum of the products
- By alternative elimination and retention
- By mere observation, The POS is the sum of the Products.

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III. URDHVA TIRYAKBHYAM SUTRA

Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the Urdhva Tiryakbhyam Sutra is one of the most highly preferred algorithms for performing multiplication. The algorithm is competent enough to be employed for the multiplication of integers as well as binary numbers. The term "Urdhva Tiryakbhyam" originated from 2 Sanskrit words Urdhva and Tiryakbhyam which mean "***vertically***" and "***crosswise***" respectively. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques, is the fact that it utilizes only logical "AND" operations, half adders and full adders to complete the multiplication operation. Also, the partial products required for multiplication are generated in parallel and apriori to the actual addition thus saving a lot of processing time.

Let us consider two 8 bit numbers A_7 -A_0 and B_7-B_0, where 0 to 7 represent bits from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). P_0 to P_{15} represent each bit of the final computed product. It can be seen from equation (1) to (15), that P_0 to P_{15} are calculated by adding partial products, which are calculated previously using the logical AND operation. The individual bits obtained from equations (1) to (15), in turn when concatenated produce the final product of multiplication which is depicted in (16).The carry bits generated during the calculation of the individual bits of the final product are represented from C_1 to C_{30}. The carry bits generated in (14) and (15) are ignored since they are superfluous.

A.Method of Urdhva Tiryakbhyam calculation

$$P_0 = M_0 * N_0 \quad (1)$$

$$C_1P_1 = (M_1 * N_0) + (M_0 * N_1) \quad (2)$$

$$C_3C_2P_2 = (M_2 * N_0) + (M_0 * N_2) + (M_1 *N_2) + C_1 \quad (3)$$

$$C_5C_4P_3 = (M_3 * N_0) + (M_2 * N_1) + (M_1 *N_2) + (M_0 * N_3) + C_1 \quad (4)$$

$$C_7C_6P_4 = (M_4 * N_0) + (M_3 * N_1) + (M_2 * N_2) + (M_1 * N_3) + (M_0 * N_4) + C_3 + C_4 \quad (5)$$

$$C_{10}C_9C_8P_5 = (M_5 * N_0) + (M_4 * N_1) + (M_3 * N_2) + (M_2 * N_3) + (M_1 * N_4) + (M_0 * N_5) + C_5 + C_6 \quad (6)$$

$$C_{13}\,C_{12}C_{11}P_6 = (M_6 * N_0) + (M_5 * N_1) + (M_4 * N_2) + (M_3 * N_3) + (M_2 * N_4) + (M_1 * N_5) + (M_0 * N_6) + C_7 + C_6 \quad (7)$$

$$C_{16}\,C_{15}C_{14}P_7 = (M_7 * N_0) + (M_6 * N_1) + (M_5 * N_2) + (M_4 * N_3) + (M_3 * N_4) + (M_2 * N_5) + (M_1 * N_6) + (M_0 * N_7) + C_9 + C_{11} \quad (8)$$

$$C_{16}\,C_{15}C_{14}P_7 = (M_7 * N_1) + (M_6 * N_2) + (M_5 * N_3) + (M_4 * N_4) + (M_3 * N_5) + (M_2 * N_6) + (M_1 * N_7) + C_{10} + C_{12} + C_{14} \quad (9)$$

$$C_{22}C_{21}C_{20}P_9 = (M_7*N_2) + (M_6*N_3) + (M_5*N_4) + (M_4*N_5) + (M_3*N_6) + (M_2*N_7) + C_{13}+C_{15}+C_{17} \quad (10)$$

$$C_{25}C_{24}C_{23}P_{10} = (M_7*N_3) + (M_6*N_4) + (M_5*N_5) + (M_4*N_6) + (M_3*N_7) + C_{16}+C_{18}+C_{20} \quad (11)$$

$$C_{27}C_{26}P_{11} = (M_7*N_4) + (M_6*N_5) + (M_5*N_6) + (M_4*N_7)+C_{19}+C_{21}+C_{23} \quad (12)$$

$$C_{29}C_{28}P_{12} = (M_7*N_5) + (M_5*N_6) + (M_5*N_7) + C_{22}+C_{24}+C_{26} \quad (13)$$

$$C_{30}P_{13} = (M_7*N_6) + (M_6*N_7) + C_{25}+C_{27}+C_{28} \quad (14)$$

$$P_{14} = (M_7*N_7) + C_{29} + C_{30} \quad (15)$$

$$P_{15} = (M_7*B_7) \quad (16)$$

Further these equations are modified to get the partial product results. The results of partial products for 16-bit Vedic multiplication are demonstrated from (17) to (31).

$$P_0 = M_0 * N_0 \quad (17)$$

$$P_1 = (M_1 * N_0) \oplus (M_0 * N_1) \quad (18)$$

$$P_2 = (M_2 * N_0) \oplus (M_0 * N_2) \oplus (A_1 * B_1) \quad (19)$$

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$P_3 = (M_3 * N_0) \oplus (M_2 * N_1) \oplus (M_1 * N_2) \oplus (M_0 * N_3)$

(20)

$P_4 = (M_4 * N_0) \oplus (M_3 * N_1) \oplus (M_2 * N_2) \oplus (M_1 * N_3) \oplus (M_0 * N_4)$
(21)

$P_5 = (M_5 * N_0) \oplus (M_4 * N_1) \oplus (M_3 * N_2) \oplus (M_2 * N_3) \oplus (M_1 * N_4) \oplus (M_0 * N_5)$ **(22)**

$P_6 = (M_6*N_0) \oplus (M_5*N_1) \oplus (M_4*N_2) \oplus (M_3*N_3) \oplus (M_2*N_4) \oplus (M_1*N_5) \oplus (M_0*N_6)$ **(23)**

$P_7 = (M_7*N_0) \oplus (M_6*N_1) \oplus (M_5*N_2) \oplus (M_4*N_3) \oplus (M_2*N_5) \oplus (M_1*N_6) \oplus (M_0*N_7)$ **(24)**

$P_8 = (M_7*N_1) \oplus (M_6*N_2) \oplus (M_5*N_3) \oplus (M_4*N_4) \oplus (M_3*N_5) \oplus (M_2*N_6) \oplus (M_1*N_7)$
(25)

$P_9 = (M_7*N_2) \oplus (M_6*N_3) \oplus (M_5*N_4) \oplus (M_4*N_5) \oplus (M_3*N_6) \oplus (M_2*N_7)$
(26)

$P_{10} = (M_7*N_3) \oplus (M_6*N_4) \oplus (M_5*N_5) \oplus (M_4*N_6) \oplus (M_3*N_7)$
(27)

$P_{11} = (M_7 * N_4) \oplus (M_6 * N_5) \oplus (M_5 * N_6) \oplus (M_4 * N_7)$

(28)

$P_{12} = (M_7 * N_5) \oplus (M_5 * N_6) \oplus (M_5 * N_7)$ **(29)**

$P_{13} = (M_7 * N_6) \oplus (M_6 * N_7)$ **(30)**

$P_{14} = (M_7 * N_7)$ **(31)**

Fig.1 Graphical representation of Urdhva Tiryakbhyam sutra

IV. VEDIC MULTIPLIER USING RIPPLE CARRY ADDER AND CARRY SELECT ADDER

Carry select adder (CSLA) is the combination of two Ripple Carry Adders (RCAs). Ripple carry adder based Vedic multiplier gives the better result as compared to compressor based Vedic multiplier. Advantage of ripple carry adder based Vedic multiplier is an area reduction but speed must be low. Hence we propose a novel method of Vedic multiplier using carry select adder.

Carry select adder is the advanced adder circuit that undergoes in this research. This paper gives a new method of Vedic multiplier using carry select adder. The conventional Carry Select Adder consists of dual RCA or RCA&BEC combinations for implementation of addition process. In each of these type yields better results when compared to the performance RCA circuits. However, dual RCA or single RCA results in poor performance which again causes more delay and area consumption problem. In order to reduce this problem, in this paper reduced Carry Generations based CSLA has been introduced with the help of less number of slices and chip size.

In conventional CSLA circuit, two number of RCA involved for the addition process, these are indicated as RCA-0 (RCA when Carry input 0) and RCA-1 (RCA when Carry input 1). To design a single N-bit RCA circuit, there will be require a single half adder and N-1 full adder

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circuits [8]. These complexities are reduced in our proposed work. The sequence of AND and OR operations take care the results of a single RCA. Hence, we can reduce the overall circuit complexity for CSLA. Generally dual RCA units in CSLA represents as the Carry Generation (CG) unit [5]. Therefore our new designed CSLA called as the reduced CG based CSLA, Simply also referred as reduced CSLA. The conventional circuit for 16-bit Vedic multiplier with the help of RCA circuits is illustrated in fig 2. The circuit of proposed reduced CSLA is illustrated in fig 3.

Vedic multiplier is one of the best multipliers for multiply the two n-bit binary integer values. In conventional n-bit Vedic Multiplier, four (n/2) X (n/2) Vedic multiplier and three (2n)-bit Ripple Carry Adders (RCAs) performs the multiplication operation.

This multiplication process provides results with average performance in terms of area and delay. However, there are some limitations in conventional Vedic Multiplier. Initially, the conventional Vedic multiplier generates correct values for multiplication when carry of second RCA leads to zero, otherwise it generates incorrect values for multiplication. When large bit of binary multiplication this circuit yields absolutely incorrect results. Secondly, RCA gives large propagation delays for performing addition process.

In order to overcome this problems, Vedic multiplies is modified in this paper. Modified Vedic multiplier consists of four (n/2) X (n/2) Vedic multiplier and two (2n)-bit advanced Carry Select Adder (Reduced CSLA).

When compared to RCA circuits, reduced CSLA circuit gives better performance in terms VLSI concerns. Further third RCA in conventional Vedic multiplier is replaced by six half adders (HAs) and a single full adder (FA) circuit for reduce the occupied slices for n-bit multiplication.

In addition, modified Vedic multiplier provides correct results for multiplication at any large bit binary numbers. The proposed 16-bit Vedic multiplier with the help of reduced CSLA is illustrated in fig 4

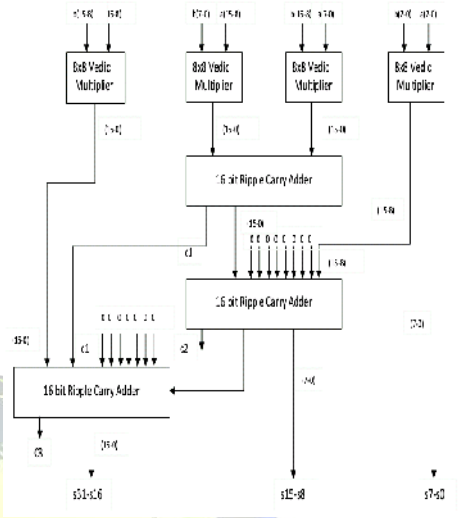

Fig.2. Ripple Carry Adder based Vedic multiplier

When compared to the compressor based Vedic multiplier, reduced CSLA based Vedic multiplier offers 27.27% reduction in area and 35.32% reduction in delay

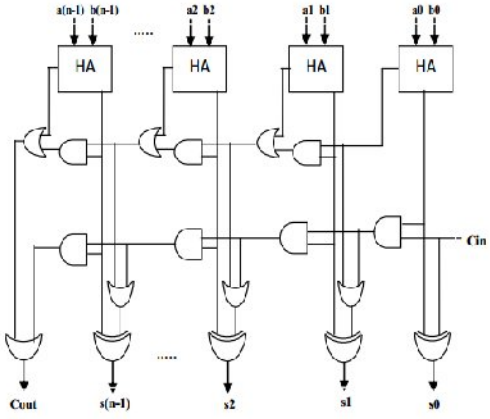

Fig.3. Reduced CSLA

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Further the comparison of Compressor based Vedic multiplier; Ripple Carry based Vedic multiplier and Reduced CSLA basVedic multiplier is shown in table 1.

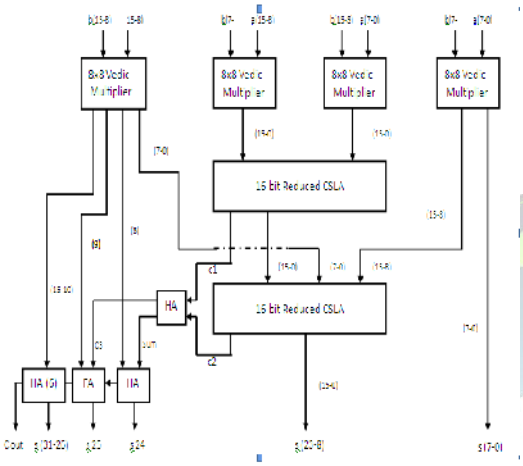


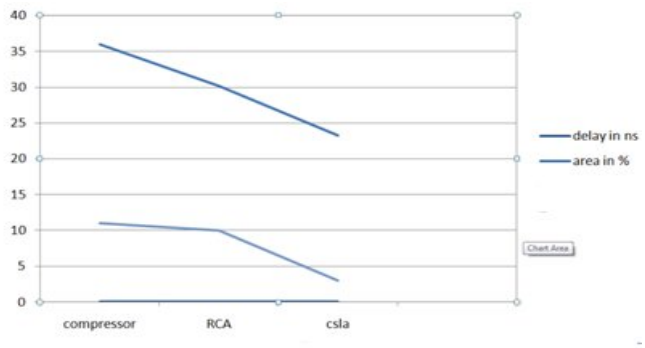
Fig.4.Carry select adder based Vedic multiplier

Similarly when compared to the RCA based Vedic multiplier, reduced CSLA based Vedic multiplier offers 30% reduction in area and 23%reduction in delay.

Table 1 Comparison of different types of Vedic Multipliers with proposed Vedic multiplier

Method of Multipliers	Number of LUTs(%)	Delay obtained(ns)
Compressor based Vedic multiplier	11	35.974
Ripple carry adder based vedic multiplier	10	30.219
Carry select adder based vedic multiplier	3	23.268

As comparing the proposed reduced CSLA based Vedic multiplier into different types of Vedic multiplier, the proposed Vedic multiplier offers best performance in terms of area and delay. It must be widely used for communication purposes. Generally the high speed processors having the multiplier blocks they need the high speed multipliers. This paper gives idea for choosing the best method of multiplier in any high speed processors.



Graph.1.Representation of output analysis.

From the analysis vedic multiplier gives the better performance as compared to other techniques of multiplication.

VI.CONCLUSION

In this paper, reduced CSLA based Vedic multiplier is designed. Vedic mathematics is method of parallel multiplication that tends to high speed and reduced delay. The vast reduction in the total number of gates is advantageous in terms of both area and delay. Generally, the addition part of Vedic multiplication and partial product generation of Vedic multiplication makes the best performance in terms of area and delay. In this paper, conventional CSLA circuit has re-designed with the help of only less number of hardware. Hence a result of adder is reducing the area and delay effectively than conventional one. Further this proposed adder is incorporated into Vedic multiplier in order to add the partial product results. Also the final stage of Vedic multiplier is re-designed by using less hardware instead of RCA circuit, which yields better performance for multiplication in terms of area and delay.

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