ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 2, Issue 2, February 2015

Nine Level Cascaded Full Bridge Topology for Transformerless System

Jenitha V[1], Annam M[2]
P.G Scholar, Department of Power Electronics and Drives, Dr.Sivanthi Aditanar College of Eng, Tiruchendur[1]
Assistant Professor,Department of EEE, Dr.Sivanthi Aditanar College of Eng, Tiruchendur[2]

Abstract-This paper deals "A Nine Level Cascaded Full Bridge Topology for Transformer less System". Nine levels are bridges with different dc-link voltages. One of the bridges is supplied by dc source and another is supplied by a flying capacitor. The main objective is to reduce the harmonic distortion and electromagnetic interference. By designing a transient circuit ground leakage current can be minimized. MATLAB /Simulations are performed to show the best results.

Keywords: Cascaded full bridge, Flying capacitor voltage regulation, transient circuit, ground leakage current.

I. Introduction

Multilevel converters have been investigated for years but only recently have the results of such researches found their way to commercial photovoltaic (PV) converters. Classical designs of PV converters use transformers which is heavy and costly. In order to reduce cost, weight and to improve efficiency transformer less architectures is preferred. Removing the grid frequency transformer worsens the output power quality, allowing the injection of dc current into the grid [1],[2] and giving rise to ground leakage current problem [3],[4]. In full bridge based topologies the ground leakage current is mainly due to the high frequency variations of the common mode voltage at the output of the power converter [4]. By reducing the filter size cost and weight is reduced and the efficiency is improved. Multilevel converters subdivide the input voltage among several power devices, allowing for the use of more efficient devices. Multilevel converters were used in high-voltage industrial and power train applications. Single-phase multilevel converters can be divided into three categories based on design: neutral point clamped (NPC), cascaded full bridge (CFB), and custom.

In NPC topologies the electrical potential between the PV cells and the ground is fixed by connecting the neutral wire of the grid to the constant potential, resulting from a dc-link capacitive divider [5]. The advantage of single phase NPC converters is that it is immune from ground leakage currents but it is not true for three phase NPC converters. The main drawback of NPC converter is that they need twice the dc-link voltage compared to the full bridge. CFBs make for highly modular designs. CFB converter needs an insulated power supply that matches with multi string PV fields [6]. This is also proposed for stand-alone applications. CFBs provide degrees of freedom for control strategy.

A CFB consists of n full bridges and if there is a same supply voltage for each full bridge it can able to synthesize 2n+1 voltage levels. More output levels with given number of active devices are possible by custom architectures and it generally requires custom pulse width modulation (PWM) and control schemes [7]-[9]. In CFB structures reduction in the switches-per-output-voltage-level ratio can be achieved by considering different supply voltages for each full bridge [10], [11]. The proposed work consists of two asymmetrical CFBs, generating nine voltage levels.

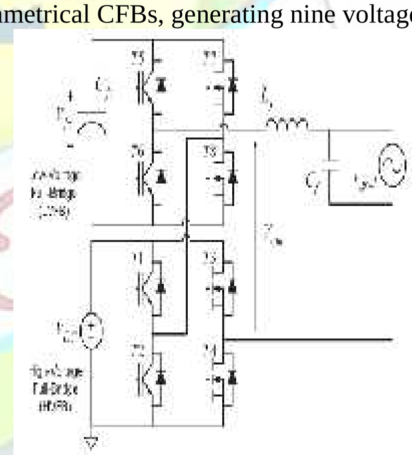

Fig.1. CFB Topology

In fig 1 one of the full bridge is supplied by dc voltage source and the other bridge is supplied by a flying capacitor. The different sets of output levels can be achieved by controlling the ratio between two voltages. The flying capacitor is a secondary energy source that performs limited voltage boosting. Transient Circuit (TC) consists of two low power switches and bidirectional switch to reduce the ground leakage current.

II. Control Strategy Of CFB Topology

The converter consists of two CFBs with one of the bridge is supplied by a flying capacitor and another by a dc source. This basic topology was shown in fig.1. Different PWM strategy can be generated for a grid connected transformer less system. In addition

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 2, Issue 2, February 2015

to PWM strategy other components are added to maintain a low ground leakage current. One leg of the topology is provided by a Insulated-gate bipolar transistors (IGBTs) with fast anti parallel diodes where high frequency hard switching commutations occurs. Other leg consists of low voltage drop Metal oxide semiconductor field effect transistor (MOSFETs) lacking a fast recovery diode.

At steady state flying capacitor voltage V_{fc} is kept lower compared to dc link voltage V_{DC}. The full bridge with the dc link is called high voltage full bridge (HVFB) and the full bridge with the flying capacitor is called the low voltage full bridge (LVFB). Different PWM techniques can be considered. The switching pattern of this topology is shown in Table 1.

III. Operation

The output voltage operates between two specific levels. The boundaries of the operating zones can vary according to the flying capacitor voltage, dc link voltage and the adjacent zones can overlap. This is shown in Fig.2.

The flying capacitor voltage to the converter output is positive in zone A and it is negative in zone B. Depending on the V_{fc}/V_{Dc} ratio different operating zones occur. The converter can generate nine voltage levels when $V_{fc}=V_{Dc}/3$. The voltage of the flying capacitor is difficult to control and so it is regulated by chosing the operating zone of the converter.

The V_{fc} can be added to or subtracted from the HVFB output voltage so that the flying capacitor charge or discharge depending on the operating zone of the converter. When a positive current is injected into the grid the flying capacitor is discharged in zone A and charged in zone B. When the flying capacitor voltage is higher than the reference value, the flying capacitor voltage is controlled by forcing the converter to operate more in A zones. Similarly when it is lower than a reference value it is operated more in B zones.

The switching between 0 and V_{DC}-V_{fc} is obtained by replacing the level V_{fc} by V_{Dc}-V_{fc} when V_{fc} is too low. This is shown in zone 2B. Similarly to switch between V_{fc} and V_{DC} levels V_{Dc}-V_{fc} is replaced with V_{fc} when V_{fc} is too high. This is shown in zone 2A.

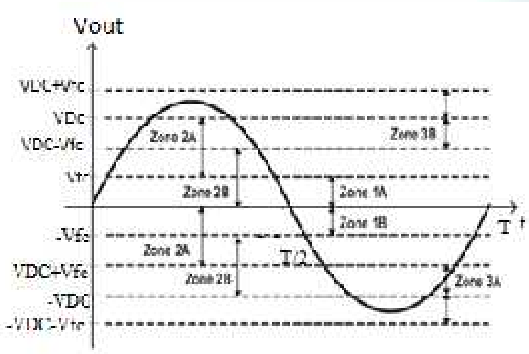

Fig.2. Operating zones when $V_{fc}<0.5V_{DC}$

TABLE I
SWITCHING STRATEGY OF NINE LEVEL CONVERTER

Zone	Switching pattern		
	On devices	**Off devices**	**Switching devices**
Zone 3B	T_2,T_3,T_7	T_1,T_4,T_8	T_5,T_6
Zone 3A	T_2,T_3,T_8	T_1,T_4,T_7	T_5,T_6
Zone 2A	T_3,T_7	T_4,T_8	T_1,T_2,T_5,T_6
Zone 2B	T_3,T_7	T_4,T_8	T_1,T_2,T_5,T_6
Zone 1B	T_1,T_3,T_7	T_2,T_4,T_8	T_5,T_6
Zone 1A	T_2,T_4,T_8	T_1,T_3,T_7	T_5,T_6
Zone 2A	T_4,T_8	T_3,T_7	T_1,T_2,T_5,T_6
Zone 2B	T_4,T_7	T_3,T_8	T_1,T_2,T_5,T_6
Zone 3B	T_1,T_4,T_7	T_2,T_3,T_8	T_5,T_6
Zone 3A	T_1,T_4,T_8	T_2,T_3,T_7	T_5,T_6

IV. Simulation Results

The nine level converter is designed by using MATLAB/Simulink. A dc link voltage is V_{DC} = 100 V is used in the simulations. Resistor R = 10Ω. V_{fc}/V_{DC} is chosen as 0.33. Nine levels are generated with eight switches. For each level four switches are in conduction. T_3 conducts for negative cycle and T_4 conducts for positive cycle. Similarly T_1, T_5, T_7 switches conducts opposite to that of T_2, T_6,T8.

As the level of the voltage increases the harmonic content decreases. The grid voltage is V_{grid} = 230 V which is sinusoidal and the frequency is 50 Hz. If the HVFB voltage is less than the grid voltage then the voltage is supplied from the grid and if it is more than grid voltage then the voltage is supplied to the grid. So that the flying capacitor is charged or discharged.

The dc current injection into the grid is the main problem in most case which leads to ground leakage current. So in order to prevent this the output filter is designed. The filter is composed of capacitor and inductor in which the values are C_f = 1μF and L_f = 1.5 mH respectively. The flying capacitor has the capacitance of C_{fc} = 500 μF.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 2, Issue 2, February 2015

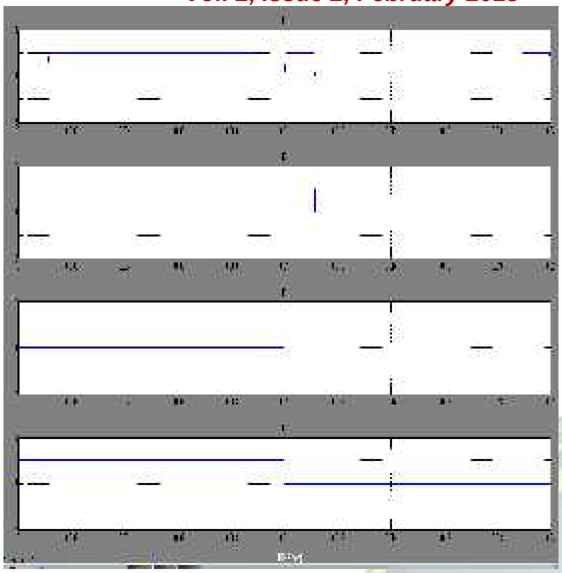

Fig.3. Pulse generation for switches T_1 to T_4

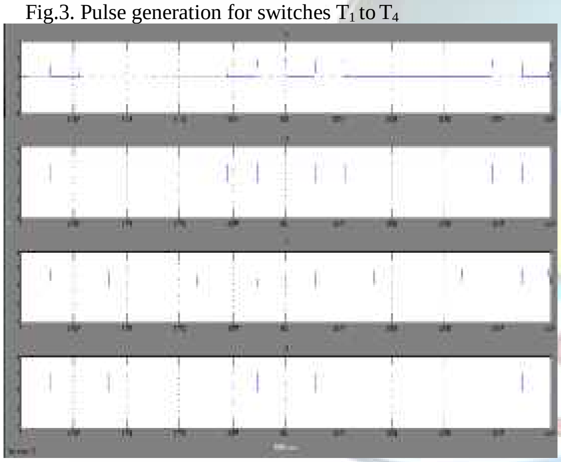

Fig.4. Pulse generation for switches T_5 to T_8

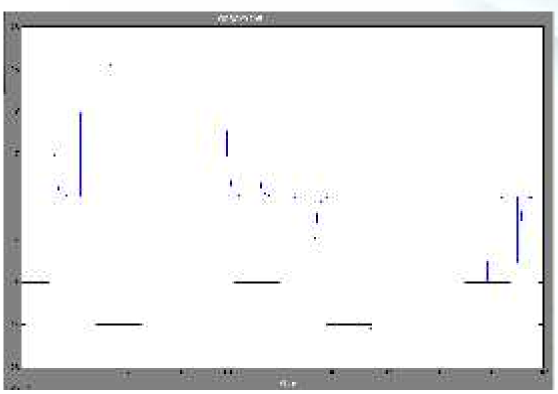

Fig.5. Output voltage for nine level CFB topology

The ground leakage current is reduced by using transient circuit. A transient circuit is designed to decrease the surge currents. The Transient circuit consists of two low power MOSFETs, bidirectional switch, and resistor. This transient circuit is operated during zone 1 when HVFB voltage becomes zero. At this zone either T_1 and T_3 or T_2 and T_4 is on otherwise T_1, T_2, T_3, T_4 are kept off and T_9 switch which is bidirectional switch is kept on. At this point either M_1 or M_2 is kept on. So that parasitic capacitance C_p gets charged through resistor so that limiting the surge current. The pulse for switches T_1 to T_4 shown in fig 3, pulse for switches T_5 to T_8 is shown in fig 4 and the output voltage for nine level CFB topology is shown in fig 5.The transient circuit behaviour is shown in fig 6.

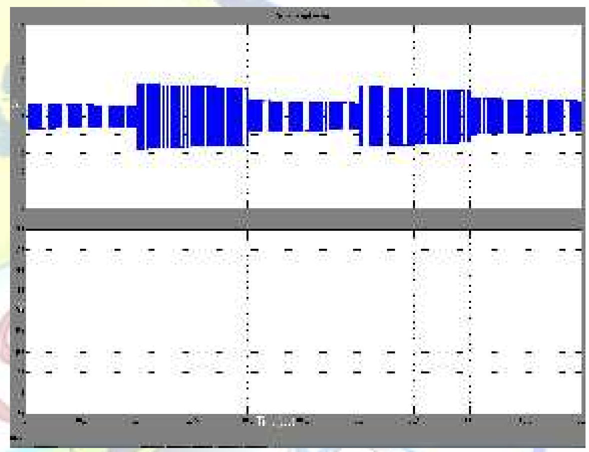

Fig.6. Transient circuit behaviour

V.CONCLUSION

This paper proposed the nine level cascaded full bridge topology with transformer less system with one of the bridge is supplied by a dc source and the other bridge is supplied by a flying capacitor. The flying capacitor is controlled by suitably choosing the operating zone of the converter depending on the output voltage. By controlling V_{fc}/V_{Dc} the nine levels are generated. The operating zones of flying capacitor $V_{fc}/V_{Dc} = 0.33$ is performed using MATLAB/ Simulink.

REFERENCES

[1] G. Buticchi, L.Consolini, and E.Lorenzani, “Active filter for the removal of the dc current component for single-phase power lines,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4403–4414, Oct. 2013.

[2] G. Buticchi and E. Lorenzani, "Detection method of the dc bias in distribution power transformers," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8,pp. 3539–3549, Aug. 2013.

[3] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov. 2010.

[4] O. Lopez, F. Freijedo, A. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy,"Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.

[5] Y. Kashihara and J. Itoh, "The performance of the multilevel converter topologies for PV inverter," in *Proc. CIPS*, Beijing, China, Mar. 2012, pp. 1–6.

[6] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photovoltaic systems with fuzzy logic control," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, Dec. 2010.

[7] N. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[8] N. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[9] J. Selvaraj and N. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 149–158, Jan. 2009.

[10] V. Antunes, V. Pires, and J. Silva, "Narrow pulse elimination PWM for multilevel digital audio power amplifiers using two cascaded H-bridgesas a nine-level converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2,pp. 425–434, Mar. 2007.

[11] D. Zambra, C. Rech, and J. Pinheiro, "Comparison of neutral-point clamped, symmetrical, and hybrid asymmetrical multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2297–2306, Jul.2010.

BIOGRAPHY

Jenitha V received the B.E degree in Electrical and Electronics Engineering from Francis Xavier Engineering College, Tirunelveli in the year 2013. Currently pursuing M.E degree in Power Electronics and Drives from Dr.Sivanthi Aditanar College Of Engineering, Tiruchendur.

Annam M received the B.E degree in Electrical and Electronics Engineering from The Indian College of Engineering in the year 2000. Also received the M.E degree from Sathyabama Institute Of Science and Technology in the year 2006.