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Resistive Switching Memories for Logic Circuits Using PCSA

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Abstract— The Non volatile logic (NVL) architecture consists of the complementary non volatile memories and it is based on resistive switching (RS-NVM). The non volatile memories (NVM) are STT-MRAM, OxRRAM, CBRAM,etc,. Non volatile memory means it can get back stored information even when not powered. This improves the efficiency of power and area, it helps the system to be powered off in idle state thereby, eliminates the static power caused by the leakage current. Here the resistive switching non volatile memory RRAM is integrated with non volatile logic device full adder to optimize power and area requirement and involves fast read/write operation. The logic in memory architecture is used for computing purposes and helps to perform complex logic functions.

Keywords*:* Complementary logic gates, low power, non volatile full adder, resistive switching memories.

I. INTRODUCTION

Memory is one of the most important defining components used in computer system, storage solution and mobile device existence today. The memory system is one of the most critical components of modern computers. It has attained a high level of complexity due to the many layers involved in memory hierarchy such as application software, operating system, cache, main memory and disk. Normally the devices mainly suffer from high power dissipation.

The main sources of power dissipation [1] include static and dynamic dissipation. The static power (off-state) is mainly due to leakage current and dynamic power is due to data transfer from memory to logic units that requires more power. These sources of power dissipation can be reduced by using non volatile memories. The NVM is a non-volatile memory that will retain data once power is turned off. The Non volatile memory is a computer memory that can get back stored information even when not powered. Non-volatile memory (NVM) is typically used for the task of secondary storage or long-term persistent storage. The (RS-NVMs) spin transfer torque magnetic RAM (STT-MRAM), oxide resistive RAM (OxRRAM) and conductive-bridge RAM (CBRAM) these include fast read and write operation. Here the (RRAM) Resistive Random access memory is one type of has emerging technology of non volatile memory. The resistive switching method is used in logic architecture is to reduce amount of power that is dissipated during the operation. Integrating the resistive switching non volatile memory RS-NVM in the Full Adder (NVFA) logic circuit shows an interesting performance in terms of power, area and speed. Resistive random-access memory (RRAM) is a type of non-volatile random access memory, where their resistance can be varied between 0s and 1s non volatile states as high resistance switching and low resistance switching.

II. Non Volatile Spin Transfer Torque Random Access Memory (Stt-Mram) - Principle

Spin-transfer torque is an effect in which the orientation of a magnetic layer in a magnetic tunnel junction or spin valve can be modified using a spin-polarized current. STT-MRAM functionality is enabled by two phenomena are the tunnelling magneto-resistance (TMR) effect for reading and the spin-transfer torque (STT) [3] effect for writing. Magnetic element consisting of two magnetic layers separated by a thin insulating layer. The information is stored in the magnetic state of one of the magnetic layers, called the free layer (FL). A second magnetic layer called the reference layer (RL) provides a stable reference magnetic orientation required for reading and writing.

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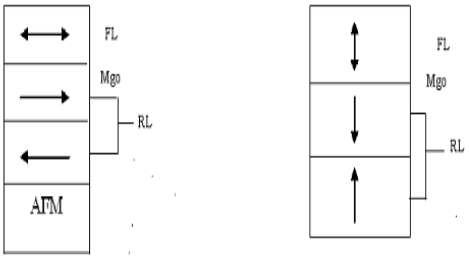

Fig. 1 Design of STT-MRAM cell

Based on the tunnel magneto-resistance (TMR) [10] effect the nanopillar resistance, R_P or R_{AP} depends on the relative orientation, parallel (P) or anti-parallel (AP), of magnetizations in the two FM layers. It simplifies the circuitry as it requires only a bipolar current. The MTJ switches state as the current exceeds a given critical current denoted as I_{C0}. These recent progress demonstrates the perpendicular magnetic anisotropy (PMA) in CoFeB/MgO structures provides a high-energy barrier, to resist the thermal instability of in-plane anisotropy. In STT switching reliability is decreased because of usuage of common read and write is used.

III. Resistive Switching Rram Model

Resistive random-access memory (RRAM) is a type of non-volatile random access computer memory that works by changing the resistance across [5] a dielectric solid-state material often referred to as a mem-resistor. RRAM device contains a component called as memristor, whose resistance varies when voltages are imposed across it. The RRAM stores data using ions as changes in electrical resistance than as electrons. It is an alternative to floating gate flash technology since it is faster and requires less voltage.

RRAM requires less energy to operate and has a greater number of write cycles for a longer lifespan, depending on the components being used. With the ability for high and low levels of resistance, this allows RRAM to store different values on the chip to make up bits of data.

The structure of RRAM memory is always connected serially with NMOS transistor in order to achieve the better controllability of device operation and these acts as cell selector. It has two pulses, when positive pulse is applied a high resistance is generated. When negative pulse is applied, high resistance is disappeared. The oxide thickness is the main parameter determining the value of the forming voltage (V_F), which is typically the highest voltage and needed only once, to get the RRAM cells ready for operation. It has Set (on-switching) and Reset (off-switching) voltages are lower and, in a common situation, do not depend on oxide thickness.

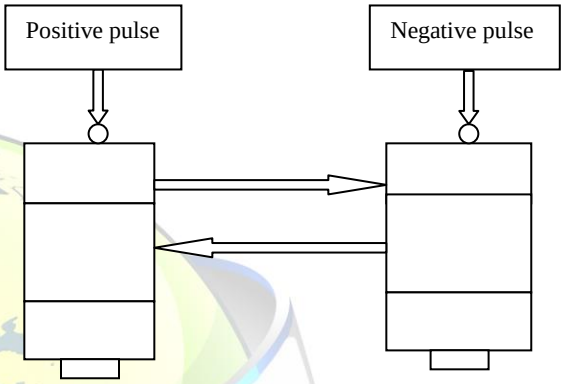

Fig. 2 Model of RRAM

Polarity of the RRAM can be operated by either binary or unary. Bipolar effects cause polarity to reverse when switching from low to high resistance (reset operation) compared to switching high to low (set operation). Unipolar switching leaves polarity unaffected, but uses different voltages.

The Set/Reset (S/R) voltages, as well as the levels of the on/off states, turn out to be essentially independent not only of oxide thickness, but also of cell size. The operation of cell in extreme conditions (i.e. with very deep Reset or strong Set switching) may turn these characteristics invalid, the common situation is consistent with the filamentary nature of the conductive path.

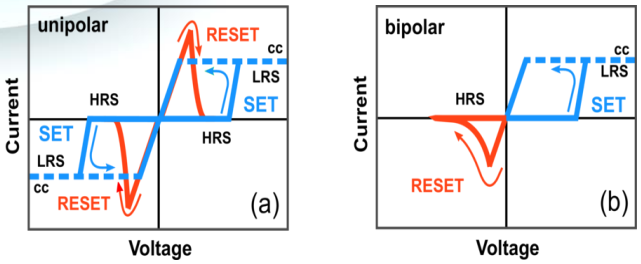

Fig. 3 Resistive switching behaviours of (a) unipolar (b) bipolar

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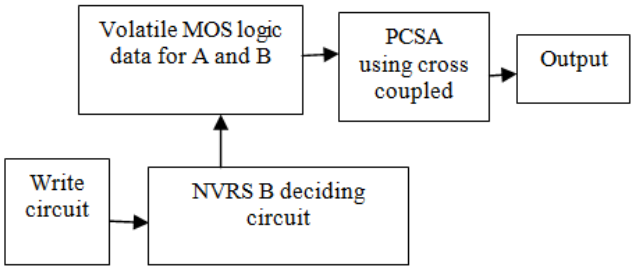
Furthermore, it supports the model of a partial rupture and restoration of the filament during device operation. Therefore, the oxide thickness corresponding to forming-free operation. A RRAM device can be switched between HRS and LRS frequently, but each operation can introduce permanent damage or normally reffered to as degradation. Endurance is also called as electric fatigue is the number of set/reset cycles that can be endured between HRS and LRS are no longer distinguishable.

IV. Synchronous RS-NVL Structure

Synchronous Resistive switching non volatile logic gate structure is composed of three main blocks, as sense amplifier, logic tree, writing circuit with non volatile logic. Here a sense amplifier is used to set the gate outputs, an hybrid MOS/RS-NVMs tree to implement the logic function and a writing circuit to store non-volatile data in the RS-NVM elements.

Sense amplifier and write circuit are used to interface the gate to the surrounding logic while the logic function is build with the MOS/RS-NVMs. In order to perform the logic function, a SA is firstly required as the RS-NVM cell with analog data is integrated directly with the logic circuit. This SA should be fast, robust and consume low power to ensure the computing purpose of this structure. Different from the SA for memory chip, it is impossible to embed error correction circuits (ECC) and to share the circuit for multi-cells.



Fig, 4 Synchronous logic structure

Thereby we use here the pre-charge sense amplifier (PCSA) which shows high performance in terms of reliability, power and speed. There is no capacitance in this structure, which allows better minimization in fabrication.

A. Pre Charge Sense Amplifier

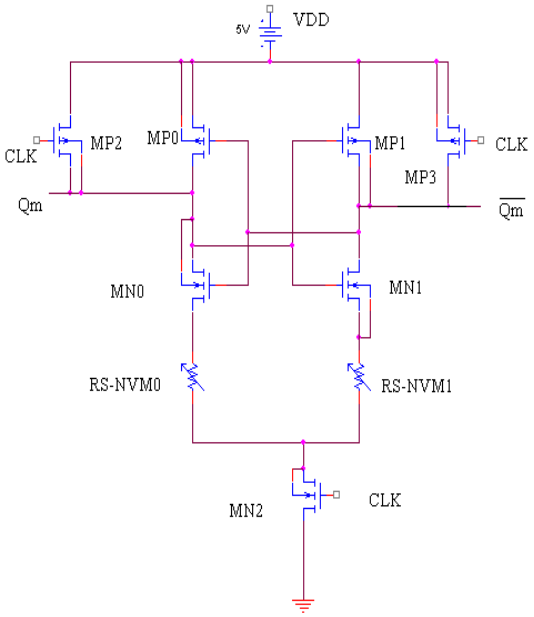


Fig. 5 Schematic diagram of PCSA circuit

The PCSA consists of a pre-charge sub-circuit (MP2 and MP3), a discharge sub-circuit (MN2) and a pair of inverters (MN0-1 and MP0-1), which act as an amplifier. During the first phase, the signal CLK is pulled down and the outputs (Qm and (not)Qm) are pulled up to VDD or logic '1' through MP2-3 while MN2 remains OFF.

During the Evaluation phase, CLK is pulled up, MP2-3 are turned OFF and *MN2* ON. The two hybrid MOS/RS-NVMs branches RS-NVM0 and RS-NVM1 are in complementary states, thus discharge currents are different in the two branches. The lower resistance branch is pulled down to reach the threshold voltage of transistor (MP1 or MP2) more quickly, at the same time, the other branch will be pulled up to VDD or logic '1' and this low-resistance branch will continue to drop to Gnd or logic '0', setting the outputs of the PCSA.

V. Resistive Switching Full-Adder Architecture

This NVFA architecture consists of three blocks representing pre-charge sense amplifier to evaluate the logic value of RS-NVFA outputs, MOS logic for implementing the addition sum and outputting carry and write logic to program the RS memory cells for non volatile memory. In

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this architecture the input 'A' is volatile computing data and input 'B' is a critical data. MOS transistors and RS-NVM are used to represent data 'A' and 'B', respectively.

The PCSA circuit enables providing the best sensing reliability and power efficiency while keeping high-speed performance. For a 1-bit full-adder, the inputs are 'A', 'B', 'Ci' and the outputs are 'SUM', 'Co'.

SUM = ABCi + ABCi + ABCi + ABCi (1)

Co = AB+ ACi + BCi (2)

It has (MP0, 3, 4, 7) as precharge sub-circuit, a discharge sub-circuit (MN16-17) and a pair of inverters (MN0-1, 2-3) and MP (1-2, 5-6), which act as current sense amplifier. The PCSA has two phases Precharge phase and Evaluation phase. during the first phase, 'CLK' is '0', the RS-NVFA outputs are pulled-up to 'VDD' or logic '1' through MP0,3,4,7 while MN16-17 remains OFF. During the second phase CLK is '1', MP0, 3, 4, 7 are turned off and MN16-17 are ON.

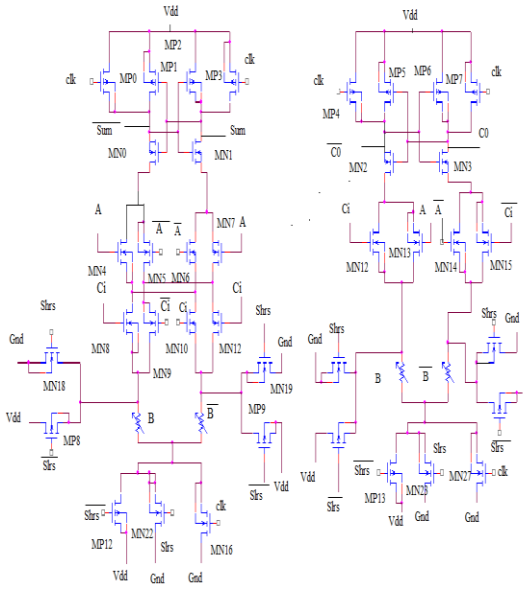

Fig. 6 NVFA architecture based on RS-NVMs

The RSNVFA outputs are pulled-down through the logic tree (MN4-15) and the RS cells. The MOS transistors are controlled with complementary values and RS cells are programmed in opposite resistance states as a control signal (SLRS or SHRS) is activated, the first RS device noted B is put in RHRS or RLRS state. while the second RS device noted B is put in the complementary state RLRS or RHRS. The right branch of the general structure to perform "C_O" logic. The B value is denoted by low resistance switching and high resistance switching.

Table 1. Truth table for carry

A	B	Ci	Resistance comparison	Co
0	0	0	$R_L > R_R$	0
0	0	1	$R_L > R_R$	0
0	1	0	$R_L > R_R$	0
0	1	1	$R_L < R_R$	1
1	0	0	$R_L > R_R$	0
1	0	1	$R_L < R_R$	1
1	1	0	$R_L < R_R$	1
1	1	1	$R_L < R_R$	1

VI. SIMULATION RESULTS

The performance of the Resistive switching non volatile full adder (RS-NVFA) in terms of power and area are simulated using TANNER and MICROWIND tools respectively. Both performance and power have become key factors in efficient memory design. The output window shows the average power requirement for circuit can be obtained using TANNER.

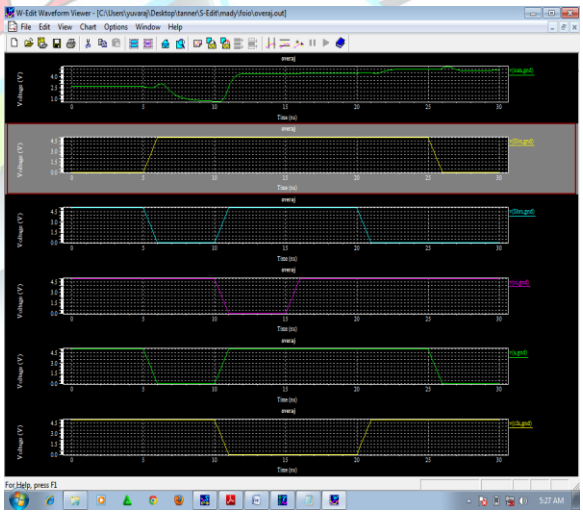

Fig 7(a). Simulation result for sum

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Power Results
v1 from time 0 to 1e-007
Average power consumed -> 7.471807e+004 watts
Max power 5.076041e-002 at time 7.1e-008
Min power 7.425167e-006 at time 4e-008


* END NON-GRAPHICAL DATA

* Parsing                          0.00 seconds
* Setup                            0.01 seconds
* DC operating point               0.00 seconds
* Transient Analysis               0.22 seconds
* ----------------------------------------------
* Total                            0.23 seconds
```

Fig 7(b). Output showing power for sum

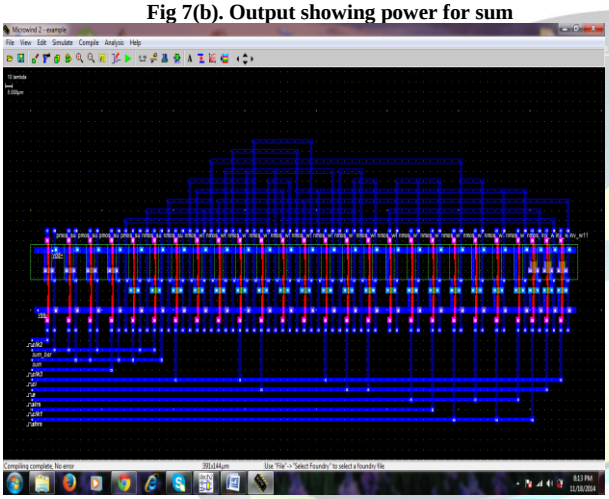

Fig 7(c). Layout simulation for sum

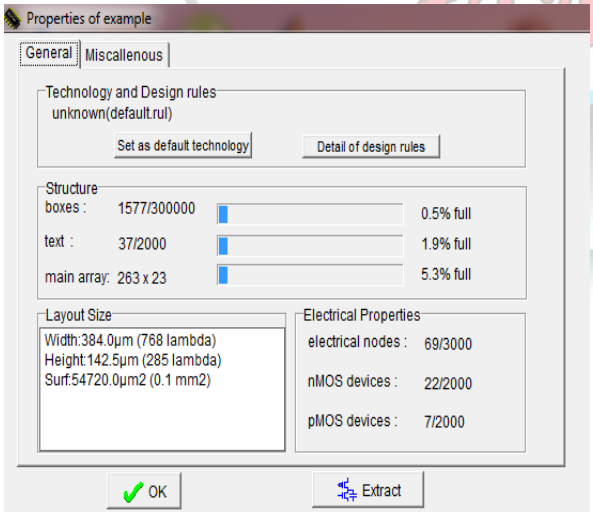

Fig 7(d). Output of area for sum

VII. Conclusion

The non volatile full adder architecture design is proposed using resistive switching method. RS-NVL can able to implement all basic logic functions. It allows a relatively complex function such as full-adder to be built up easily. Mainly it focuses on the power of the architecture. This logic-in-memory architecture gives the average range of power and thereby it reduces the static power dissipation. The operation is mainly depending on synchronous logic gate structure with PCSA, MOS tree and write circuit of NVM. RS-NVM architecture provides fast read and write operation.

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