ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 4, December 2014

Design Of High Throughput MIMO Detectors with Hardware Efficient Architecture

K.JOHN SAMUEL RAJ[1], R.JASMINE ARUL MANI ARASI[2]

Assistant Professor, ECE, SCAD College Of Engineering and Technology, Tirunelveli, India[1]
Student, M.E. VLSI Design, SCAD College of Engineering And Technology, Tirunelveli, India [2]

Abstract— MIMO-OFDM is the foundation for most advanced wireless local area network (Wireless LAN) and mobile broadband network standards. The efficient architecture of 4*4 64-QAM MIMO detectors are mainly used for the wireless communication. The existing architecture embedded large number of buffer memories, increases the chip area and power consumption. In order to reduce the area and power consumption novel error-resilient k-best MIMO detector architecture is used. This paper concentrates to modify the IPM processor and the PCM blocks in MIMO detector architecture. This optimization technique to reduce the power consumption and increase the speed also. The two-way sorting approach mainly used to reduce the power consumption level and also reduce the circuit complexity. This methodology to reduce the internal component level and to design the internal component in tree formation process and modified the child process. And find the minimum distance in the gate component architecture. MIMO detector architecture Synthesis and implementation is done by using Xilinx 14.2i Spartan 3E kit.

Keywords*:* VLSI, MIMODETECTOR, IPM, PCM

I. INTRODUCTION

In radio multiple-input and multiple-output, or MIMO is the use of multiple antennas at both the transmitter and receiver to improve communication performance. Multiple antennas may be used to perform smart antenna functions such as spreading the total transmit power over the antennas to achieve an array gain that incrementally improves the spectral efficiency (more bits per second per hertz of bandwidth,) or achieving a diversity gain that improves the link reliability (reduces fading) or both. The term "mimo" usually refers to method for multiplying the capacity of a radio link by exploiting multipath propagation. This modern mimo is an essential element of wireless communication standards such as ieee 802.11n (wi-fi), ieee 802.11ac (wi-fi), 4g, 3gpp long term evolution, wimax and hspa+. More recently, mimo has been applied to power line communications for 3-wire installations as part of standard itu g.hn and specification homeplug av2.The use of multiple antenna at both transmitter and receiver to improve the communication performance.It offers significant increases in data throughput & link range without additional bandwidth (or) increased transmitter power. Not only do embedded buffering memories occupy a significant portion of the chip area but also a large percentage of the power consumption. According to the international technology roadmap for semiconductors (itrs) report[2],embedded memories are predicted to consume approximately 50%of power consumption for modern socs. In designing mimo detector embedded buffering memories occupy a large portion of chip area and a significant amount of power consumption. In order to design the efficient architecture of novel error resilient k-best mimo detector. 4*4 64 QAM to modify the ipm processor and the pcm blocks in mimo detector architecture. This optimization technique to reduce the power consumption and increase the speed also. The two-way sorting approach mainly used to reduce the power consumption level and also reduce the circuit complexity. This methodology to reduce the internal component level and to design the internal component in tree formation process and modified the child process.

II. SYSTEM DESIGN FLOW

The MIMO architecture mainly used to wireless communication technology and to modify the architecture for MIMO detector using K-best scheme. This method to improve the system performance and used to the error resilient analysis process. This technique to reduce the BUFFER memories architecture based on the CMOS design process. This architecture to optimize the 4*4 QAM multi channel MIMO architecture. This design mainly consider the memory power optimization process and to improve the

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 4, December 2014

system speed. This process mainly used to the two-way sorting algorithm and to optimize the circuit complexity. This architecture consider the two-way sorting approach can achieve the low power consumption and to remove the channel noise and hardware errors. The design approach mainly focused by complexity and power consumption analysis for memory block and overall MIMO architecture. MIMO-OFDM is the foundation for most advanced wireless local area network (Wireless LAN) and mobile broadband network standards. The efficient architecture of 4*4 64-QAM MIMO detector is mainly used for the wireless communication. In this architecture, we implement hierarchical tree arrangement based MIMO 64-QAM detector architecture. This architecture to modify the IPM processor and the PCM blocks in MIMO detector architecture. This optimization technique to reduce the power consumption and increase the speed also. This design to modify the internal mux and d-flip flop arrangement for IPM and PCM block in MIMO- detector architecture

III. TWO-WAYSORTING METHODOLOGY

The two-way sorting approach mainly used to reduce the power consumption level. And also reduce the circuit complexity. This methodology to reduce the internal component level and to design the internal component in tree formation process and modified the child process. The two-sorting methodology to find the error term in the tree formation architecture. And to design the mux and DFF formation in the mimo architecture. And to find the minimum distance in the gate component architecture. The K-best scheme to apply the two-way sorting system. And to optimize the distance in the gate component in overall architecture. To estimate the error analysis process in the k-best algorithm for two-way sorting method and to optimize the processing time and to increase the speed. This method to modify the sorting unit based on the VLSI architecture and to enhance the system performance. And mainly focused by architecture optimization level and to implement the optimize the child process in sorting tree architecture.

A. *Processing Steps*

This method to modify the sorting unit based on the VLSI architecture and to enhance the system performance And mainly focused by architecture optimization level and to implement the optimize the child process in sorting tree architecture. One of the main reasons that the approach presented contains high complexity lies in the fact that it employs an exhaustive enumeration for the child nodes. In other words, while expanding the tree nodes, it considers all the candidates resulting from either the error-free scenario or all possible combinations of error terms. This results in an excessively expanded tree dimension and significantly increased computation overhead. Although a complexity-reduction technique based on the concept of "learning" was utilized, the resulting complexity can still be further decreased. Based on the observation that only one branch (among the error-free and all of the erroneous terms) associated with a certain QAM symbol needs to be expanded; in this section, we propose a novel node-enumeration strategy that does not require the computation of all the distances of erroneous branches. Assuming 16-QAM modulation with the real-value decomposition, the parent node at level can possibly expand to four children at level. However, by considering the scenario of only one bit flip at the MSB (which could result into positive or negative errors), four more children per each error scenario needs to be examined. Furthermore, considering the other single-bit flips at the remaining integer bits will significantly increase the number of child nodes being examined and branch distances being calculated. This will result into an explosion of the computation complexity. However, considering the fact that only one distance should be associated with each one of the four children, it can be argued that, for each QAM symbol, only the branch with the minimum distance should be valid and needs to be saved. Only the smallest distance out of the three distances for any given modulation symbol is selected. The first step is per parent node, for each symbol in the QAM scheme, to identify the one with minimum branch metric considering both error-free term and all of the erroneous terms. The second one is the typical sorting of the best K survivors out of all of the candidate child nodes. In the sequel, we will present an efficient algorithm to realize this two-way sorting. Considering the scenario of one-bit flip at any of the bits of the integer part, there exist possible errors.

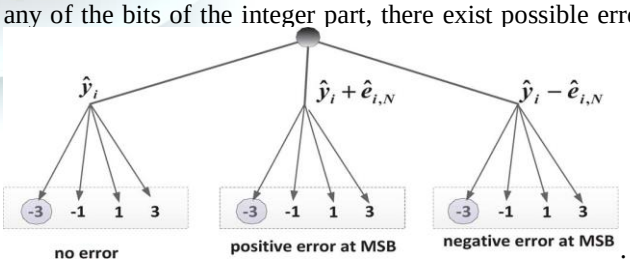

Fig. 1 Tree structure with erroneous children nodes using 16-QAM.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 4, December 2014

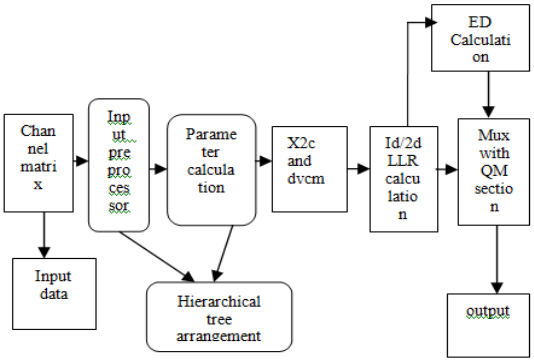

Fig. 2 System Architecture

B. *Hierarchical Tree*

A tree is a non-linear data structure that consists of a root node and potentially many levels of additional nodes that form a hierarchy. A tree can be empty with no nodes called the null or empty tree. A tree is a structure consisting of one node called the root and one or more sub trees. The tree elements are called "nodes". The lines connecting elements are called "branches". Nodes without children are called leaf nodes, "end-nodes", or "leaves". The hierarchical tree arrangement used to MIMO design based PCM and the IPM architecture. This technique to optimize the gate pattern count for the MIMO architecture

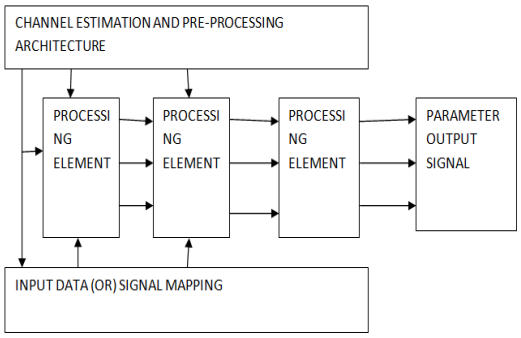

Fig. 3Two way sorting

C. *MIMO Design*

The energy efficiency has become one of the hot studies in MIMO wireless communication systems in the last decade. An energy-efficiency model for cellular networks considering spatial distributions of traffic load and power consumption was proposed. The MIMO architecture worked with the digital based form process and to modify the circuit for regular architecture and the modification process depends on the IPM and PCM blocks.

D. Input Preprocessor Module (IPM)

The input data of PCM for MIMO mode by reordering the estimated channel vectors and received signal vector. Especially, the column-switching of the channel matrix, H, is performed for multi-stage pipelining in case of SM mode. Since the vertical coding for SM(special multiplexing) mode is generally specified in most recent wireless communication standards. Therefore, LLR values are generated sequentially by column-switching in IPM and the hardware blocks are fully shared to reduce the complexity in the proposed architecture.

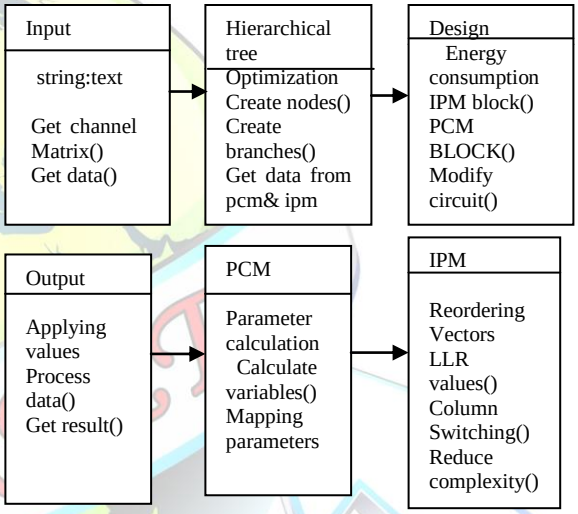

Fig. 4 MIMO Class Diagram

PCM calculates the parameters, which are the commonly required operations for both SD (sphere detection) and SM modes. It is used to calculating the decision variable in DVCM is utilized as the channel state information (CSI). In case of SM mode, all the parameters are mapped to the input data. This PCM block and IPM block to be modified and to apply the hierarchical tree formation in the internal architecture of MIMO. So we design only these two blocks.

F. Two Way Sorting Algorithm

The two-way sorting approach mainly used to reduce the power consumption level. And also reduce the circuit complexity. This methodology to reduce the internal component level and to design the internal component in tree formation process and modified the child process. The two-sorting methodology to find the error term in the tree

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 4, December 2014

formation architecture. And to design the mux and DFF formation in the mimo architecture. And to find the minimum distance in the gate component architecture. The K-best scheme to apply the two-way sorting system. And to optimize the distance in the gate component in overall architecture. To estimate the error analysis process in the k-best algorithm for two-way sorting method and to optimize the processing time and to increase the speed. This method to modify the sorting unit based on the VLSI architecture and to enhance the system performance. And mainly focused by architecture optimization level and to implement the optimize the child process in sorting tree architecture. This will result in minimum area and power. And operate in high frequency rating. To reduce the circuit complexity compare to the existing architecture. This will result in minimum area and power

IV. PROPOSED ARCHITECTURE

The proposed architecture for mimo detector. It shows the number of gates, flipflops, multiplexers used in our design. The number of gates is considerably reduced by the efficient implementation of mimo detector by VLSI technique. In proposed novel error –resilient k- best mimo detector to design the efficient architecture to modify the input preprocessor module and parameter calculation blocks by using the two way sorting methodology

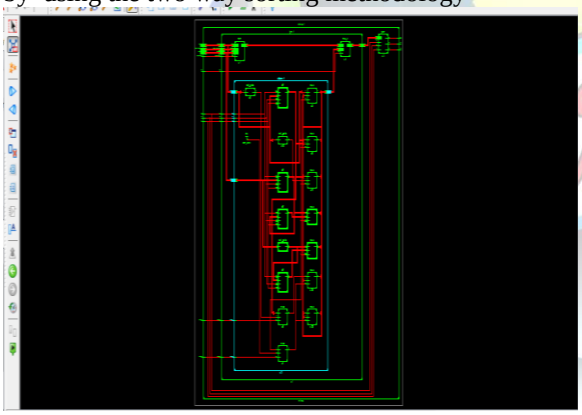

Fig. 5 RTL schematic of NSTPC

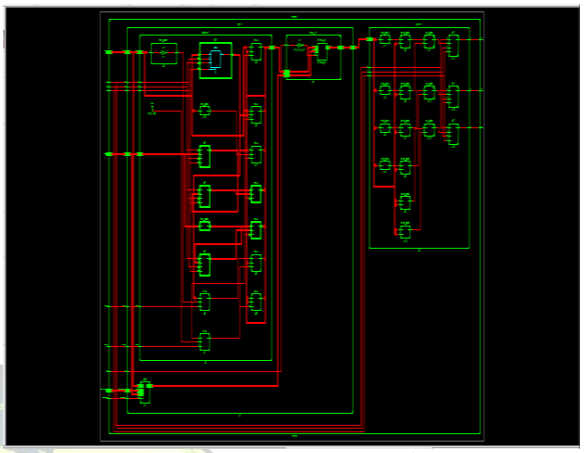

Fig. 6 RTL schematic of STPC

IV. RESULTS

A. *Simulation Result*

The number of slices utilized by this design on Spartran-3E are 13 out of 1920 which is considerably very economical and area saving. The number of bonded IOB's is 50 out of 66 available resources which also is very convenient.

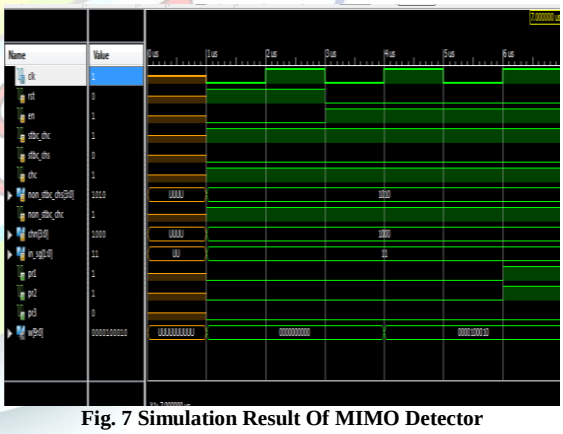

Fig. 7 Simulation Result Of MIMO Detector

B. *Synthesis Result*

The receiver blocks are implemented on one of Xilinx's Spartan 3E FPGAs. Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE 14.2i. In synthesis process, the RTL model will be converted to the gate level netlist mapped to a specific technology library. This modified turbo decoder design is implemented on FPGA (Field Programmable Gate Array) family of Spartan3E. Here in this Spartan3E family many different devices were available in the Xilinx ISE tool. In

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 4, December 2014

order to implement this MIMO detector, the device named as "XC3S500E" has been chosen and the package as "FT256" with the device speed as "– 4". The design of MIMO detector for low power and high speed is synthesized successfully and its results are analyzed. After completion of synthesize, the entire circuit model is processed through Translate, Map, Place and Route successfully.

The design of k-best MIMO detector architecture and compare the conventional detector to improve the speed and reduce the delay

Table 1.1 Comparison Table for Proposed and Conventional MIMO Detector

PARAMETER	CONVENTIONAL k-best MIMO detector	PROPOSED k-best MIMO detector
MEMORY REQUIRED(KB)	417KB	148KB
CLOCK FREQUENCY(MHz)	671MHZ	730.14MHZ
DELAY(ns)	2.785ns	1.370ns

V. CONCLUSION

To design MIMO detector architecture and to modify the conventional based MIMO architecture. This architecture to reduce the delay time and to improve the system performance. This architecture increases the speed for the signal processing architecture. The MIMO detector architecture to reduce the running time for required detecting process for the any data transmission processing applications. This proposed architecture using the two way sorting methodology. This methodology to reduce the time consumption level compare to the existing methodology. This proposed system to improve the system performance and efficiency level also. The implementation of the MIMO detector architecture is carried by Verilog HDL programming and synthesized in Spartan 3E using Xilinx ISI 14.2i .The device utilization of MIMO detector architecture is compared in terms of synthesis and implementation.

In future work to optimize the circuit complexity using the hierarchal based MIMO detector architecture. This technique to improve the system performance level compare to the proposed methodology. This method to reduce the power consumption level and to increase the system speed also. This method mainly focused by the circuit optimization process. This hierarchal based architecture to improve the MIMO detector efficiency level.

REFERENCES

[1]. D. Gesbert, M. Shafi, D.-S. Shiu, P. J. Smith, and A. Naguib, " Fromtheory to practice: An overview of MIMO space-time coded wirelesssystems," *IEEE J. Sel. Areas Commun., vol. 21, no. 3, pp. 281302,Apr. 2003.*

[2]. J.M. Rabaey, A. P. Chandrakasan, and B. Nikolic, Digital IntegratedCircuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ,USA: Pearson Education, 2001.

[3]. A.P.Chandrakasan, and B. Nikolic, Digital IntegratedCircuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ,USA: Pearson Education, 2003.

[4]. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of failureprobability and statistical design of sram array for yield enhancementin nano-scaled cmos*," IEEE Trans. Comput.-Aided Design Integr. CircuitsSyst.*, vol. 24, no. 12, pp. 1859–1880, Dec. 2005.

[5]. S. Li, J. H. Ahn, R. D. Strong, J. B. Brockman, D.M. Tullsen, and N.P. Jouppi, "McPAT: An integrated power, area, and timing modelingframework for multicore and manycore architectures," in Proc. Annu.IEEE/ACM Int. Symp. Microarchit., Dec. 12–16, 2009, pp. 469, 480.

[6]. Novak, C. Studer, A. Burg, and G. Matz, "The effect of unreliableLLR storage on the performance of MIMO-BICM," in Proc. AsilomarConf Signals, Syst., Comput. (ASILOMAR), 2010, pp. 736–740.

[7]. VLSI implementation of MIMO detection using the spheredecoding," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1566–1577, Jul. 2005.

[8]. Yang and D.Markovic, "A flexible DSP architecture for MIMO sphere decoding," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp.2301–2314, Oct. 2009.

[9]. S. Li, J. H. Ahn, R. D. Strong, J. B. Brockman, D.M. Tullsen, and N.P. Jouppi, "McPAT: An integrated power, area, and timing modelingframework for multicore and manycore architectures," in *Proc. Annu.IEEE/ACM Int. Symp. Microarchit.*, Dec. 12–16, 2009, pp. 469, 480.

[10]. M. Alioto, L. Giancane, G. Scotti, and A. Trifiletti, "Leakage poweranalysis attacks: A novel class of attacks to nanometer cryptographiccircuits," *IEEE Trans. Circuits.*