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# Reduction of Congestion in 3D NOC Using PCAR

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**Abstract**—Network on chip (NOC) systems can perform better performance than SOC for chip microprocessor systems.When more than one processor transmits its data to a same node there is a possible of occurrence of congestion in the path of transmission. In order to avoid this condition, Path Congestion Aware Adaptive Routing Algorithm is being used here.FSM (Finite State Machine) memory controller will switch data to the other nodes or processor where the transmission path is free of traffic or congestion. The processors which are frequently used will be placed in TRB(Thread Row Buffer) and hence we can directly fetch the processor from TRB, instead of going to memory.

**Index terms—**Network on chip, Path Congestion Aware Adaptive Routing, Finite State Machine, Thread Row Buffer.