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RANDOM TEST PATTERN GENERATION FOR HIGH FAULT COVERAGE USING BIST SCHEME

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***Abstract*-A Test Pattern Generator (TPG) is used for generate special test patterns in Built-In Self-Test (BIST) schemes. This work generate Multiple Single Input Change (MSIC) vectors in a sample, applies each vector to a scan chain is an SIC vector. A MSIC-TPG and squirrel based TPG are designed and residential a reconfigurable Johnson counter and a scalable SIC counter to generate a class of minimum move sequences. The Test Pattern Generator is flexible to both the test-per-clock and the test per-scan schemes. A theory is also urbanized to symbolize and investigate the sequences and to pull out a class of MSIC cycle. investigation results show that the bent Multiple Single Input Change sequences have the approving features of uniform delivery and low input shift density. It also achieve the target slip treatment without increasing the test length. The style modify scan-path structure, and let the Circuit under Test (CUT) inputs wait untouched during a shift function. Compared with the MSIC-TPG, the proposed miser based TPG achieve abridged region and average control spending through scan base test and the peak rule in the CUT. By writing VHDL code, the test pattern are virtual using MODELSIM and the outcome are validate.**

Key Words— Built-in self-test (BIST), low power, Multiple single-input change (MSIC), Test Pattern Generator (TPG).

I.INTRODUCTION

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT). The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compacts and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit.A digital system is tested and diagnosed during its lifetime on numerous occasions. Such a test and diagnosisshould be quick and have very high fault coverage. One way to ensure this is to specify such a testing to as one of the system functions, so now it is called Built Sin Self Test (BIST). With properly designed BIST, the cost of added test hardware will be more than balanced by the benefits in terms of reliability and reduced maintenance cost. For BIST, we would require that the test patterns be generated on the system/chip itself. However, this should be done keeping in mind that the additional hardware is minimized. One extreme is to use exhaustive testing using a counter and storing the results for each fault simulation at a place on the chip (like ROM). Christo Ananth et al. [7] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S-Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message. The weights are dynamically adjusted during the course of the test to "go after" the remaining untested faults. An accumulator-based 3- weight test pattern generation scheme is presented; the 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of built in self test pattern generation, as well. Comparisons with previously presented schemes indicate that the proposed scheme compares favorably with respect to the required hardware. A new design methodology for a pattern generator, formulated in the context of on-chip BIST. The

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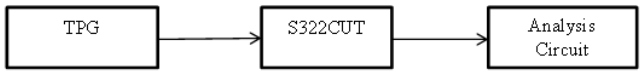
design methodology is circuit-specific and uses synthesis techniques to design BIST generators. The pattern generator consists of two components: a pseudorandom pattern generator like an LFSR and a combinational logic to map the outputs of the pseudorandom pattern generator. This combinational logic is synthesized to produce a given set of target patterns by mapping the outputs of the pseudorandom pattern generator.

II.METHODOLOGY

Existing Method

A new weighted random pattern design for testability is described where the shift register latch is distributed throughout the chip are modified so that they can generate biased pseudo-random patterns upon demand. A two-bit code is transmitted to each weighted random pattern shift register latch to determine its specific weight. The weighted random pattern test is then divided into groups, where each group is activated with a different set of weights. The weights are dynamically adjusted during the course of the test to "go after" the remaining untested faults.



An accumulator-based 3-weight test pattern generation scheme is presented. The proposed scheme generates set of patterns with weights 0, 0.5, and 1. Since accumulators are commonly found in current VLSI chips, this scheme can be efficiently utilized to drive down the hardware of built in self test pattern generation, as well.

Current System

1. The input from the clock is given to the Johnson counter.
2. The input of Johnson counter is in bit wise , so we have to generate the bit in the form of pattern.
3. The TPG (Test Pattern Generator) is used to generate the bit in the form of pattern so the input from the Johnson counter is given to the test pattern generator.
4. Then the output from the pattern generator is given to the multiple input signature register (MISR) to store the pattern to reduce the number of transition .
5. The output from the MISR is given to the Circuit Under Test (CUT) to check the given input and stored output are equal , if the input are equal then the circuit are considered as not a fault circuit .
6. If the given output are not equal then it is considered as a fault circuit.

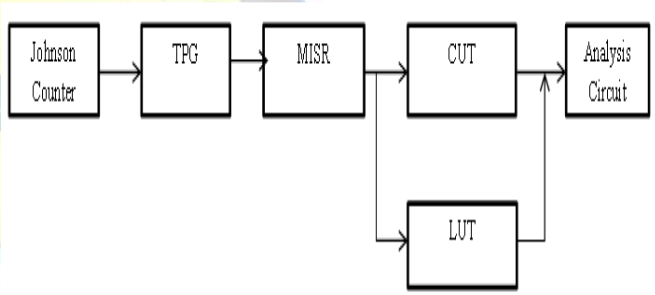


Fig..Block Diagram

MISR

BIST requires ability to capture the test results without the need for an external tester. This is often achieved by using a multi input signature register (MISR) to capture individual test results and compress these into an overall value called the test signature. A MISR is quite similar to an in-tapping LFSR, it consists of *n* memory cells (*M*1…*Mn*) with linear feedbacks from cell *Mn* (n is the number of output of the CUT).Like the LFSR, the MISR can be characterized by the polynomial given . Given theCharacteristic Polynomial and the initial state of the MISR, every cycle, the MISR will generate a new state, based on the current state, the Characteristic Polynomial and the response of the CUT. The state of the MISR is referred to as the *signature*. Given the

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initial state, the Characteristic Polynomial and the set of responses from the CUT to a given test, the signature of the MISR is determined after the complete test can be determined. This signature is compared to the signature of a simulated fault-free circuit. When these signatures do not match, the CUT is not fault-free.

TPG

Several methods to perform automatic test generation have beenproposed. They can be classified in two categories : the synthetic methods and the analytic methods. ;Synthetic methods are based upon the checking of the state-tables of the networks and of the transitions from state to state. The most well known are the Hennie 2 and Poage 3 methods. These methods are well adapted to small networks but, in general, are heuristic in nature and are much harder to implement than the analytic methods.The most commonly used analytic methods are the pathsensitizing, pseudo-random, D-algorithm, manual patterns, and methodsdirectly derived from the above. Pseudo-random pattern generation isfast and economic but has severe limitations with high fan-incircuits. The path sensitizing method implies the use of algorithmsand of heuristics. But it cannot detect faults which re~uire tosensitize several paths at a time. The D-algorithm may beconsidered to be a formalized version of the path sensitizing methodwith the added intelligence necessary to sensitize multiple paths.In a test generation system, these methods are exercised concurrently for a given network to achieve a sufficient testcoverage.

LUT

A look-up table (LUT) is a mechanism used to transform a range of input colours into anotherrange of colours. It can be a hardware device built into an imaging system or a software function built into an imageprocessing application. The hardware colour look-up table will convert the logical colour (pseudo-colour) numbers stored in each pixel of videomemory into physical colours, normally represented as RGBtriplets, that can be displayed on a computer monitor. The palette is simply a block of fast RAM which is addressed by the logical colour and whose output is split into the red, green, and blue levels which drive the actual display.

A LUT is characterized by:

- The number of entries in the palette: determines the maximum number of colours which can appear on screen simultaneously (a subset of the wider *full palette*, which is to be understood as the total number of colours that a given system is able to generate or manage.

- The width of each entry in the palette: determines the number of colours which the wider full palette can represent.

FAULT DETECTION

Fault detection, isolation, and recovery (FDIR) is a subfield of control engineering which concerns itself with monitoring a system, identifying when a faulthas occurred, and pinpointing the type of fault and its location. Two approaches can be distinguished: A direct pattern recognition of sensor readings that indicate a fault and an analysis of the discrepancy between the sensor readings and expected values, derived from some model. In the latter case, it is typical that a fault is said to be detected if the discrepancy or *residual* goes above a certain threshold. It is then the task of fault isolation to categorize the type of fault and its location in the machinery. Fault detection and isolation (FDI) techniques can be broadly classified into two categories. These include Model-based FDI and Signal processing based FDI.

JOHNSON COUNTER

A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. The MOD of the Johnson counter is 2n if n flip-flops are used. The main advantage of the Johnson counter is

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that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD.

III. Simulation Result

A. Simulation Result for Accumulator cell Configurations

The waveform of Accumulator cell‟s configurations is shown in the fig 8. The configuration (a) that drives the CUT inputs when A=‟1‟ is required. Set[i] = „1‟ and reset[i] =‟0‟ and hence A=‟1‟ and B=‟0‟. Then the output is equal to „1‟, and Cin is transferred to Cout.

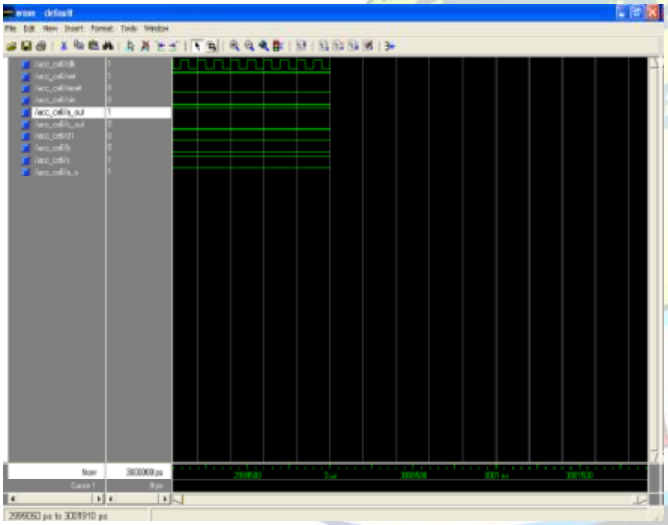

Fig. Waveform for the configuration of set=‟1‟ and reset=‟0‟

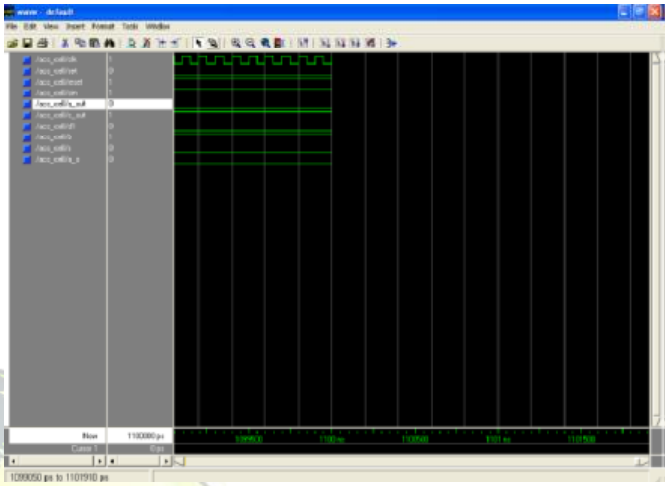

Fig. waveform of the configuration of set=‟0‟ and reset=‟1‟

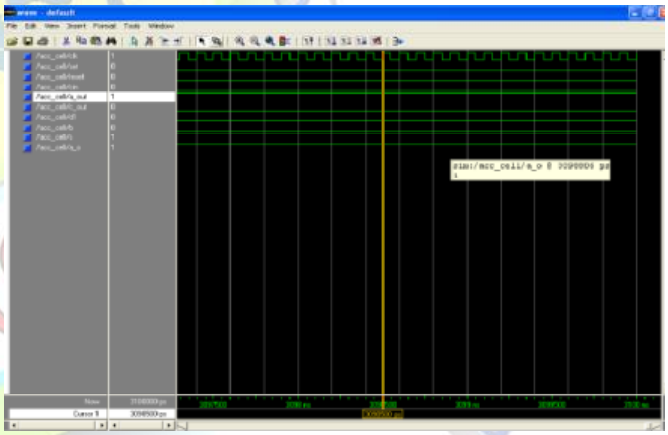

Fig. Waveform of the configuration of set=‟0‟ and reset=‟0‟

B. *Simulation Result for Test Vector Generation for Fault Coverage*

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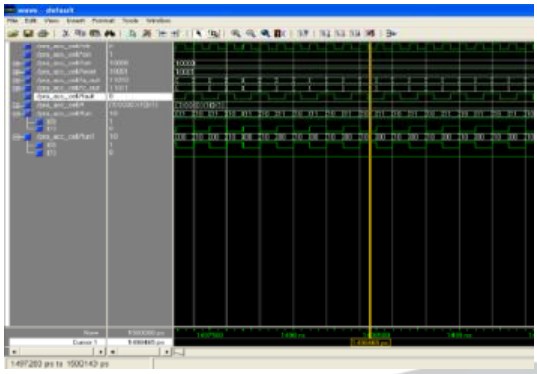
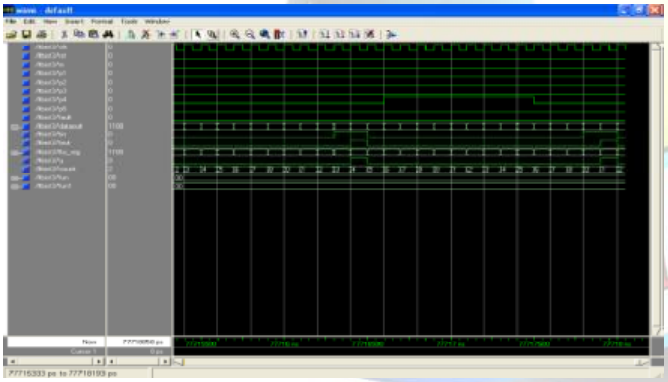


Fig. Output Waveform For Benchmark Circuit Using Accumulator

Cell

C. *Simulation Result for LT-RTPG*

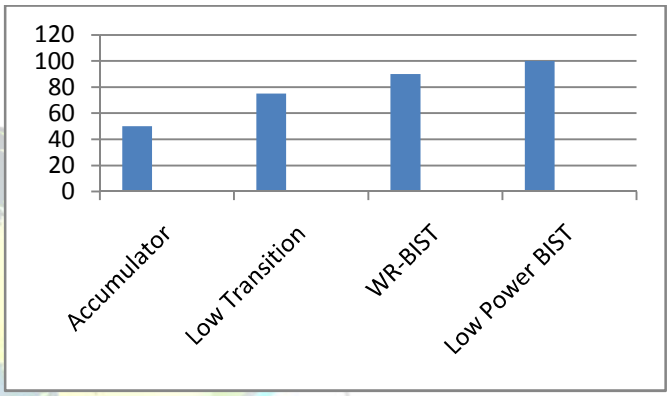


IV.Power Table

POWER AND FAULT CALCULATION

Series	Accumulator	Low Transition BIST	Weighted Transition BIST	Low Power BIST
Power[w]	0.08	0.025	0.024	0.020
Fault Coverage	50	75	90	100
%				

Power and Fault Comparison Chart



Advantages

1. Easily we can identify the fault, where it occurs.
2. Reduce the amount of power consumption and the transition level.

Conclusion

This project presents a low hardware overhead TPG for scan based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with an arguable length of test sequence. The test patterns are engender by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random pattern resistant faults (RPRFs)

only with (pseudo) random patterns generated by an LFSR often require unforeseeable long test Sequences thereby
resulting in prohibitively long test time. The proposed TPG 3-weight BIST reduces switching activities in the circuits, so that the number of transitions will be debase an d less power will be consume.

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