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Design of low power-High Speed CSLA by using Data Gathering Technique

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Abstract – The overture of the work principally focused on Carry select adder. Because of complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system, the FCSA done this work. The logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter(BEC)-based CSLA are analyzed to study the data dependenceand to identify redundant logic operations. Modified GDI logic architecture concentrating on the area level &fast carry selections. The fixed Carry Selections of different stage parallel Adder i.e (Carry in=0,1) is directly based on the GDI technique. This concept provides less area and low delay than previous SQRT-BEC CSLA.

Keywords-DSP,SQRT,BEC,FCSA,CSLA.

I INTRODUCTIONS

The integrated circuits mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized ICs in place of designs using discrete transistors. Here the hot spot is combinational circuit, so the basic portion of the combinational circuit is Adder.A complex digital signal processing (DSP) system involves several adders. A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder. Carry look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders.[1],[2].

Low power, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation [2][3].A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses a dual RCA. Few attempts have been made to avoid dual use of RCA in CSLA design.

A ripple carry adder uses a simple design, but carry propagation delay (CPD) is the main concern in this adder. A conventional carry select adder (CSLA) is an RCA–RCA configuration that generates a pair of sum words and output carry bits corresponding the anticipated input-carry (cin =0 and 1) and selects one out of each pair for final-sum and final-output-carry.

In the previous methods of adder designs, logic is optimized without giving any consideration to the data dependence [1]. In this proposal, we made an analysis on logic operations involved in conventional and BEC-based CSLAs with GDI based Carry selections to study the data dependence and to identify redundant logic operations.

As well as based on this analysis, we have proposed a logic formulation for the GDI CSLA. The main contribution main motto is the logic formulation based on data dependence and optimized carry generator (CG) and CS design. Based on the proposed logic formulation, we have derived an efficient logic design for CSLA. Due to optimized logic units, the proposed CSLA involves significantly less ADP than the existing BEC-CSLAs. We have shown that the GDI based SQRT-CSLA using the proposed CSLA design involves nearly 45% less ADP and consumes 40% less energy than that of the corresponding SQRT-CSLA. Christo Ananth et al. [9] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the

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delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

II FUNCTIONAL FORMULATION

In this section we concentrate the overall functional logic formulations method. The GDI concept is taken from the Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit[4] by Partha Bhattacharyya.

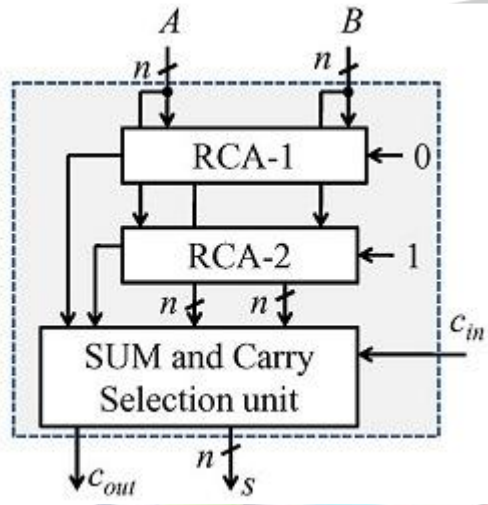

Figure 1:Basic structure of CSLA

The CSLA is originally started in RCA[5].The main objective of this study is to identify redundant logic operations and data dependence.

In a SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide a parallel path for carry propagation that helps to reduce the overall adder delay.

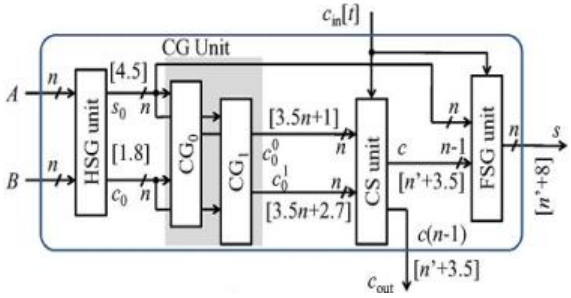

Figure 2: BEC-SQRT structure CSLA

The figure 2 indimate the final sturcutre of SQRT-BEC CSLA[1].which provide less delay (apprx 33%)than previous convolutions based CSLA.The carry selection formula is based on the below eqn due to get low propagations delay.

S1[0]=~s[0] (1)

C1[0]=s[0] (2)

S1[i]=s[i-2]^c[i-1] (3)

C1[i]=s[i-2]&c[i] (4)

The S1[0]=~s[0] describes the sum selcetions of 2nd stage adder. Furtherly C1[0]=s[0] shows the carry selections of second stage carry selections unit.S1[i],C1[i]vice versa..Where i is the number of digits in the adder desgn.

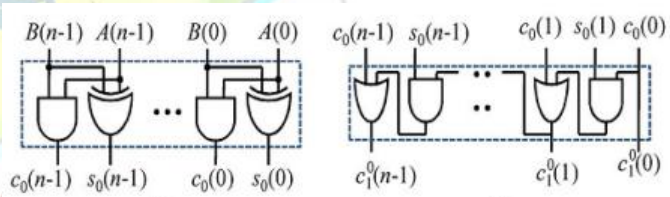

figure 3:AND and OR gate based Adder design.

The figure 3 shows the N number of bit adder design ,this sturcture is taken from the fast CSLA adder[4].

It the CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n-bit operands (A and B) and generate half-sum word s0 and half-carry word c0 of width n bits each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generate two n-bit full carry words c01 and c1 1 corresponding to input-carry '0' and '1', respectively.

Due to early generation of output-carry with multipath carry propagation feature, the CSLA design is more favorable than the existing CSLA designs for area–delay efficient implementation of SQRT-CSLA.To do design an efficient CSLA by using optimized logic units. The proposing CSLAdesign involves significantly less area and delay than the recentlyproposed BEC-based CSLA.

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The proposed method would be initiate the GDI(Gate Diffusion Input) Technique, and it will be Modify for getting suitable low power digital circuits design further to reduce the swing degradation problem. This techniques allows reduction in power consumption, carry propagation delay and transistor count of the carry select adder too.

An adder is the main component of an arithmetic unit. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system[7].

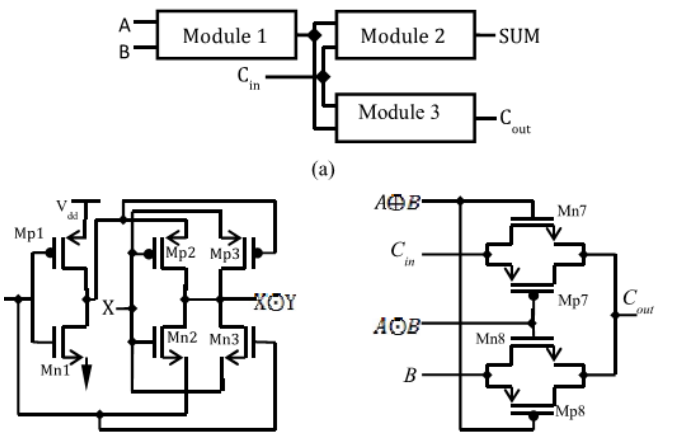

Figure 4: The single bit full adder desing module by using GDI

The figure 4 clearly explain the transitor selections of single bit full adder circuit by using GDI technique[2].from this concept we have to think how about multi bit adder circuit,how to reduce area and dely finally we proved this design is well suited for high speed multiplier design.as well as low area multi bit full adder design.For this design we had chosen Tanner 13 tool initially next xilinix.

The basic Gate Diffusion Input (GDI) logic style suffers from some of the practical limitations like swing degradation, fabrication complexity and bulk connections. These limitations can be overcomes by modified gate diffusion input (Mod-GDI) logic[2]. This modified gate diffusion input (Mod-GDI) logic allows reduction in power consumption, delay and area of digital circuits.

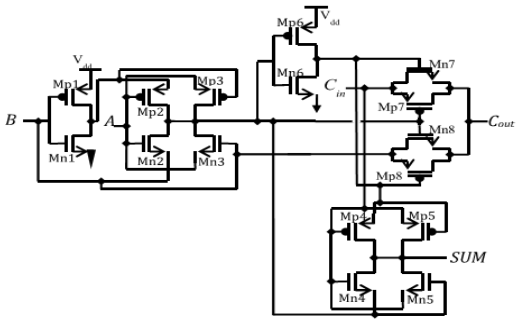

Figure 5:full adder sum and carry selections based on modified GDI Technique

T his arrangement of modified GDI cell provides reduction in both sub threshold and leakage power compared to static CMOS gate. Mod-GDI is more suitable while designing of high speed, low power circuits by using reduced number of transistors as well as improved swing degradation and static power characteristics. This logic allows simple top-down design by using a small cell library . Mod GDI logic performance is testable, so that Mod-GDI logic and logic circuit design methods is hopeful for design a low power and high performance applications.

Various logic function implementation with Mod-GDI logic:

S_N	S_P	G	P	N	D	FUNCTION
0	1	A	1	0	A'	INVERTER
A	A	B	0	A	AB	AND
0	D	B	A	1	A+B	OR
0	A	B	A	A'	A'B+AB'	XOR
0	A	B	A'	A	AB+A'B'	XNOR
0	1	A	B	C	A'B+AC	MUX

Table 1:Mod-GDI based bit selections which is taken from[2].By using this table we have to formulate the worthfull

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equations for Fast Carry Selection Adder(FCSLA).which is describes below.

```
if(c[0]&&c[1] )
        fastcla[0]=1'b1;
        else
        fastcla[0]=1'b0;

 if(c[1]&&c[2] )
        fastcla[1]=1'b1;
        else
        fastcla[1]=1'b0; vice versa…..
```

The logical Equations is design and simulate by using Xilinix 14.7v ,the synthesis and simulations result is described by below sections.

III SYNTHESIS AND SIMULATIONS RESULTS

The simulation and synthesis work is finally done by the xilinix and modelsim.initially the desing is done by the tanner.

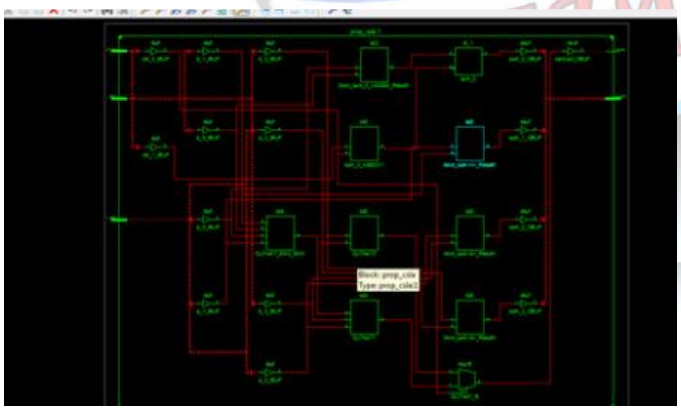

Figure 6:synthesis results of BEC-SQRT design.

The figures intimate the BEC-SQRT proposed carry select adder,which is compined form of conventional and binary to excess code conversion method.by this work we confirmed the over all area of the adder is reduced by comparing previous method .The area related to delay of both logic and routing also reduced .We got this result by analysing Look Up Table of this design.the result I which we got is below.

Total delay 7.716ns (6.219ns logic, 1.497ns route)

(80.6% logic, 19.4% route)

Carry selections delay 4.368ns (3.948ns logic, 0.420ns route)

(90.4% logic, 9.6% route)

From the SAED 90nm technology Cell library data sheet the area,delay of the OR,NOT,AND gates[1] are is below.

	AND-gate	OR-gate	NOT-gate
Area (um^2)	7.37	7.37	6.45
Delay (ps)	180	170	100

The use of less number of transistors in this GDI concept also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid FCSLA is significantly improved in comparison with the earlier hybrid adders.

Figure 7:synthesis diagram of FCSLA

The figure 7 is desinged by using verilog language with xilinix synthesis tool.for this design we had to use 16 bit carry select adder.with GDI Concept.

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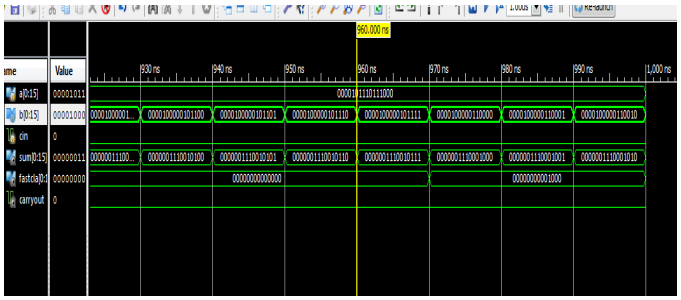

Figure 8: simulations result of FCSLA

The figure 8 shows the simulations result of the FCSLA,which is checked by the random test bench code in xilinix tool.here we have to reduce almost best case redundancy minimizations.the wave form is indicate the flag register for intimate the final bit(0,1)of every sum,because of Ex-OR gate is enable if odd number of one is there.The final delay and area of the FCSLA is below.

```
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: 2.852ns
   Maximum output required time after clock: 4.368ns
   Maximum combinational path delay: 6.320ns
```

Figure 9:snap of compinational path delay from the xilinix

The wired delay also reduced by perfect RTL coding,here we never allowed the latch forming that's why we achieved less combinational delay i.e 6.320ns.

IV.CONCLUSION

From the analysis of various CSLA finally we had to choosed BEC-CSLA with SQRT technology for high speed Carry selections and modified this concept with GDI technology and we had achieved less area and low delay compare than BEC-CSLA,but we could'nt solve the power reuctions.i.e we have same amount of power consumption as SQRT-BEC CSLA.The originality of the simulations and synthesis work also we had designed and analysied.The reudundancy bit reduced almost 100%.we had analyzised logic formulations involved in SQRT-BEC CSLA.for the indivitual carry selcetions the GDI based design is used.

V.REFERENCE

[1] "Area–Delay–Power Efficient Carry-Select Adder" Basant Kumar Mohanty, *Senior Member, IEEE*, and Sujit Kumar Patel.

[2] "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit" Partha Bhattacharyya, *Senior Member, IEEE*.

[3] "Ultralow-power electronics for biomedical applications,"A. P. Chandrakasan, N. Verma, and D. C. Daly *Annu. Rev. Biomed. Eng.*, Aug. 2008.

[4] "Revised Carry-select adder," O. J. Bedrij Jun. 1998.

[5] "64-bit carry-select adder with reduced area," Y. Kim and L.-S. Kim, May 2001.

[6] , "An area-efficient 64-bit square root carryselect adder for low power application"Y. He, C. H. *Syst.*, 2005.

[7] "ULPFA: A new efficient design of a power-aware full adder," I. Hassoune, D. Flandre, I. Aug. 2010.

[8] "Architecture of adders based on speed, area and power dissipation,"P. Prashanth Dec. 2011.

[9] Christo Ananth, H.Anusuya Baby, "Encryption and Decryption in Complex Parallelism", International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), Volume 3, Issue 3, March 2014,pp 790-795

[10] "An efficient SQRT architecture of carry select adder design by common Boolean logic," S. Manju *VLSI ICEVENT*, 2013.