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Design of Pulse-Triggered Flip-Flop using Signal Feed Through Scheme for Low-Power Consumption

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Abstract: InthisPaper, Pulse-triggered FF (P-FF) isa single-latchstructurewhichismorepopularthan the conventionaltransmissiongate (TG)andmaster–slave based FFs in high-speed applications are presented. Besidesthespeedadvantage,itscircuitsimplicitylowers thepowerconsumptionoftheclock treesystem.Thelow- power flip-flop (FF) design featuring an explicit type pulse-triggeredstructureanda modifiedtruesinglephase clock latchbasedonasignalfeed-throughschemeis presented. The proposed design successfully solves the long discharging path problem in conventional explicit typepulse-triggeredFF(P-FF)designsand achievesbetter speed andpowerperformance.Basedonpost-layout simulationresultsusingTSMCCMOS90-nm technology, theproposed designoutperforms theconventional P-FF design byusing only17transistors. Theaverage power delayisreducedto 3.57µW.Inthemeantime,the performance edges onpower andpower- delay-product metricsare22.7% and29.7% ,respectively.

Keywords: Flip-flop,Transmissiongate, Signal feed throughscheme,Designmethodology.

I. INTRODUCTION

Low powerhasemergedasaprincipaltheme intoday'selectronicsindustry.The needforlowpower has causedamajorparadigmshiftwherepower dissipation hasbecomeasimportantaconsiderationas performanceandarea.SothisLow PowerPulse TriggeredFlipFlop reviewsvarious strategiesand high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and methodologiesfordesigninglow powercircuitsand systems.Itdescribesthemanyissuesfacingdesignersat architectural, logic, circuit and device levels and presents some of the techniques that have been proposedtoovercomethesedifficulties.The article concludeswiththefuture challengesthatmustbe metto designlowpower,highperformancesystems.

Flip-flops(FFs)are thebasicstorageelements usedextensively inallkindsofdigitaldesigns.In particular,digitaldesignsnow a-daysoftenadopt intensivepipeliningtechniquesandemploy many FF-richmodulessuchasregisterfile,shift register,andfirst

Infirstout.It isalsoestimatedthat thepower consumption of the clock system, which consists of clockdistributionnetworksandstorageelements,isaspowercon sumptiontotheoverallsystemdesign.

AP-FFconsistsof apulsegeneratorforstrobe signalsanda latch for data storage. Ifthetriggering pulses are sufficiently narrow, the latch acts like an edge-triggeredFF.Sinceonlyonelatch,asopposedto twointhe conventionalmaster–slaveconfiguration,is needed,aP-FFissimpler in circuitcomplexity. This leadstoa highertoggleratefor high-speedoperations.P- FFsalso allow timeborrowingacrossclockcycle boundariesandfeature azeroor even negative setup time. Despite these advantages, pulse generation circuitryrequiresdelicatepulsewidth control tocope withpossiblevariationsinprocesstechnologyandsignal

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distributionnetwork.Inastatisticaldesignframe work is developed to takethesefactorsinto account.To obtain balancedperformanceamong power,delay,and area, designspaceexplorationisalsoawidelyusedtechnique.

Inthisbrief,wepresenta novellow-powerP- FF designbasedonasignalfeed-throughscheme. Observingthedelaydiscrepancyinlatchingdata1and 0,the design manages to shorten the longer delayby feedingtheinputsignaldirectlytoaninternalnodeof thelatch design tospeedupthedatatransition.This mechanismisimplementedby introducingasimplepass transistorforextrasignal driving. Whencombined with the pulse generation circuitry, it forms a new P-FF designwithenhancedspeed and power-delay-product (PDP)performances.

II.RELATEDWORK

.AReducedClock-SwingFlip-Flop(RCSFF) is proposed,whichcanreducetheclockingsystempower of anVLSIdownto1/3comparedtotheconventional Flip-Flop.TheareaandthedelayoftheRCSFFcanalso bereducedbyafactorofabout20%. Transistorcount of theRCSFFis20includingan inverter for generating whilethatoftheconventionalFlip-Flop is24.[1]

Certainmisleadingparameters havebeen properly modifiedandweightedtoreflectthereal propertiesof thecomparedstructures.Furthermore,the results of thecomparisonofrepresentativemaster–slave latches and flip-flops illustrate theadvantages of our approachandthesuitabilityof differentdesignstylesfor high-performanceandlow-powerapplications.[2] Conditional-Capture Flip-Flopdescribesa family ofnovellow-powerflip-flops,collectivelycalled conditional-captureflip-flops(CCFFs).Theseflip-flops also havenegativesetuptimeandthusprovidesmall data-to-outputlatencyandattributeofsoft-clockedge forovercoming clockskew-relatedcycletimeloss[3].

Anovellow-power pulse-triggeredflip-flop (FF)designispresented[3].First, thepulse generation controllogic,anAND function, isremovedfromthe criticalpathto facilitateafasterdischargeoperation.A simpletwo-transistorANDgatedesignisusedtoreduce the circuitcomplexity.Second,aconditionalpulse-enhancementtechnique is devisedtospeedupthe dischargealongthe criticalpathonly whenneeded[4].

The pulse generationcontrollogicanAND function,is removedfromcriticalpathtofacilitatea faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second,a conditional pulse-enhancement technique is devisedtospeedupthe discharge alongthe criticalpathonlywhenneeded.As aresult, transistor sizesindelayinverterandpulse-generationcircuitcan bereducedforsaving[5].

III.CONVENTIONALP-FFDESIGNS

PF-FFs,intermsof pulsegeneration,canbe classified as an implicit or an explicit type. In an implicittypeP-FF,thepulsegeneratorispartofthe latchdesignandno explicitpulsesignalsaregenerated. InanexplicittypeP-FF,thepulsegeneratorandthe latch areseparate . Without generating pulsesignals explicitly,implicittype P-FFs is ingeneral more power- economical.However,they sufferfromalonger dischargingpath,whichleadsto inferiortiming characteristics. Explicit pulse generation, on the contrary,incursmore powerconsumptionbutthelogic separationfromthe latchdesigngives the FF designa unique speedadvantage.Itspowerconsumptionandthe circuit complexity can be effectively reduced if one pulsegeneratorissharesagroupof FFs(e.g.,ann-bit register).Inthisbrief,wewillthusfocusonthe explicit typeP-FFdesignsonly.

A.*EP-DCO:explicit-Dataclosed tooutputFlip-Flop*

Toprovideacomparison,someexistingP-FFdesigns arereviewedfirst.Fig.3.1(a)shows aclassicexplicitP- FF design, nameddata-closet-to-output(ep-DCO).It contains a NAND-logic-based pulse generator and a semi dynamic true single-phase-clock (TSPC) structuredlatchdesign.InthisP FF design,invertersI3 andI4 areused to latchdata,andinverters I1 andI2are usedtoholdthe internalnodeX.The pulse widthis determinedbythedelayofthreeinverters.Thisdesign suffersfromaseriousdrawback,i.e.,the internalnodeX isdischargedoneveryrisingedgeoftheclockinspiteof thepresenceofastaticinput"1."Thisgivesrise tolarge switchingpowerdissipation.To overcomethisproblem, manyremedial measures such as conditional capture, conditionalprecharge,conditionaldischarge, and conditionalpulseenhancementscheme havebeen proposed.

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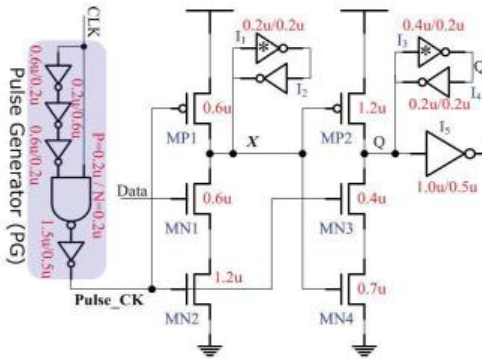

Fig.3.1(a)EP-DCO

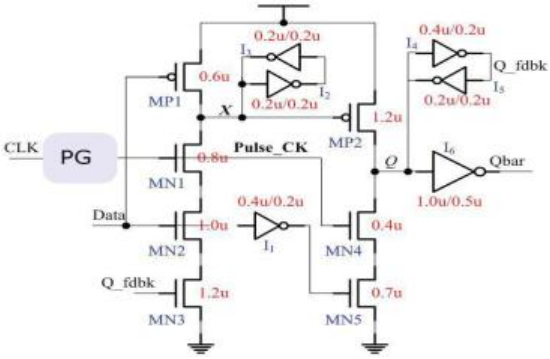

Fig.3.1(c)SCDFF

B.*CDFF:conditionaldischargedFlip-Flop*

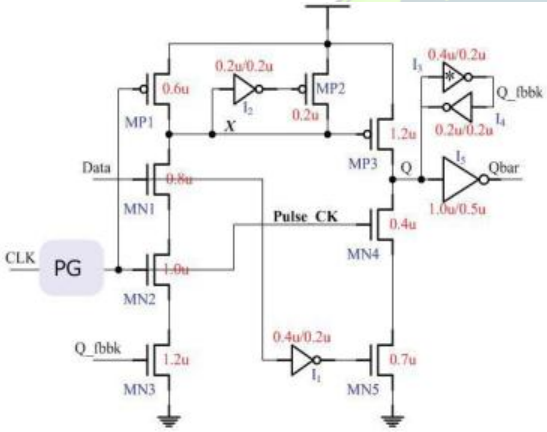

Fig.3.1(b)CDFF

Fig. 3.1(b) shows a conditional discharged (CD) technique.Anextra nMOS transistorMN3controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition,the keeperlogic forthe internalnodeXis simplified and consists of an inverter plus a pull-up pMOStransistoronly.C.*SCDFF:Static-conditionaldischargedFlip-Flop*

Fig. 3.1(c) shows a similar P-FF design (SCDFF)usingastaticconditionaldischargetechnique .ItdiffersfromtheCDFFdesigninusing astaticlatch structure.Node X isthusexemptedfromperiodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay thantheCDFFdesign.Bothdesignsfaceaworst casedelaycausedby adischargingpathconsistingof threestackedtransistors,i.e.,MN1–MN3.To overcome thisdelayforbetterspeedperformance,apowerfulpull-downcircuitryisneeded,whichcausesextra layoutarea andpowerconsumption.Themodified hybrid latchflip-flop(MHLFF).

D.*MHLFF:Modified hybridlatch flip flop*

Fig.3.1(d)also usesastaticlatch.The keeper logicatnodeX isremoved.Aweakpull-uptransistor MP1controlledbytheoutputsignalQmaintainsthe levelofnode XwhenQ equals0.Despite itscircuit simplicity, the MHLFF designen counters two drawbacks.First,sincenodeXis notpredischarged,a prolonged0to1delay isexpected.Thedelay deteriorates=further,becausea level-degradedclock pulse(deviatedbyoneVT)isappliedtothedischarging transistor MN3.Second,nodeXbecomesfloatingin certaincasesanditsvaluemay driftcausingextradc power.

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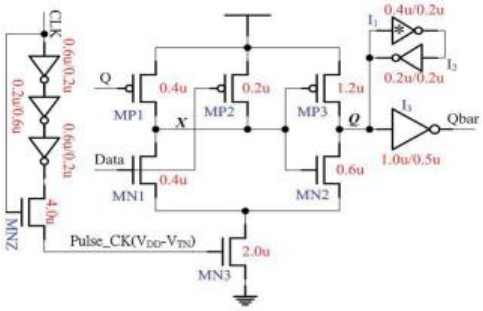

Fig.3.1(d)MHLFFI

V.PROPOSEDP-FFDESIGN

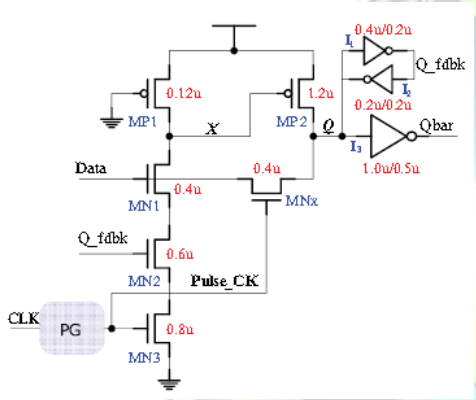

Fig.4.1proposedsignalfeedthroughP-FFdesign

Inthisbrief,wepresenta novellow-powerP-FFdesign basedonasignalfeed-throughscheme.Observing the delay discrepancy in latching data "1" and "0," the designmanagestoshortenthelongerdelaybyfeeding theinputsignaldirectly toaninternal nodeofthelatch designtospeedupthedata transition.This mechanismis implementedby introducingasimplepasstransistorfor extrasignaldriving.Whencombinedwiththe pulse generationcircuitry,itformsanew P-FFdesignwith enhancedspeed and power-delay-product(PDP) performances.

A. *SignalFeedThroughScheme*

The proposeddesignadoptsasignalfeed-throughtechniqueto improvethisdelay.Similarto the SCDFF design, the proposed design also employs a staticlatchstructureand aconditionaldischargescheme to avoidsuperfluous switchingataninternalnode. However,therearethreemajordifferencesthatleadto a unique TSPClatchstructureand maketheproposed designdistinctfromthepreviousone.

First,a weak pull-up pMOStransistor MP1 withgateconnectedtothegroundisusedinthefirst stageof theTSPClatch.This givesrisetoapseudo-nMOSlogicstyledesign,andthechargekeepercircuit fortheinternalnode*X*canbesaved.Inadditionto the circuitsimplicity, thisapproachalsoreducestheload capacitanceof node*X*.Second,apasstransistorMNx controlledbythepulseclockisincludedsothatinput datacandrivenodeQofthelatchdirectly (thesignal feed-throughscheme).Along withthepull-uptransistor MP2atthesecondstageinverterofthe TSPClatch,this extrapassagefacilitatesauxiliary signaldrivingfromthe input sourcetonode Q. Thenodelevel can thusbe quickly pulleduptoshortenthedatatransitiondelay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employedpasstransistorMNxprovidesadischarging path.

Table1.Comparisonofvarious P-FFdesigns

P-FF(Pulse TriggerflipFlop)	EPDCO	SCDFF	CDFF	MHLFF	ProposedP-FF
NO. OF TRANSISTORS	28	31	30	19	17
AVG. POWER (μW)	9.42	9.61	9.37	9.27	3.57
DELAY(ps)	1530	711.69	853.8	615	508

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Theroleplayedby MNxisthus twofold,i.e., providingextra drivingtonodeQduring0to1data transitions,anddischargingnode Qduring"1" to "0" datatransitions.Comparedwiththe latchstructureused inSCDFFdesign,thecircuitsavingsof theproposed designinclude achargekeeper(twoinverters),apull- down network(two nMOStransistors),andacontrol inverter. Theonlyextra component introduced isan nMOSpasstransistortosupportsignalfeedthrough. Thisschemeactually improvesthe"0"to"1"delayand thusreducesthedisparitybetweenthe risetimeandthe falltime delays.IncomparisonwithotherP-FF designs suchasep-DCO,CDFF,andSCDFF,the proposed designshows themostbalanceddelaybehaviors.

Theprinciplesof FFoperationsof the proposeddesignare explainedas follows.Whenaclock pulsearrives,ifno datatransitionoccurs,i.e.,theinput dataandnode Q areatthesamelevel,oncurrentpasses throughthe passtransistorMNx,whichkeepsthe input stageoftheFFfromanydrivingeffort.Atthesame time,the inputdataand13the outputfeedbackQ_fdbk assume complementarysignallevelsandthe pull-down pathofnode*X*isoff.Therefore,no signalswitching occursinanyinternalnodes.Ontheotherhand,ifa"0" to"1"datatransitionoccurs,node*X*isdischargedto turnontransistorMP2, whichthenpullsnode Qhigh.

V.SIMULATIONRESULTSANDDISCUSSION

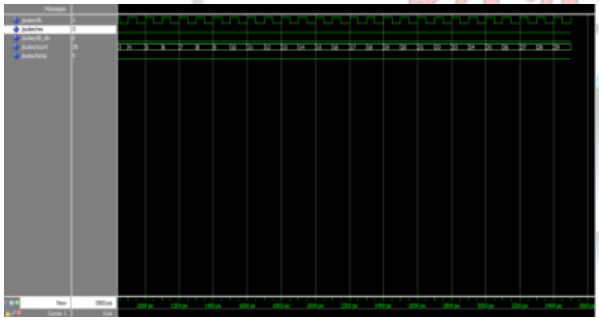

Fig5.1.SimulationResultsforPulsegenerator

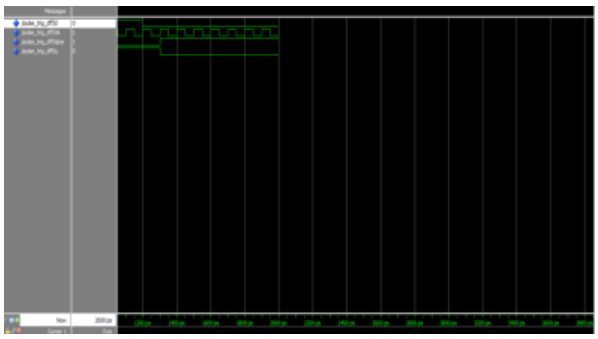

Fig.5.2 SimulationResultsfor P-FFDesign

TheabovecomparisontableshowsthattheFiveof them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% data transition probabilities,respectively.

VI.CONCLUSION

Inthisbrief,wepresenteda novelP-FFdesignby employingamodifiedD-FFstructure incorporatinga mixeddesignstyleconsistingof apasstransistoranda pseudo-nMOS logic. The key idea was to provide a signal feed through from input sourcetotheinternal nodeof thelatch,whichwouldfacilitateextradrivingto shortenthe transitiontimeandenhancebothpowerand speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensivesimulationswereconducted,andtheresults didsupporttheclaimsof theproposeddesigninvarious performanceaspects.

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