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Efficient Approach for Power Reduction by Using Multi-Bit Flip-Flops

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ABSTRACT

Power consumption plays a vital role in modern nanometer IC design. Clocking takes a foremost part of total chip power. Clock power can reduce by replacing a number of flip-flops with Multi-bit flip-flops. This paper proposes an efficient technique for designing a multi-bit flip-flop. It has main three approaches. First,identifying the mergable flip-flop. After identifying the mergeable flip-flops, the combination of flip-flop table provided by a library has been build. Finally the possible flip-flops can be merged. The performance has been compared with existing scheme and it can reduce the clock power.

II.INTRODUCTION

Power is the major consideration in modern VLSI Design. In recent past, low power consumption is attracted by many researchers. A large portion of total power dissipation in synchronous systems is due to the operation of flip-flops in clock network. In Fig.1 shows the power distributions in VLSI Product. Clock system and a logic part itself consume almost the same power in various chips, and the clock system consumes 20–45% of the total chip power. In this clock system power, 90% is consumed by flip-flops[1].The large power consumption of the clocking system is depends on two main reason. First one is switching activity of the clock is very high. Clock system is that the transition probability of the clock is 100% while that of the ordinary logic is about one-third on average. Second, the clock drives a large number of flip-flops. Advancedtechnology issued more and more components, it leads high power density.Reducing power consumption not only can enhance battery life and also avoid overheating problem.

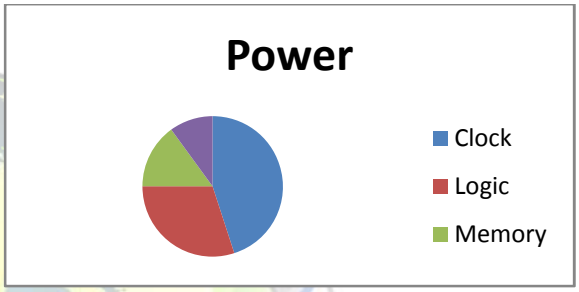

Fig 1: Power distribution Chart

In conventional synchronous designs, all one-bit flip-flops are considered as independent components. In the recent years, as the process technology advances, feature size of IC is shrank, the minimum size of clock drivers can trigger more than one flip-flop.Many kind of different power reduction methodologies have been proposed [5],[9]. Multi-bit flip-flop is an effective power-savingimplementation methodology by merging single-bit flip-flops in the design. Using multi-bit flip-flopscan reduce clock dynamic power and the total flip-floparea effectively. The locations of the cells have been determined by givendesign. The power consumed by clocking can be reduced further by replacing several flip-flops with multi-bit flip-flops. During clock tree synthesis, less number of flip-flops means less number of clock sinks. Clock sink is used to reduce delay on the clock network. Thus, the resulting clock network would have smaller power consumption and uses less routingresource. As the technology progresses, the driving capability of an inverter-based clock buffer increases significantly. The driving capability of a clock buffer can be evaluated by the number of minimum-sized inverters that it can drive on a given rising or falling time. Clocking power can be reduced by replacing several flip-flops with multi-bit flip-flops. If we replace the two 1-bit flip-flops as shown in Fig. 2(a) by the 2-bit flip-flop as shown in Fig.2(b), the total power consumption can be reduced because the two 1-bit flip-flops can share the same clock buffer to avoid the unnecessary power wastage. The clock signal can arrive at

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different components at different time. The above problem can be caused by many different things such as wire-interconnect length, temperature variation in intermediate devices, material imperfects and different input capacitance on clock input. The problem of clock skew can be reduced and enable the signals for a group of flip-flops by using common clock buffer

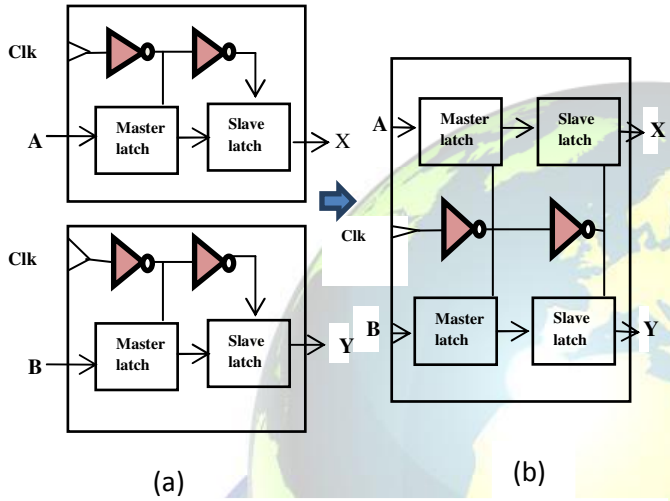

Fig 2 (a).Two 1-bit flip-flops (before merging) (b).2-bit flip-flop (after merging)

III. LITERATURE SURVEY

A. *Clock swing*

In order to reduce the clock system power, it is effective to reduce a clock voltage swing [5].This is because the power consumption of the clock system is proportional either to the clock swing or to the square of the clock swing, depending on the circuit configuration.Power distribution of VLSI's differs from product to product. Reduced clock-swing flip-flop (RCSFF) is projected to lower the voltage swing of the clock system. Power consumption per flip-flop is a sum of a clock driver, a flip-flop itself, and interconnection between them. The problem by using RCSFF requires an additional high power supply voltage to reduce the leakage current.

In other hand half swing scheme requires four clock cycle signals.It suffer from skew problem among the 4 clock signals and it requires additional chip area. Single clock flip-flop for half swing clocking does not require high power supply but has long latency.Hybrid latch Flip-Flop(HLFF) and Semi dynamic flip-flop(SDFF) are fastest flip-flops but it consumes large amount of power due to redundant transition at internal nodes.To reduce the redundant power consumption in internal node of high – performance flip-flop Conditional Capture Flip-Flop (CCFF)has been proposed.HSFF,RCSFF,SDFF use full-swing clock signals cause significant power consumption in clock tree.To overcome above problem LSDFF is used. Steve et al. [8] introduced Low-Swing Clock Double Edge triggered Flip-Flop(LSDFF). Christo Ananth et al. [7] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.

B. *Placement*

The use of multi-bit flip-flop (MBFF) was first proposed for reducing clock delay, controlling clock skew, and improving routing resource utilization. [9] Introduced a design methodology for MBFF inference during logic synthesis for area and power reduction. However, to form MBFFs in early design stage, it is hard to consider its effect on timing. Recently, [10] introduced a new algorithm to reduce the power consumption of flip-flops by incrementally forming more multi-bit flip-flops at the post-placement stage.

Considering a discrete and finite MBFF library, Chang *et al.* [6] proposed the problem of using multi-bit flip-flops. To reduce power consumption in the post-placement stage. They use the graph-based approach to deal with this problem. In a graph, each node represents a flip-flop. If two flip-flops can be replaced by a new flip-flop without violating timing and capacity constraints, they build an edge between the corresponding nodes. After the graph is built, the problem of replacement of flip-flops can be solved by finding an *m*-clique in the graph. The flip-flops corresponding to the nodes in an *m*-clique can be replaced by an *m*-bit flip-flop. They use the branch-and-bound and backtracking algorithm [8] to find all *m*-cliques in a graph. Because one node (flip-flop) may belong to several *m*-cliques (*m*-bit flip-flop), they use greedyheuristic algorithm to find the maximum independent set of cliques, which every node only belongs to one clique, while finding *m*-cliques groups. However, if some nodes correspond to

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k-bitflip-flops that k-1, the bit width summation of flip-flops corresponding to nodes in an *m*-clique, *j* , may not equal *m*. If the type of a *j* -bit flip-flop is not supported by the library, it may be time-wasting in **finding impossible combinations** of flip-flops.

IV.ANALYSIS OF MULTI-BIT FLIP-FLOP ALGORITHM

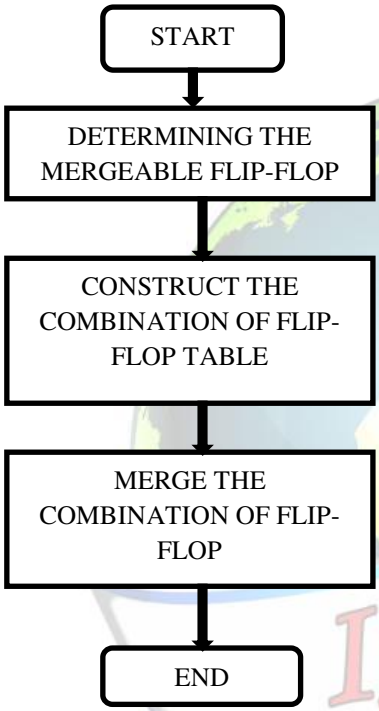

Fig 3: Flow chart for algorithm

1) To facilitate the identification of mergeable flip-flops, transform the coordinate system of cells. In this way, the memory used to record the feasible placement region canalso be reduced.

2) To avoid wasting time in finding impossible combinations of flip-flops, initially build a combination table before actually merging two flip-flops. For example, if a library only provides three kinds of flip-flops, which are 1-, 2-, and 3-bit, first separate the flip-flops into three groups. Therefore, the combination of 1- and 3-bit flip-flops is not considered since the library does not provide the type of 4-bit flip-flop.

The difficulty of this problem has been demonstrated in the above reports. To deal with this problem, the direct way is to repeatedly search a set of flip-flops that can be replaced by a new multi-bit flip-flop until none can be done. However, as the number of flip-flops in a chip increases dramatically, the complexity would increase exponentially, which makes the method impractical. To handle this problem more efficiently and get better results, The

3) The chip can be partitioned into several sub regions and perform replacement in each sub region to reduce the complexity. However, this method may degrade the solution quality. To resolve the problem, hierarchical way is used to enhance the result.

Co-ordinate algorithm

Identifyingthe legal placement region using co-ordinate algorithm. After the legal placement regions of flip-flops are found and the combination table is built, flip-flops can easily merge by using table. To speed up our program, chip can divided into several bins and merge flip-flops in a local bin. However, the flip-flops in different bins may be mergeable. The several bins can combine into a larger bin and repeat this step until no flip-flop can be merged anymore.

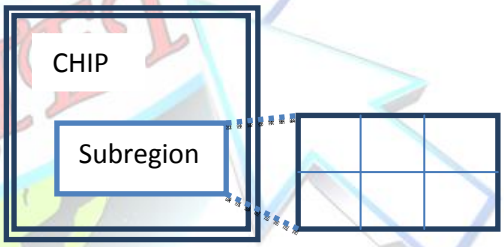

Fig: Region partition with six bin in one subregion

A chip may have millions of gates with a very complex structure. The synchronization of clocks on a chip is critical to the performance and reliability of the chip. In a Synchronous digital system, the clock signal defines the time reference for the movement of data within thesystem. The chip can divided into several subregion, Here we first determine a suitable size for each sub region during partitioning. Since the execution time is actually dominated by the average number of flip-flops included in a subregion, the number of flip-flops can used in a single subregion to represent the size of a subregion, which can be obtained from multiplying the number of bins in a subregion by the average number of flip-flops in a bin. The number of flip-flops removes included in a subregion

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to observe its effect on power consumption and execution. While a subregiongets larger, the execution time becomes longer. However, the power consumption does not decrease proportionally. On the contrary, if the subregion size becomes very small, the power consumption will increase significantly.

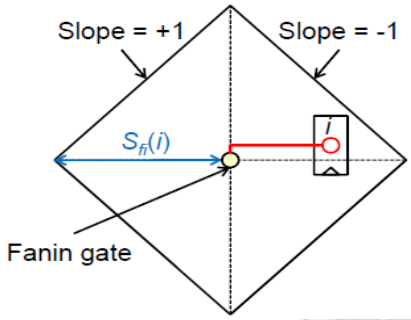

Fig 5a.Timing slack

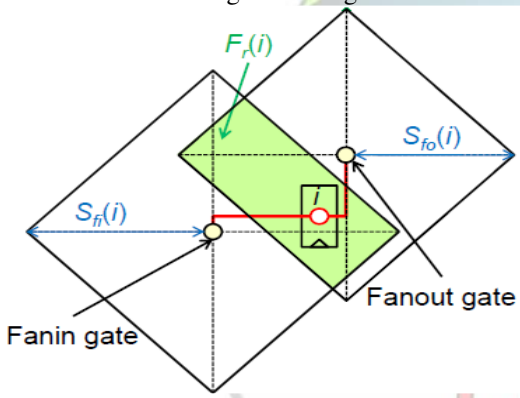

Fig 5b. Feasible Region

The feasible region of each original FF is a 45-degree tilted rectangular region, and these feasible regions may intersect each other shown in figure5. Every intersected region represents the feasible region of a MBFF for the corresponding original FFs. As shown in Figure 6, each intersection of feasible regions of original FFs is a clique in the corresponding rectangle intersection graphs.

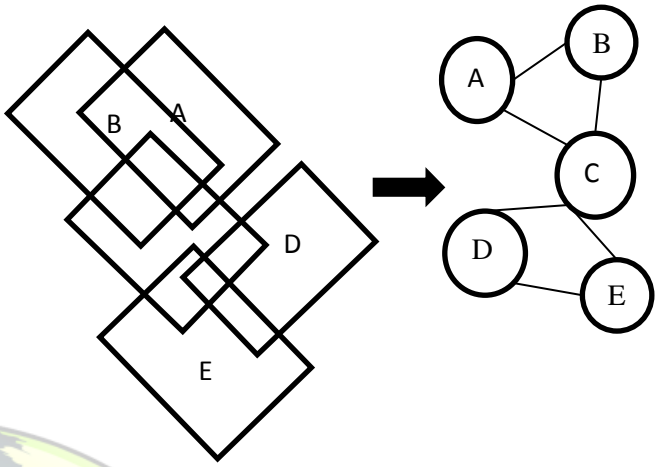

Fig 6: Intersection Graph

Finding legal placement region

Wirelengthis the fundamental objective in standard-cell placement problem. It is generally believed that a timing or congestion oriented approach can hardly be successful without a good wire length minimization. Given a design and a placement which contains a lot of flip-flops, our target is to merge as many flip-flops as possible in order to reduce the total power consumption. A placement with shorter total wire length is relatively easier to be modified to meet timing constraints. several pins connecting to flip flops, the legal placement region of flip flops are the overlapping area of several regions.However, because these regions are in the diamond shape, it is not easy to identify the overlapped area. Therefore the overlapped area can be identified more easily if the coordinate system of cells transforms to get rectangular regions. Thus, if the each segment can rotate 45°, the shapes of all regions would become rectangular, which makes identification of overlapping regions become very simple.

For example, the legal placement region, enclosed by color section in Fig.6 can be identified more easily if the original coordinate system can be changed.In such condition, two coordinates are needed which arethe left-bottom corner and right- top corner of a rectangle, as shown in Figure.

Combination of Flip-Flop table

Uncertainty replaces several flip-flops by a new flip-flop, sure that the new flip-flop is provided by the library ***L*** when the feasible regions of these flip-flops overlap

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Combination Table T	
K1 1-bit	*K2 4-bit*

Library L	
Type1 1-bit	*Type2 4-bit*

Fig (a) Initialize the library L and combination table T

Now a combination table is to be built, which records all possible combinations of flip-flops to get feasible flip-flops before replacementscan gradually replace flip-flops according to the order of thecombinations of flip-flops in this table.

Combination Table T				
K1 1-bit	K2 4-bit	K32-bit K1+k1	K4 3-bit K1+k3	K5 4-bit K3+k3

Fig: New combination obtained from combining k1and k3,and combining k5 is obtained by combining two k3s.

V.EXPERIMENTAL RESULT

This section shows our experimental results.The algorithm is implemented in VHDL language.

Table:1 Power comparison of existing method

Method	Clock Power Reduction	AREA Reduction
HSC	40%	5%
RCSFF	63%	80%
SCFF FOR HSC	21%	5%
PAP	25.3%	1.2%

HSC-Half Swing Clock
RCSFF-Reduced Clock Swing Flip-Flop
SCFF-Single clock Flip-Flop
PAP-Power Aware Placement

VI.CONCLUSION

The proposed design is to reduce the number of flip-flops using multi-bit flip-flops. The legal placement region of flip flops can be identified by using coordinate transformation method. The work can proceeded with a VHDL based code for construction of combination table to identify those flip flops that can be merged and as well as to merge the flip-flops those given by the combination table and later employing a design to work out the proposed work.

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