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A Low-Complexity VLSI Based Color Interpolation Using CSA Algorithm for Real Time Video Applications

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Abstract- A novel low-cost, high-quality, and low-memory-requirement adaptive edge-enhanced color interpolation processor is proposed in this paper. It consists of an laplacian edge detector to enhance the edge information in the images, The anisotropic weighting model is designed to catch more information in horizontal than vertical directions and also this weighting model is to reduce the memory requirement, a filter-based RB compensator to improve the quality, and a register bank to process streaming data directly by using only a two-lime-buffer memory. This low-complexity color interpolation algorithm is proposed for the VLSI implementation in real-time applications using carry save adder for arithmetic operation. This output will be high quality less memory requirements and low complexity. The controller must monitor its input and output data access with the memory to fit the performance of pixel-in and pixel-out. Finally, the proposed color interpolation processor achieves high performance and high throughput. This project can be extended by using combined edge detector and bilinear interpolator is used for the interpolation of RGB. A high-performance and low-complexity algorithms is developed to improve the camera DSP system.

keywords:csa,isotropic filter,DSP system

I.INTRODUCTION

Recently, digital cameras are integrated into many consumer electronic products, such as digital camera, digital video, smart TV, smart phone, tablet PC, etc. The digital cameras are developed by a CCD or a CMOS image sensor that can capture images by color filter array (CFA) technique. The red (R), green (G), and blue (B) colors are sampled as one color in each pixel. Color filter arrays called Bayer CFA, in which two colors have disappeared in each pixel. Thus, it is important to reconstruct the images from CFA to full RGB formats. Many efficient high-quality algorithms have been proposed for reconstructing the full RGB color from CFA images. A spectral model for preserving spectral characteristics of refined CFA images was introduced by Lukac. A low-complexity interpolation method that used a simple image model was proposed by Pei. Moreover, Gunturk and Li presented high performance algorithms to refine the missing colors by using the correlation between the frequencies of the three colors components.

II. THE PROPOSED ALGORITHM

The proposed novel color interpolation algorithm is composed of low-complexity edge detection, a green color interpolation, and a red-blue color interpolation technique.

Each color is interpolated by different methodologies according to the relative locations and reference neighboring samples, in which the BRg(i, j) and RBg(i, j) represent that the green color pixel g(i, j) was interpolated and prepared when it interpolates R(i, j) and B(i, j).

III. SYSTEM IMPLEMENTATION

Fig.3 shows the block diagram of the VLSI architecture for the proposed color interpolation processor. It consists of seven main blocks: a register bank, an edge detector, a green color interpolator (G interpolator), a red and blue colors interpolator model 1 (RB_M1 interpolator), red and blue colors interpolator model 2 (RB_M2 interpolator), a red and blue colors interpolator model 3 (RB_M3 interpolator), and a controller.

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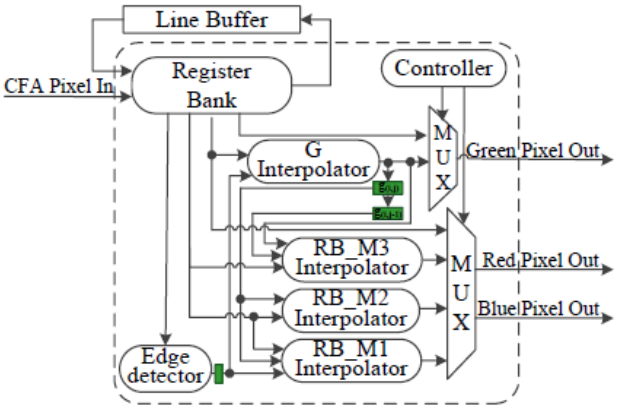

Fig.3 Architecture for the Proposed Color Interpolation Processor

3.1 Register Bank

The register bank was designed to real-time provide fifteen pixels in CFA format for processing the G interpolator and three RB interpolators during each cycle. Fig. 3.1 shows the architecture of the register bank. It is designed with a two-line-buffer memory and constructed with fifteen shift registers. The proposed register bank is designed such that only one value of pixel from memory is received in each cycle time, and then provides fifteen values of CFA pixels as inputs for color interpolation. By adding this register bank, the proposed color interpolation processor achieves the memory access through pixel in and pixel out.

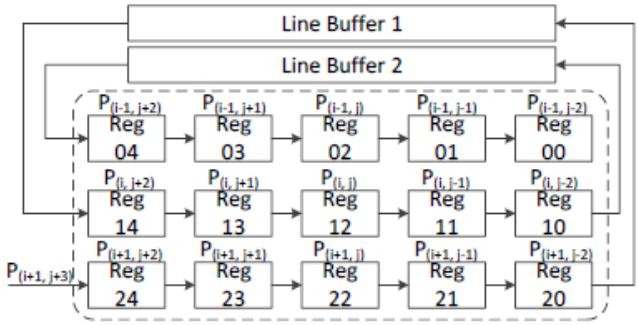

Fig 3.1 Architecture of Register Bank

3.2 Edge Detector

Fig. 3.2 shows the architecture of the proposed edge detector. It consists of six absolute subtractors (|Sub|) and five adders (Add).the adder is of carry save adder.The eight input signals receive their inputs from the registerbank. After being

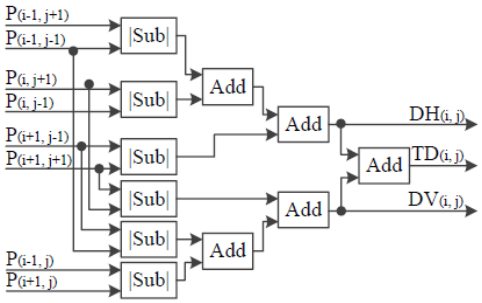

Fig 3.2 Architecture of Edge Detector

processed by the edge detector, the values of TD, DH, and DV at the position of P(i, j) are produced for the green color interpolator and the first model of red and blue color interpolator (RB_M1). In addition, the output signals of the edge detector are also sent to the controller. The output signal of TD provides information of the edge intensity. The other two output signals, DH and DV, give the direction information of the edges.

3.3 Green Color Interpolator (G Interpolator)

Fig. 3.3 shows the architecture of the reconfigurable green color interpolator design. It consists of eight adders, one subtractor, four multiplexers, and five shifters. The control signals, which are sent to multiplexers, are produced by the controller according to the values of TD, DH, and DV. By using reconfigurable technique, the proposed green color interpolator has the characteristics of low cost, high flexibility and high performance. In order to shorten the critical path and improve the design performance, three registers were added in this architecture. The first register is used to store the result of the G interpolator g(i, j). It provides input signal g(i, j) for the RB_M1 and RB_M2 modules.

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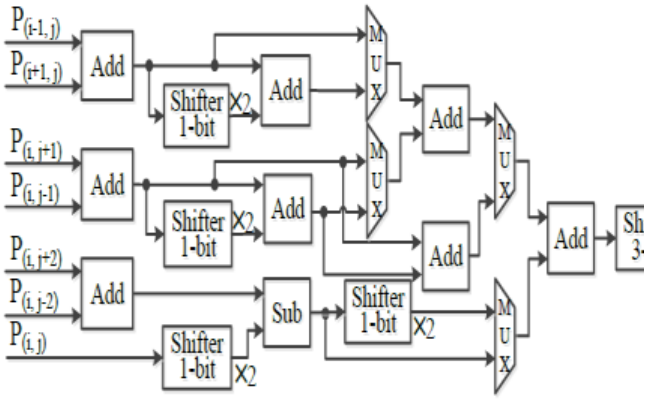

Fig 3.3 Green Color Interpolator

The second register is used to store the value of g(i, j) that provides the input signal g(i, j-1) for the RB_M3 module. Lastly, the third register is used to store the edge information of the TD, DH, and DV. By adding these three registers, this implementation is a pipeline architecture design. It achieves shortening the critical path and providing the interpolated green pixels of g(i, j) and g(i, j-1) for R and B interpolators to improve the quality of the interpolated R(i, j) and B(i, j) pixels.

3.4 Red and Blue Colors Interpolators

The RB_M1 interpolator is shown in Fig. 3.4, which consists of nine adders, one subtractor, two multiplexers, and five shifters. Fig. 3.4.1 shows the VLSI architecture of the RB_M2 interpolator. The RB_M2 interpolator consists of five adders, one subtractor, and two shifters. Fig. 3.4.2 illustrates the VLSI architecture of the RB_M3 interpolator, which can be implemented. RB_M3 interpolator performs like RB_M2. It consists of three adders, one subtractor, and one shifter and has the lowest cost module among the four interpolators.

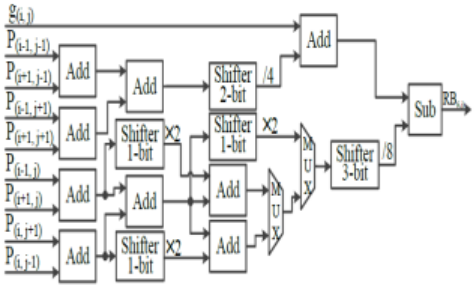

Fig. 3.4.1. Architecture of the red and blue colors interpolator model 1 (RB_M1 interpolator)

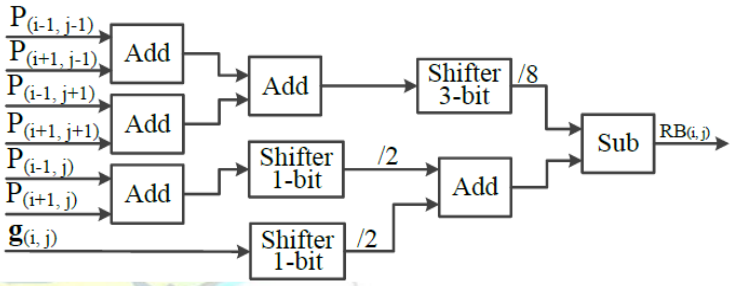

Fig.3.4.2 . Architecture of the red and blue colors interpolator model 2 (RB_M2 interpolator)

3.5 Controller

The controller is implemented by a finite state machine (FSM) sequential circuit. It provides control signals to the multiplexer for selecting input data for the interpolators and is capable of sending reconfigurable control signals for changing the architecture of the interpolators. Moreover, the controller must monitor its input and output data access with the memory to fit the performance of pixel-in and pixel-out. Finally, the proposed color interpolation processor achieves high performance and high throughput.

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3.6 Carry Save Adder

A carry-save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more *n*-bit numbers in binary. The sum and the carry may be fed into two inputs of the subsequent 3-number adder without having to wait for propagation of a carry signal. After all stages of addition, however, a conventional adder (such as the ripple carry or the lookahead) must be used to combine the final sum and carry results.th main advantage of CSA is reduced propagation delay characteristics.

IV. RESULTS AND DISCUSSIONS

Waveform Generated

The Figure 4.1 shows the waveform generated for the given pixel values the waveform shows the input and output and also their corresponding waves.

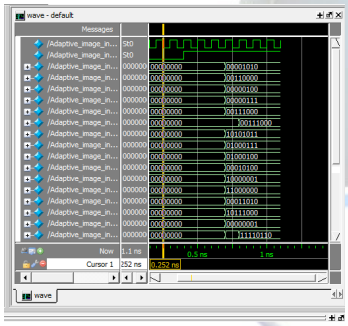

Fig 4.2 comparison between ripple carry adder and carry save adder

V. CONCLUSIONS

In this paper, a novel color interpolation algorithm is proposed to develop a low-cost, low-power, high performance, and high quality color interpolation processor for real-time video applications. Carry save adder is used to reduce the propagation delay. Thisalgorithm became more effective and low arithmetic operations required.

FPGA Spartan3e Xc3s250	Color Interpolation Using Ripple Carry adder Algorithm	Color Interpolation Using Carry Save adder Algorithm
SLICE	133	81
LUT	195	118
DELAY	10.970(ns)	9.203(ns)
POWER	0.391(W)	0.334(W)

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