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Exploring Power Optimal Implementation Technique of 128-Pt radix-24 SDF FFT/IFFT processor for WIMAX using VLSI DESIGN

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ABSTRACT

In this paper we present SISO based decoding scheme for turbo codes using bi-directional SOVA algorithm. The entire implementation has been analyzed in order to suite the IEEE 802.16e, the mobile WiMAX standard. For wireless communication this scheme can be implemented using orthogonal frequency division multiplexing (OFDM) which is a wideband technology designed to eliminate inter symbol interference (ISI) over the multi path fading channel by dividing the whole bandwidth into smaller parallel sub bands and consequently increasing the symbol duration.

Keywords: SISO decoder, Bi-SOVA Decoder, Turbo codes, Mobile WIMAX standard, OFDM, VHDL Synthesis, Puncturing

I.INTRODUCTION

As both of these paradigms of mobile and computer communications strive to meet the market requirements of both high speed and quality of service, they seemingly also move to meet each others characteristics.WiMAX, based on IEEE Std. 802.16 attempts to bring quality of services, high data rates and coverage to wireless computer networks and to work as a ”last mile” solution for end user access. Although not designed for mobility from the start, the standard could lend itself for use in mobility scenarios and for this purpose the IEEE Std. 802.16e has been developed with requirements to support vehicular mobility and seamless handover while maintaining differentiated QoS.

II. The block Scheme of WiMAX signal Transmission from OFDM based transmitter to receiver

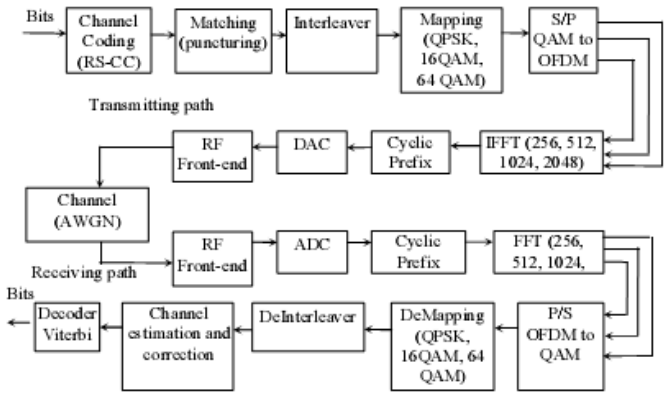

Figure 1:OFDM based WiMAX System

III.BI-SOVA Decoder

SOVA is based on a modified Viterbi algorithm, that provides soft output in the form of the a-posteriori Log-Likelihood Ratios(LLR).Several architectures are proposed to implement SOVA using register exchange, memory traceback and systolic array.A major ottleneck in these architectures is the inherited latency due to trace back of the trellis.This latency is limited by the forward recursion in the Add-Compare-Select operation constraining the throughput.Bi-directional scheme could be used to increase the throughput by eliminating the dependency of the forward recursion only by adding both both forward and backward recrsion at the same time.

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VI. 128 point IFFT/FFT -OFDM

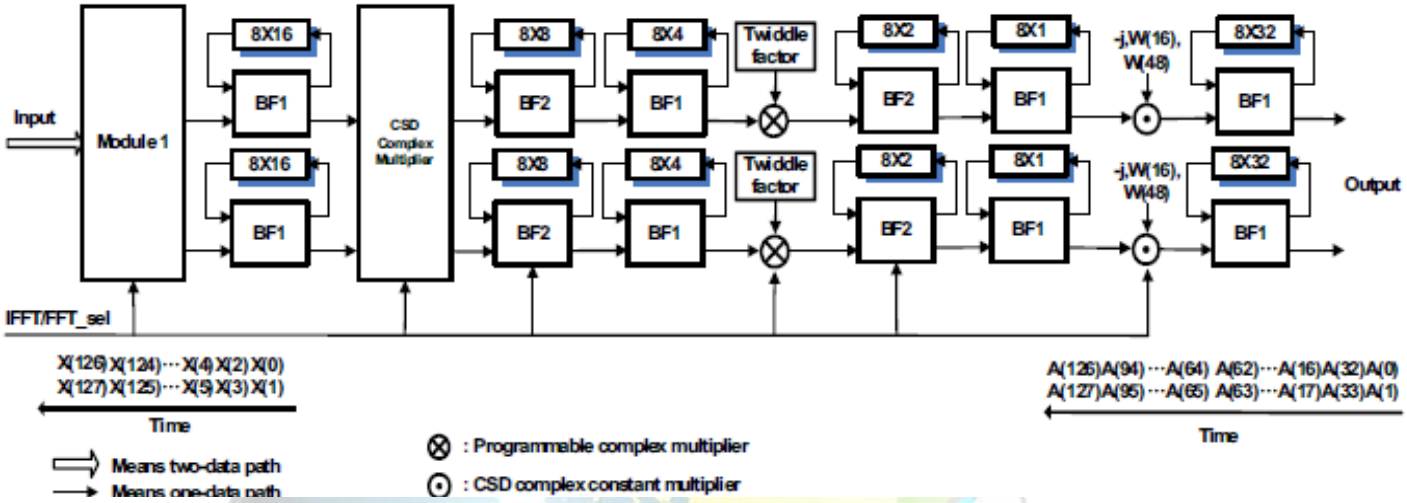

Figure 6: Proposed 2-parallel data-path 128-point radix-24 SDF FFT/IFFT processor

The figure depicts a high-speed, low-complexity two data-path 128-point radix-24 FFT/IFFT for OFDM WiMAX systems.The FFT/IFFT is one of the modules having high computational complexity in the physical layer of the OFDM WiMAX system. The four parallel data path Multipath Delay Feedback structure yields for high hardware complexity. Because more memory and complex multipliers are needed to allow multiple data to be operated simultaneously. Further the main motivation of this paper is to reduce the bit-with of two-parallel data-path pipelined radix-2^4 FFT/IFFT architecture using Booth multipliers with error compensation circuit and minimize the critical path delay using Dadda reduction network.This method leads to reduction of truncation errors compared with direct truncated multipliers.The radix2^4 algorithm can take complex constant multiplier instead of programmable complex multiplier, so it can reduce area and power consumption. Therefore, the proposed two-parallel data-path radix-2^4 single-path delay feedback (SDF) FFT/IFFT architecture offers high throughput, low hardware complexity and low power consumption.It consists of RAM units , Butterfly units (BF1, BF2) ,Complex Booth Multiplers, CSD Complex Constant multipliers Multiplexers and adders.

VII. INTERLEAVER

The performance of a Turbo code with short block length depends critically on the interleaver design. There are two major criteria in the design of an interleaver: the distance spectrum of the code and the correlation between the information input data and the soft output of each decoder corresponding to its parity bits. This paper describes a new interleaver design for Turbo codes with short block length based on these two criteria.

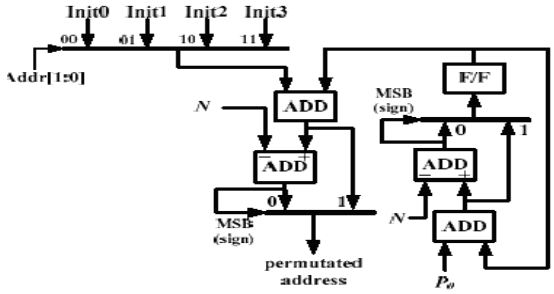

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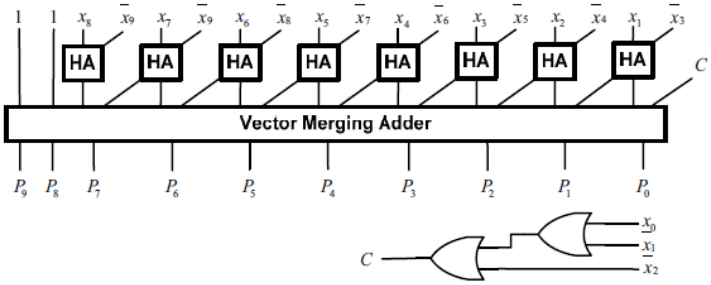
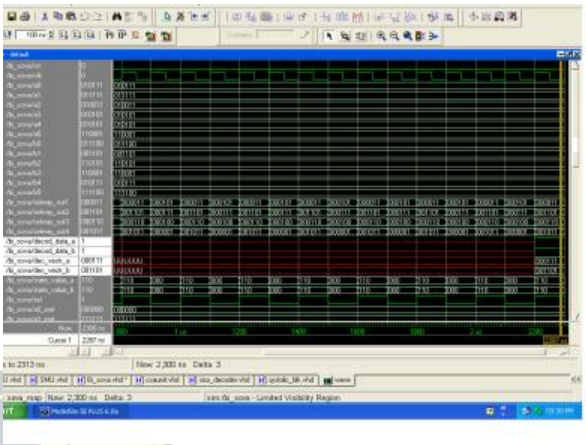
Figure 7: INTERLEAVER UNIT



(b)

Figure 6.1 (a) cos (Π /8) = 0.9239 (b) sin (Π /8) = 0.3827



BI-SOVA decoder

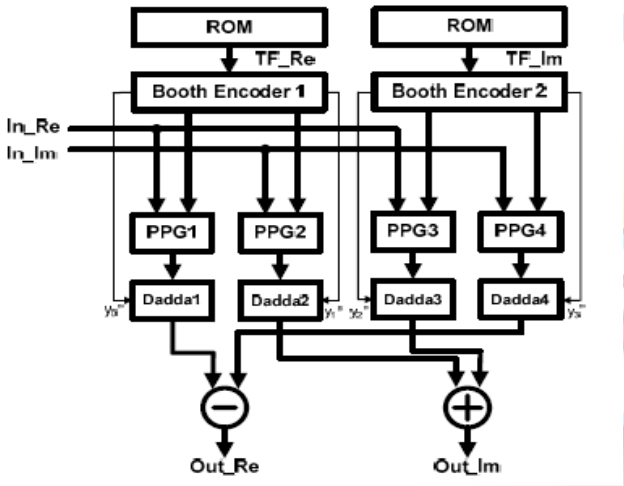
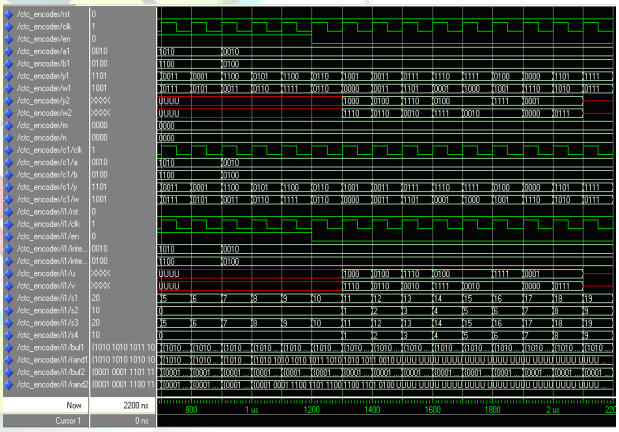


Figure 6.2 : Booth Complex Multiplier



802.16e encoder

VIII.VHDL – SIMULATION RESULTS

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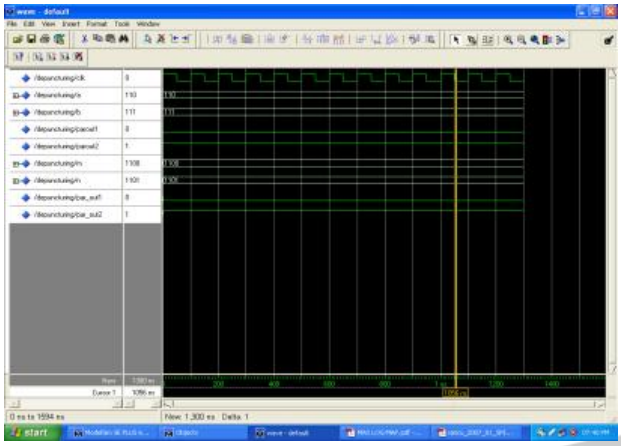
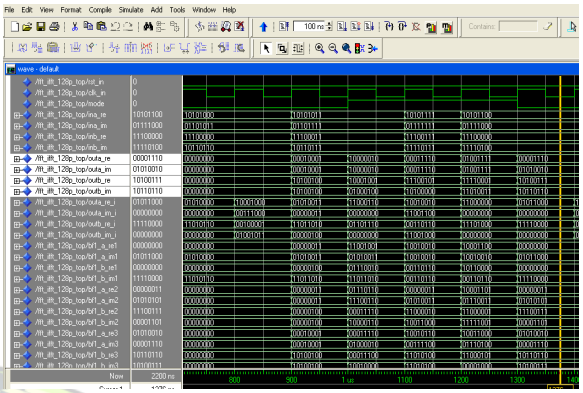
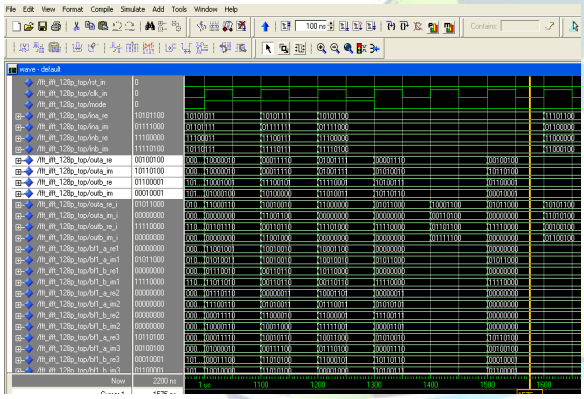


Depuncturing

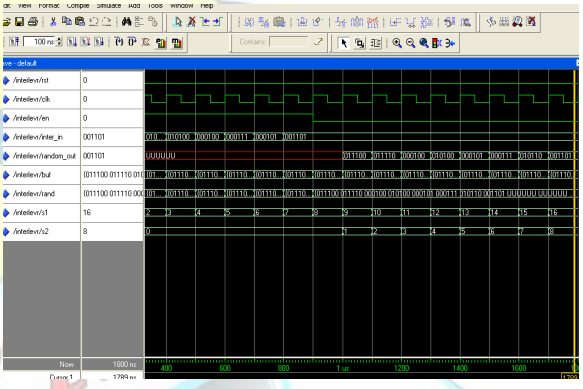
128 point IFFT



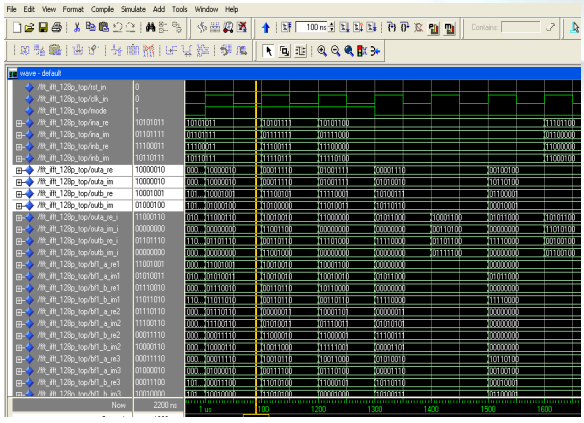
128 point FFT_IFFT



128 point FFT



Interleaver



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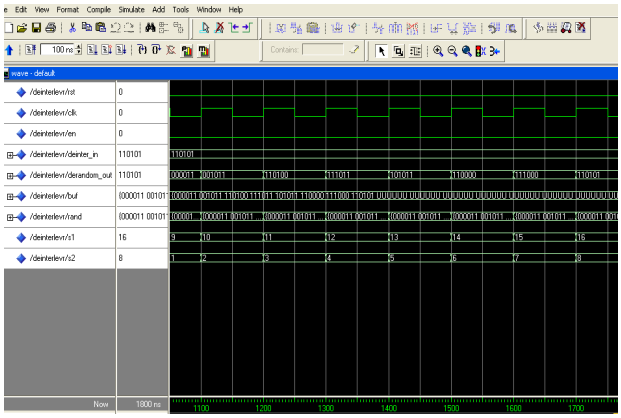

De-Interleaver

IX.SYNTHESIS RESULTS

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2	12,288	1%	
Logic Distribution				
Number of occupied Slices	2	6,144	1%	
Number of Slices containing only related logic	2	2	100%	
Number of Slices containing unrelated logic	0	2	0%	
Total Number of 4 input LUTs	2	12,288	1%	
Number of bonded IOBs	16	240	6%	
Total equivalent gate count for design	12			
Additional JTAG gate count for IOBs	768			

Puncturing scheme

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	98	12,288	1%	
Number used as Flip Flops	70			
Number used as Latches	28			
Number of 4 input LUTs	169	12,288	1%	
Logic Distribution				
Number of occupied Slices	124	6,144	2%	
Number of Slices containing only related logic	124	124	100%	
Number of Slices containing unrelated logic	0	124	0%	
Total Number of 4 input LUTs	169	12,288	1%	
Number of bonded IOBs	27	240	11%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Total equivalent gate count for design	1,916			
Additional JTAG gate count for IOBs	1,296			

802.16e encoder

CONCLUSION

In this paper SISO based Decoder has been implemented using BI-SOVA algorithm, which combines forward SOVA decoder and Backward SOVA decoder with efficient Systolic array scheme. The 802.16e encoder is implemented. Also Puncturing is added to increase the coding rate. Then 128 point FFT / IFFT, which is the kernel module of OFDM system for WiMAX has been implemented. Here two-parallel data-path radix-2^4 single-path delay feedback (SDF) 128 FFT/IFFT architecture has been proposed, which offers high throughput, low hardware complexity and low power consumption.

REFERENCES:

[1] C-H. Shin, S. Choi, H. Lee, and J-K. Pack, "Design and Performance of 4-Parallel MB-OFDM UWB Receiver," IEICE Trans. Communications, vol.E90-B, no. 3, pp. 672-675, March 2007.

[2] D.Garrett and M.Stan, " A 2.5 Mb/s, 23 mW SOVAtraceback chip for turbo decoding application", in the 2001 IEEE International Symposium on Circuits and Systems, 2001, vol.4, pp.61-64

[3] Y-W. Lin, H-Y. Liu, and C-Y. Lee, "A 1-GS/s FFT/IFFT processor for UWB applications,"IEEE Journal of Solid-State Circuits, vol. 40, no. 8, pp. 1726-1735, August 2005.

[4] C-H. Shin, S. Choi, H. Lee, and J-K. Pack, "Design and Performance of 4-Parallel MB-OFDM UWB Receiver," IEICE Trans. Communications, vol.E90-B, no. 3, pp. 672-675, March 2007.

[5] C. Thomas, M. A. Bickerstaff, and L. M. Davis, T. Prokop,Be. Widdup, G. Zhou, D, Barret, and C. Nicol, "Integrated Circuits for Channel Coding in 3G Cellular Mobile Wireless Systems",IEEE Commun. Magazine, August 2003, pp.150-159.

[6] A. Batra et al., "Multi-band OFDM Physical Layer Proposal for IEEE 802.15 Task Group3a," IEEE P802.15-03/268r3, March 2004