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Clock node power performance analysis in CMOS processor

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Abstract: In high performance CMOS device the power consumption, especially leakage and dynamic power has become a major concern for semiconductor industries. FPGAs are less power efficient than custom ASICs, due to the overhead required providing programmability. The dynamic power consumption is increased considerably due to switching of clock signals. This paper focuses on circuit optimization and design modification based on Lookup tables. . In this paper various design techniques for low power optimization are surveyed and parameters such as switching power, leakage current and timing delays were analyzed. Reduction in dynamic power consumption is observed when introducing Lookup table based grained (LUTBG) clock gating techniques in global and local routing of FPGA clock architecture. By using our proposed method dynamic power consumption has been reduced 70% at each leaf node of clock network. Simulation results are obtained using 0.12µm, 50nm, 70nm, 90nm CMOS technology**.**

Keywords: FPGA, Dynamic power, clock skew, dual V_{DD}, dual frequency, Lookup table

I. INTRODUCTION

Field-programmable gate arrays (FPGAs) are a popular choice for digital circuit implementation because of their fast turnaround time, growing density and speed, and relatively low cost. Despite continuing technology scaling and decreasing supply voltage values, the power consumed by the largest FPGA devices is increasing, with the power of the largest chips now being measured in watts. Reducing the power consumption of FPGAs is beneficial as it leads to lower packaging and cooling costs as well as improves reliability. Additionally, if FPGA‘s are to be used more pervasively in portable battery-powered applications, low power consumption are essential. In addition to digital functions, some FPGAs have analog features. A recent trend has been to take the coarse-grained architectural approach a step further by combining the logic blocks and traditional FPGAs with embedded microprocessors and related peripherals to form a complete "system on a programmable chip". The logic blocks have the flexibility to connect to the routing resources surrounding them. The I/0 pads are evenly distributed around the perimeter of the FPGA. I/O pad has a typical I/O cluster, which is a Logic block that consists of one or more Basic Logic Elements (BLEs) grouped together. The factors affecting power in FPGAs are device selection, environmental conditions, resources used by design and signal activities. Understanding these factors allows designers to effectively use the Power Play power analysis tools. Global signal networks span large portions of the device and have high capacitance, resulting in significant dynamic power consumption. Clock gating technique is predominant with clock signals are AND[ed] with explicitly defined enabling signals. In FPGAs customized clock networks can be implemented using programmable interconnects to reduce dynamic power consumption. Clock skew, clock delay, signal slew, and power dissipation measurements for the different clock topologies are mentioned and the measurements suggest that each topology provides certain advantages and disadvantages in terms of different performance criteria [1]. A set of analytical expressions which accurately model the behavior of supply noise induced period jitter of global binary clock trees without losing the details of clock distribution design parameters. These accurate expressions and their derivation process are used to provide detailed insight into the relationships between period jitter of binary clock distribution and distribution design parameters [2] an additional 12.8% reduction in the worst case peak current can be achieved by reconfiguring the polarity assignment based on the clock gating information. Random jitter and deterministic jitter

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analysis on the proposed polyphase filter (PPF)-based multiphase clock in frequency multiplier with reference to the benchmark jitter analysis of the multiphase clock counterpart using conventional delay-locked loop (DLL) approach[3].Many studies have focused on reducing the speed and area advancements include cluster- Factored form matching reduces gating logic area occupied[4].One important class of FPGAs are those that use lookup tables (LUTs) to implement combinational logic. The K inputs are used to address a 2K by 1-bit digital memory that stores the truth table of the Boolean control function. The ability of a K-input LUT to implement any Boolean function of K-variables differentiates the synthesis of LUT circuits from synthesis for conventional ASIC technologies. The major difference occurs during the technology mapping phase of logic synthesis. For values of K greater than 3, the large number of functions that can be implemented by a K-input LUT makes it impractical to use conventional library-based technology mapping. However, the completeness of the set of functions that can be implemented by a LUT eliminates the need for a library of separate junctions. It optimizes the clock network by enabling the control input which switches the logic blocks.

A. Power Consumption

Power consumption in CMOS circuits consists primarily of static power dissipated by leakage currents and dynamic power, which is in turn comprised of short circuit dissipation, and the switching power consumed while charging and discharging load capacitances. Dynamic power is the additional power consumed through the operation of the device caused by signals toggling and capacitive loads charging and discharging. CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. Power consumption is an important part of the equation determining the end product's size, weight, and efficiency. FPGAs are becoming more attractive for these applications due to their shorter product life cycle. FPGAs are programmable, so they allow product differentiation. Selecting an appropriate FPGA architecture is critical in achieving the best static and dynamic power consumption. Dynamic power is the power dissipated during active state due to switching activity of input discharging parasitic capacitances. Power consumption is determined by several factors including frequency f, supply voltage V, data activity α, capacitance C, leakage and short circuit current.

$$Pdynamic = \frac{1}{2}\alpha cfVdd^2 \quad \text{.....(1.1)}$$

Total dynamic power=Transient power + Capacitive load power Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit. To save power consumption, it has been shown that the clock signal can be gated without changing the functionality under certain clock-gating conditions. Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks.

Clock network power reduction can be obtained by the following approaches,

- Register cluster adjustments to reduce interconnect resource usage on clock network, thereby reducing capacitance and power.
- Clock gating technique, where the clock is allowed to toggle only in the required portion of clocked network.
- Reducing clock load in the system by reducing the number of clocked transistors

The techniques to reduce Dynamic Power consumption are, Clock Gating, Frequency controller, improved switching activity, Glitch removal, Pipelining, Guarded Evaluation.

II. RELATED WORK

In previous work single voltage and frequency is applied to the whole circuit. The power consumed is high as both active and inactive blocks use the same supply voltage and frequency. This power consumption degrades the system performance and life time of portable application. In order to overcome this drawback, we propose dual VDD and frequency technique along with controller device using LUTs. As the switching power is quadratically related to the supply voltage, the power consumption is effectively reduced [5] & [6]. In other words, dynamic power dissipation is caused by the charging. Since an input can change without necessarily resulting in logic transition in the output, dynamic power can be dissipated even when an output does not change its logic state. The dynamic power gating techniques can be classified into two types: coarse-grain power gating and fine-grain power gating. Low power FPGA architecture is generated with the use of fine grained VDD control lookup table have its own controller device. So the number of controllers used in fine grained technique is much larger than that of coarse grained technique. In this technique the controller device is always running, these results in large area and dynamic power overheads. Due to these overheads fine grained technique is less efficient than the coarse grained technique [7]-[10].In coarse-grain power gating, a large number of LUTs share a single sleep controller so the area and power overheads of the sleep

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controller are relatively small. An algorithm of activity-sensitive clock tree construction was used, New FPGA routing switch designs that are programmable to operate in three different modes: high-speed, low-power, or sleep. High-speed mode provides similar power and performance to traditional FPGA routing [11] & [12]. This algorithm merged the nodes with the similar activity pattern to shut off the clock signal maximally. In this approach clock tree was constructed under three different kinds of merging. First method is to merge the nodes with the similar activity patterns, second one is to merge the nodes such that the transition of control signal is minimal and in third technique they merged the nodes based on the trade-off between activity similarity and transition. Based on grained clock tree network, the considerable amount of clock tree power with much fewer gating logics and the overhead to the placement is also gets reduced. Power dissipation of the control signal for the masking gates was not reduced. Hence coarse grain gated clock tree topology was constructed. The routing phase determines the actual course of the wires connecting the cells that has been placed. There are two types of global routing, sequential and concurrent routing. In Sequential approach as the name suggests, nets are routed one by one. However, once a net has been routed it may block other nets which are yet to be routed. As a result, this approach is very sensitive to the order in which the nets are considered for routing. In Concurrent approach, it avoids the ordering problem by considering routing of all the nets simultaneously. In global routing, there are different algorithms like Maze routing algorithms, Spanning tree, Geyer's multilayer maze router etc. In previous work they first routed simple nets consisting of only two or three terminals since there are few choices for routing such nets. A nice property of Lee's algorithm is that it guarantees to find a path between two points if such a path does exist, and the path is the shortest One, even with the obstacles.

III. PROPOSED METHOD

Reducing the supply voltage (VDD) is an effective technique for reducing both dynamic and static power. Dynamic power has a quadratic dependency on supply voltage, while both sub-threshold leakage and gate leakage exhibit exponential dependencies on the supply voltage. However, reducing supply voltage also negatively affects circuit performance. . In order to minimize drastic increase in dynamic power, supply voltage scaling is an efficient method. A two level supply voltage controller is proposed which reduces power consumption in logic blocks to greater extent. The two voltage levels are VddH (3.3V) and VddL (1.2V). VddH is supplied to logic block when the input to logic block is high otherwise VddL powers the logic block. Dynamic power consumption during unnecessary switching is reduced to greater extent by utilizing this voltage controller.

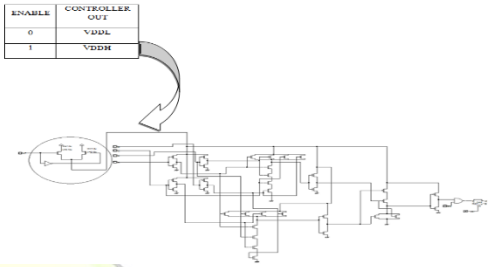

Fig 1: Schematic of simple low/high state Vdd controller circuit

Consequently, if logic blocks are statically determined to be operating at low or high VDD, the placement and routing algorithms need to be modified accordingly. However, static assignment of VDD to the blocks may prevent the ability to reduce power consumption or to meet timing constraints for some designs. In contrast, the use of VDD-programmability for each block helps to tune the number of high and low VDD blocks as desired by the application. In this approach, the challenge is in determining the VDD assignments to each block. Furthermore, positioning of the controller influences the ability to assign lower VDD to the routing blocks. In our programmable dual-VDD architecture (figure 3.1), the VDD of a circuit block is selected between VDDH and VDDL by using two high-VT transistors (supply transistors) connecting the block to the supplies. The state (ON/OFF) of each supply transistor is controlled by a configuration bit.

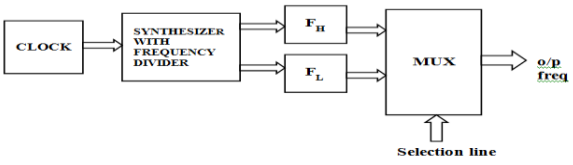

Fig 2: Schematic of simple dual frequency controller circuit

Dual frequency is selected as fH and fL, where fH is high frequency and fL is low frequency. The phase locked loop is used for dividing the single frequency into two. The fH is applied to the active nodes and fL to the inactive nodes. By halving the clock frequency in the global part of the clock tree, buffer resizing is avoided when the supply voltage is scaled; thereby power consumption is further reduced. Much

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of the logic in a CLB is implemented using very small amounts of RAM in the form of LUTs. It is assumed that the number of system gates in an FPGA refers to the number of NAND gates and NOR gates in a particular chip. But in reality, all combinatorial logic (ANDs, ORs, NANDs, XORs, and so on) is implemented as truth tables within LUT memory. A truth table is a predefined list of outputs for every combination of inputs.

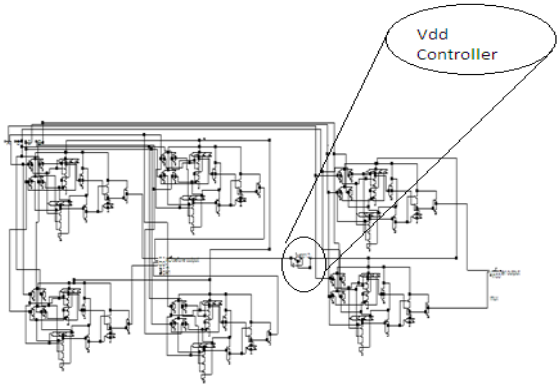

Figure 3.1 Schematic diagram of logic blocks with Vdd controller device

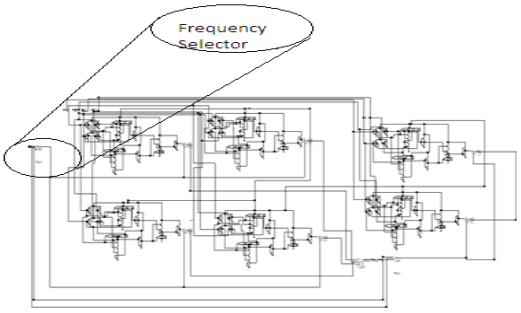

Figure 4 Schematic diagram of logic blocks with Frequency controller device

Consequently, if logic blocks are statically determined to be operating at low or high V_{DD}, the placement and routing algorithms need to be modified accordingly as in [14]. However, static assignment of V_{DD} to the blocks may prevent the ability to reduce power consumption or to meet timing constraints for some designs. Technology mapping selects sub-networks of the optimized network to be implemented by the available circuit elements. In the case of LUT-based FPGAs, any sub-network with at most K inputs can be implemented by a K-input LUT. The final circuit must include a LUT implementing each of the primary outputs and all of the LUT inputs that are not primary inputs.

The optimization goal for the synthesis of LUT circuits is typically the minimization of the total number of LUTs, the number of levels of LUTs or both. Minimizing the number of LUTs in the circuit increases the size of designs that can fit into the fixed number of LUTs available in a given FPGA. The minimization of the number of levels of LUTs can improve the performance of the circuit by reducing the number of logic block delays and programmable routing delays on the longest path. The major obstacle to applying library-based technology mapping to LUT circuits is the large number of different functions that a K-input LUT can implement. The function implemented by a K-input LUT is determined by the values stored in its 2K memory bits. Since each bit can independently be either 0 or 1, there are 2K different Boolean functions of K variables. The major target of our design is to minimize the total switching activity and dynamic power consumption of logic block without performance degradation. By utilizing these clock controllers in global and local clock routing network power consumption can be reduced in considerable proposition

IV. DYNAMIC POWER COMPARISONS

The power and Idd current for Lookup table based clock gating technique were simulated with VDD ranging from 0V to 5V.The power consumption of simple electrical clock gating network in FPGA logic blocks were analyzed. The simulation results were obtained from M-power simulations in 0.12µm, 50nm, 70nm, 90nm CMOS technology at room temperature. Each Lookup table drives logic blocks which are connected to leaf node.

Vdd (V)	Maximum Idd (mA) with LUT based gating	Maximum Idd (mA)with out gating	Power (mWatt) without gating	Power (mWatt) with LUT based gating
0.5	0.036	0.083	0.01	0.012
1.5	6.135	5.112	0.849	1.273
2.5	2.676	5.048	4.093	2.962
3.5	3.515	5.699	5.513	3.913
4.5	4.184	6.644	6.626	4.693

TABLE I Comparison results for Dynamic power dissipation leakage current of clock network and lookup table based clock network

Our design flow includes two parts: fine grained clock gating for global routing and coarse grain clock gating for local routing i.e.) leaf node of clock tree. In order to evaluate the effectiveness of our method, we compare simulation results of non-gated and Lookup table based gated clock tree network also the layout of grained clock tree is shown in fig.9The power consumption of simple electrical

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clock network in FPGA block is identified as 5.052mw with Lookup table based grained gating network and 7.117mw without clock gating network considering simple combinational logic block at leaf node of local routing. Thus using Lookup table based grained clock gating network the overall dynamic power consumption of clock network is reduced considerably and the simulation results using M-power simulations in 0.35µm CMOS processor is presented.

V. CONCLUSION

A Lookup table based dual-VDD and dual frequency FPGA architecture that provides significant power savings with efficient routing and minimal performance penalty. Variations of the VDD assignment and controller device were explored. The dynamic power was reduced around 60- 70%. This leads to efficient utilization of power consumption in FPGA Controlled Device. Power supply network to support configurable VDD and frequency may introduce extra routing congestion. The total power reduction using LUT based dual VDD and dual frequency techniques is significantly higher than other conventional methods .The simulation results indicate 70% of reduction in power dissipation in every leaf node of clock Network. It can be concluded that Lookup table based grained clock gating can be used for high speed applications with reduction in power consumption.

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