



Novel Control Technique for Interline Unified Power Quality Conditioner (iUPQC)

PG SCHOLAR PRASANTH.P.J

ASSISTANT PROFESSOR SIMON RAJA.J

DEPARTMENT OF ELECTRICAL AND ELECTRONICS SATYAM COLLEGE OF ENGINEERING AND TECHNOLOGY

Abstract—This paper presents a simplified control technique for a dual three-phase topology of a unified power quality conditioner—iUPQC. The iUPQC is composed of two active filters, a series active filter and a shunt active filter (parallel active filter), used to eliminate harmonics and unbalances. Different from a conventional UPQC, the iUPQC has the series filter controlled as a sinusoidal current source and the shunt filter controlled as a sinusoidal voltage source. Therefore, the pulse width modulation (PWM) controls of the iUPQC deal with a well-known frequency spectrum, since it is controlled using voltage and current sinusoidal references, different from the conventional UPQC that is controlled using nonsinusoidal references. In this paper, the proposed design control, power flow analysis, and experimental results of the developed prototype are presented.

Index Terms—Active filters, control design, power line conditioning, unified power quality conditioner (UPQC).

sinusoidal, and therefore, their references are also sinusoidal.

Some authors have applied this concept, using voltage source inverters in uninterruptable power supplies [35], [36] and in UPQC [10], [25], [32]. In [10], this concept is called “dual topology of unified power quality conditioner” (iUPQC), and the control schemes use the $p - q$ theory, requiring determination in real time of the positive sequence components of the voltages and the currents.

The aim of this paper is to propose a simplified control technique for a dual three-phase topology of a unified power quality conditioner (iUPQC) to be used in the utility grid connection. The proposed control scheme is developed in ABC reference frame and allows the use of classical control theory without the need for coordinate transformers and digital control implementation. The references to both SAF and PAFs are sinusoidal, dispensing the harmonic extraction of the grid current and load voltage.

This paper is organized as follows. In Section II, the iUPQC circuit is presented, and its operation is explained in detail. Section III shows the power circuit design of the converters. The analysis and design of the passive filters are presented in Section IV. The proposed control scheme and its design are shown in Section V, while the power flow is analyzed in Section VI. Section VII presents the experimental results, and finally, the conclusion is drawn in Section VIII.

II. DUAL UPQC

The conventional UPQC structure is composed of a SAF and a PAF, as shown in Fig. 1. In this configuration, the SAF works as a voltage source in order to compensate the grid distortion, unbalances, and disturbances like sags, swells, and flicker. Therefore, the voltage compensated by the SAF is

THE USAGE of power quality conditioners in the distribution system network has increased during the past years due to the steady increase of nonlinear loads connected to the electrical grid. The current drained by nonlinear loads has a high harmonic content, distorting the voltage at the utility grid and consequently affecting the operation of critical loads.

By using a unified power quality conditioner (UPQC) [1]–[32], it is possible to ensure a regulated voltage for the loads, balanced and with low harmonic distortion and at the same time draining undistorted currents from the utility grid, even if the grid voltage and the load current have harmonic contents. The UPQC consists of two active filters, the series active filter (SAF) and the shunt or parallel active filter (PAF) [1], [2].

The PAF is usually controlled as a nonsinusoidal current source, which is responsible for compensating the harmonic current of the load, while the SAF is controlled as a nonsinusoidal voltage source, which is responsible for compensating the grid voltage. Both of them have a control reference with harmonic contents, and usually, these references might be obtained through complex methods [4], [5], [14], [17], [21], [23], [27].

Some works show a control technique to both shunt and SAFs which uses sinusoidal references without the need of harmonic extraction, in order to decrease the complexity of the reference generation of the UPQC [31], [33].

An interesting alternative for power quality conditioners was proposed in [34] and was called line voltage regulator/conditioner. This conditioner consists of two single-phase current source inverters where the SAF is controlled by a current loop and the PAF is controlled by a voltage loop. In this way, both grid current and load voltage are



composed of a fundamental content and the harmonics. The PAF works as a current source, and it is responsible for compensating the unbalances, displacement, and harmonics of the load current,

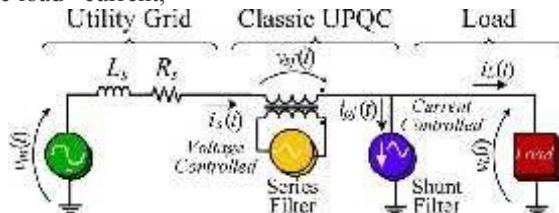


Fig. 1. Conventional UPQC.

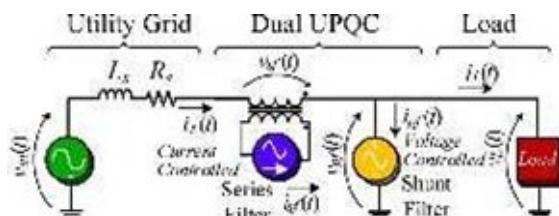


Fig. 2. Dual UPQC (iUPQC).

ensuring a sinusoidal grid current. The series filter connection to the utility grid is made through a transformer, while the shunt filter is usually connected directly to the load, mainly in low-voltage grid applications. The conventional UPQC has the following drawbacks: complex harmonic extraction of the grid voltage and the load involving complex calculations, voltage and current references with harmonic contents requiring a high bandwidth control, and the leakage inductance of the series connection transformer affecting the voltage compensation generated by the series filter.

In order to minimize these drawbacks, the iUPQC is investigated in this paper, and its scheme is shown in Fig. 2. UPQC, using an association of the SAF and PAF, diverging only from the way the series and shunt filters are controlled. In the iUPQC, the SAF works as a current source, which imposes a sinusoidal input current synchronized with the grid voltage. The PAF works as a voltage source imposing sinusoidal load voltage synchronized with the grid voltage. In this way, the iUPQC control uses sinusoidal references for both active filters. This is a major point to observe related to the classic topology since the only request of sinusoidal reference generation is that it must be synchronized with the grid voltage. The SAF acts as high impedance for the current harmonics and indirectly compensates the harmonics, unbalances, and disturbances of the grid voltage since the connection transformer voltages are equal to the difference between the grid voltage and the load voltage. In the same way, the PAF indirectly compensates the unbalances, displacement, and harmonics of the grid current, providing a low-impedance path for the harmonic load current.

III. POWER CIRCUIT

For this work, a commercial back-to-back power module was used, manufactured by SEMIKRON. The passive components are shown in Table II.

IV. OUTPUT PASSIVE FILTER DESIGN

The iUPQC circuit can be analyzed by a single-phase wiring diagram, as shown in Fig. 4. The utility grid impedance is represented by $Z_s = j\omega L_s + R_s$, while the coupling transformer leakage impedance is represented by $Z_{lg} = j\omega L_{lg} + R_{lg}$, and the voltage sources v_{sc} and v_{pc} represent the equivalent structures of the series and shunt filters, which generate a waveform composed of the fundamental component and harmonics that originated from the commutation of the switches. These high frequencies must be filtered by the output passive filters of the iUPQC, ensuring sinusoidal grid currents and load voltages.

Fig. 5 shows the equivalent circuit used for the SAF output impedance analysis, and Fig. 6 shows the equivalent circuit used for the PAF output impedance analysis. In order to simplify the analysis of the PAF, the voltage source v_{sc} and the inductance L_{sf} , which are series connected, were considered as a current source.

Observing the equivalent circuits, we can claim that the PAF output impedance affects the frequency response of the SAF, while the SAF output impedance does not affect the frequency response of the PAF. Therefore, the output passive filter design of the iUPQC should be started with the PAF design followed by the SAF design.

$$v_{pc}(s) = L_{pf} C_{pf} s^2 + s \frac{1}{C_{pf} R_L} + \frac{1}{L_{pf} C_{pf}}$$

The inductor L_{pf} was defined by the power design, so the capacitor C_{pf} will be defined according to the desired cutoff frequency of the filter. In this design, a 2.9-kHz cutoff frequency was used, resulting in a value of $10 \mu\text{F}$ for the C_{pf} filter capacitor. Fig. 7 shows the PAF frequency response for the nominal load and no load.

The high-frequency filter transfer function of the SAF is derived by analyzing the circuit of Fig. 5 and is shown in

$$\frac{i_s(s)}{v_{sc}(s)} = \frac{n}{\{sL_{sf} + n^2 [sL_{lg} + R_{lg} + \alpha + \beta] \cdot \gamma\}} \quad (2)$$

where

$$\frac{sL_{pf} R_L}{sL_{pf} R_L}$$

$$\alpha = \frac{s^2 L_{pf} C_{pf} R_L + sL_{sf} + R_L}{s^2 L_{pf} C_{pf} R_L + sL_{sf} + R_L} \quad (3)$$

$$\beta = \frac{sL_{rd} + R_{rd}}{s^2 L_s C_{sf} + sC_{sf} R_s + 1} \quad (4)$$



The power circuit of the proposed iUPQC is made up of two four-wire three-phase converters connected back to back and their respective output filters, as shown in Fig. 3.

Three single-phase transformers are used to connect the SAF to the utility grid, while the PAF is connected directly to the load. Table I shows the specification of the iUPQC.

$$\gamma = s^2 C_{sf} L_s + s C_{sf} R_{lg} + 1. \quad (5)$$

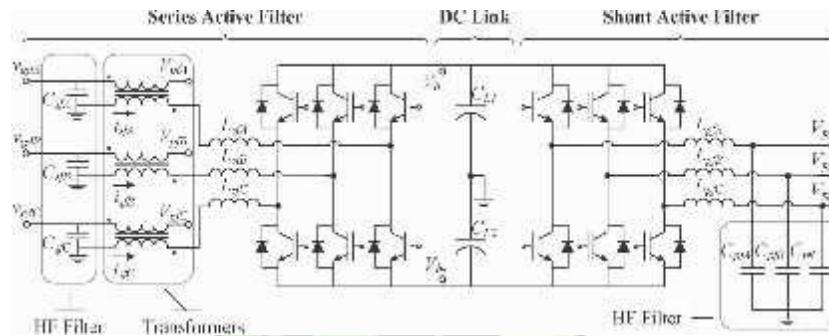


Fig. 3. Power circuit of the iUPQC.

TABLE I
DESIGN SPECIFICATIONS OF THE iUPQC

The figure displays four horizontal timelines representing different transformer models. Each timeline consists of a series of colored rectangles of varying widths, indicating the duration of specific events or components. The timelines are stacked vertically, with labels 'Transformer info' and 'n' positioned below the first timeline.

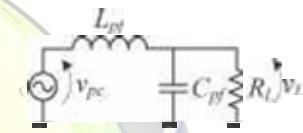


Fig. 6. Equivalent circuit as viewed by PAF.



TABLE II
 COMPONENT SPECIFICATIONS OF THE POWER MODULES

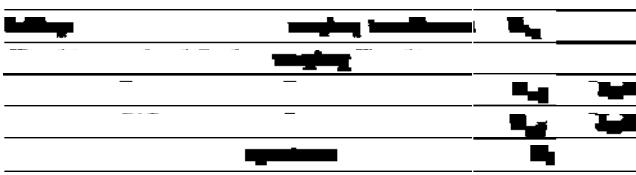


Fig. 4. Single-phase wiring diagram of the dual UPQC.

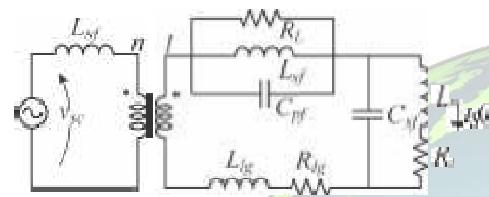


Fig. 5. Equivalent circuit as viewed by SAF.

load. It can be noted that the filter response has a low cutoff frequency that can reduce the bandwidth of the SAF, decreasing its effectiveness under operation with harmonic contents on the grid voltage. This characteristic of low-frequency attenuation is undesirable and intrinsic to the structure due to the leakage impedance of the coupling transformers.

An important contribution of this paper and different from what it was stated in some previous articles, which deal with the same iUPQC control strategy, is that, in spite of the SAF operates with sinusoidal reference, the control of this filter needs to deal with high frequency since the current imposed

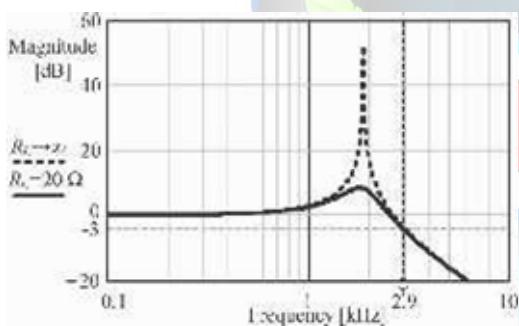


Fig. 7. HF filter frequency response of the PAF.

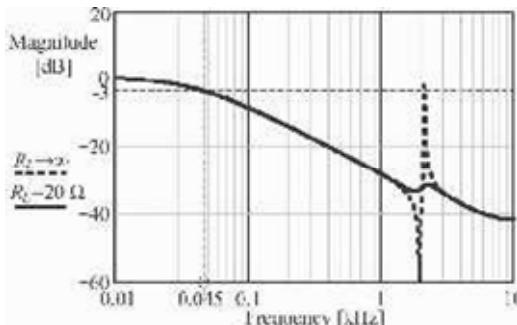


Fig. 8. HF filter frequency response of the SAF.

by the SAF is obtained through the voltage imposition on this filter output inductor. The voltage imposed on these inductors is



complementary to the utility grid voltage harmonics so that it guarantees a sinusoidal current through the filter. Different from the conventional UPQC whose narrow-band frequency control may distort the load voltage, in the iUPQC, the narrow-band frequency control may distort the current drained from the utility grid. The usage of high-power coupling transformers, with low leakage inductance, and the design of higher voltage dc link, allowing the imposition of higher current rate of change on the filter output inductor, are solutions to change the characteristics of the filter attenuation in low frequencies.

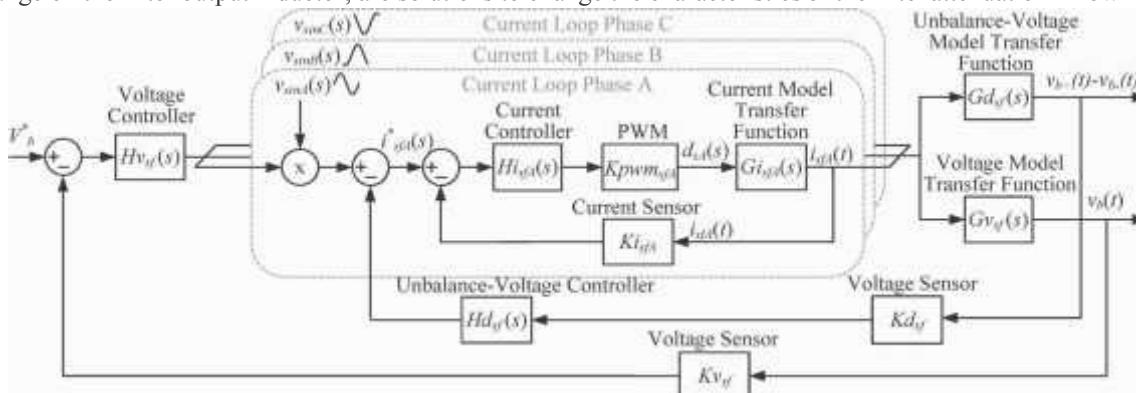


Fig. 9. Control block diagram of the SAF controller.

V. PROPOSED CONTROL SCHEME

The proposed iUPQC control structure is an ABC reference frame based control, where the SAF and PAF are controlled in an independent way.

In the proposed control scheme, the power calculation and harmonic extraction are not needed since the harmonics, unbalances, disturbances, and displacement should be compensated.

The SAF has a current loop in order to ensure a sinusoidal grid current synchronized with the grid voltage. The PAF has a voltage loop in order to ensure a balanced regulated load voltage with low harmonic distortion. These control loops are independent from each other since they act independently in each active filter. The dc link voltage control is made in the SAF, where the voltage loop determines the amplitude reference for the current loop, in the same mode of the power factor converter control schemes. The sinusoidal references for both SAF and PAF controls are generated by a digital signal processor (DSP),

A. SAF Control

Fig. 9 shows the control block diagrams for the SAF. The SAF control scheme consists of three identical grid current loops and two voltage loops. The current loops are responsible for tracking the reference to each grid input phase in order to control the grid currents independently. One voltage loop is responsible for regulating the total dc link voltage, and the other is responsible for avoiding the unbalances between the dc link capacitors.

The total dc voltage control loop has a low-frequency response and determines the reference amplitude for the current loops. Thus, when the load increases, overcoming the input grid current, the dc link supplies momentarily the active power consumption, resulting in a decrease of its voltage. This voltage controller acts to increase the grid current reference, aiming to restore the dc link voltage. In the same way, when the load decreases, the voltage controller decreases the grid current reference to regulate the dc link voltage. Considering the three-

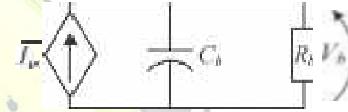


Fig. 10. Equivalent circuit of the SAF voltage loop.

neutral point can be represented by the circuit shown in Fig. 10, composed of a current source which is in parallel with the dc link impedance and whose current source represents the average charge current of the dc link.

The resistor R_b is absent in the real circuit ($R_b \rightarrow \infty$); it just represents instantaneous active power consumption of the dc link. The term instantaneous is related to the time of the switching period, since active power consumption of the dc link is null for the utility grid voltage frequency. The average charge current of the dc link is given by

which ensure the grid voltage synchronism using a phase-

The SAF peak current I_{sfpk} is considered the same for the three phases due to balanced current. Through (6), the voltage loop transfer function is obtained and is represented by

$$Gv_{sf}(s) = \frac{V_b(s)}{I_{sf}(s)} = \frac{\frac{3}{2} \cdot n \cdot V_{gdpk}}{V_b} \cdot \frac{1}{R_b + sC_b} \quad (7)$$

where

- V_{gdpk} peak of the grid voltage;
- V_b dc link voltage;
- R_b load equivalent resistance;
- C_b total dc link equivalent capacitance;
- n transformer ratio.

The open-loop transfer function ($OLT F_v$) is given by

$$OLT F_v(s) = Gv_{sf}(s) \cdot \frac{Kv_{sf}}{Ki_{sf}} \cdot Km_{sf} \quad (8)$$

where

phase input current, sinusoidal and balanced, the voltage loop transfer function is obtained through the method of power balance analysis.

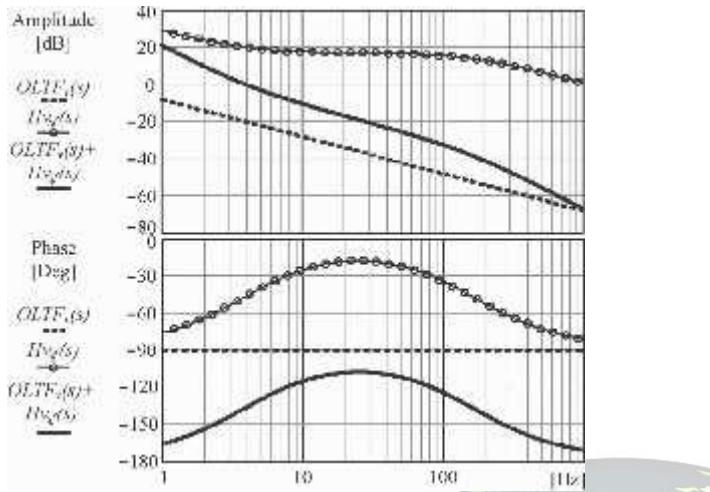


Fig. 11. Voltage loop frequency response of the SAF.

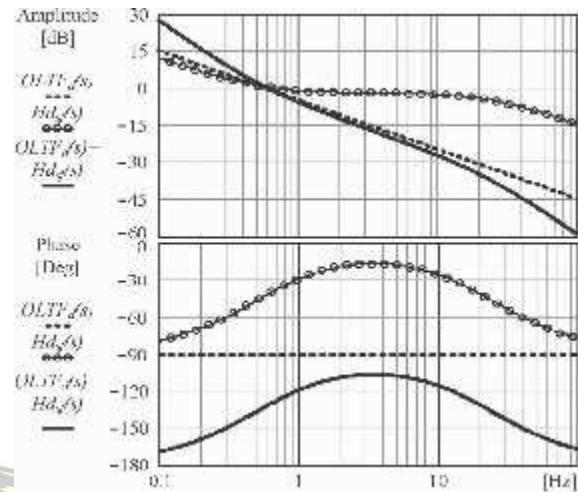


Fig. 13. Unbalanced-voltage loop frequency response of the SAF.

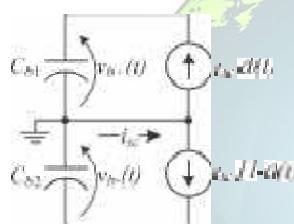


Fig. 12. Equivalent circuit of the SAF unbalanced-voltage loop.

Aiming to regulate the total dc link voltage control, a proportional integral (PI)+pole controller was designed, which ensures a crossover frequency of 4 Hz and a phase margin of 45°. The frequency response of the total voltage loop is shown in Fig. 11, including the open-loop transfer function ($OLT F_v$), controller transfer function (H_{vsf}), and compensated loop transfer function ($OLT F_v + H_{vsf}$).

The unbalanced-voltage control loop also has a low-frequency loop and acts on the dc level of the grid current reference in order to keep the voltage equilibrium in dc link capacitors. When a voltage unbalance occurs, this loop adds a dc level to the references of the grid currents, aiming to equalize both C_{L1} and C_{L2} voltages.

The unbalanced-voltage loop transfer function is obtained through the analysis of the simplified circuit shown in Fig. 12. The four-wire converter allows the single-phase analysis, where two current sources represent the current on the inverter switches. In Fig. 12, the current $i_{sc}(t)$ represents the current through the neutral point, and $d(t)$ represents the duty cycle.

Through the mesh analysis and by applying Laplace, the unbalanced-voltage loop transfer function is obtained and given by

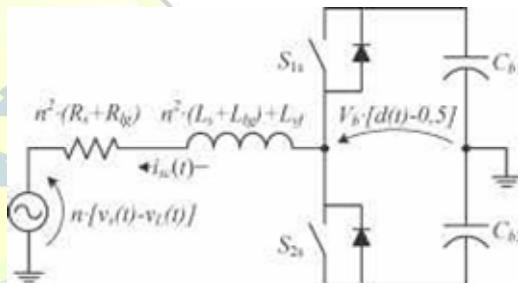


Fig. 14. Single-phase equivalent circuit of SAF.

where

Kd_{sf} differential voltage sensor gain.

Aiming to eliminate the differential dc link voltage, a PI+pole controller was designed, which ensures a crossover frequency of 0.5 Hz and a phase margin of 50°. The frequency response of the differential voltage loop is shown in Fig. 13, including the open-loop transfer function ($OLT F_d$), controller transfer function (H_{dsf}), and compensated loop transfer function ($OLT F_d + H_{dsf}$).

The current control scheme consists of three identical current loops, except for the 120° phase displacements from the references of each other. The current loops have a fast response to track the sinusoidal references, allowing the decoupling analysis in relation to the voltage loop. The current loop transfer function is obtained through the analysis of the single-phase equivalent circuit shown in Fig. 14.

The voltage source represents the voltage on the coupling transformer. The dynamic model is obtained through the circuit analysis using average values related to the switching period. Under these conditions, the voltages $v_s(t)$ and $v_L(t)$ are constants.

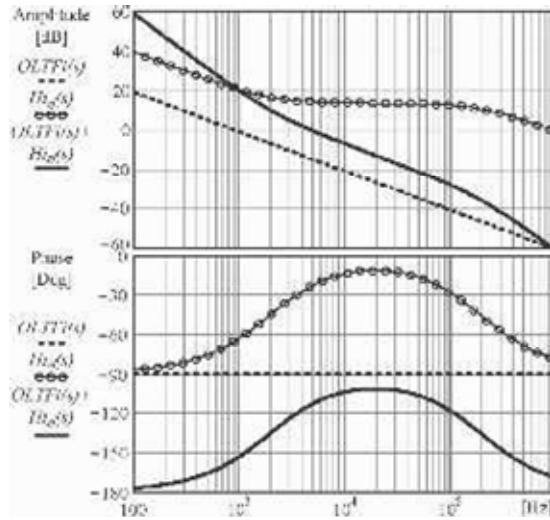


Fig. 15. Current loop frequency response of the SAF.

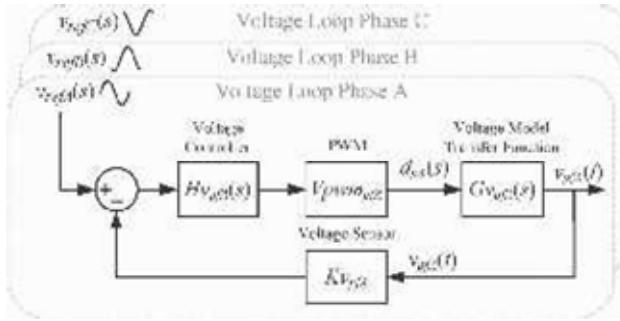


Fig. 16. Control block diagram of the PAF voltage loop.

and

L_s series grid inductance;

R_s series grid resistance;

L_{lg} leakage inductance of the coupling transformer;

R_{lg} series resistance of the coupling transformer.

The open-loop transfer function ($OLT\ F_i$) is given by

$$OLT\ F_i(s) = G_{sf}(s) \cdot K_{pwm\ sf} \cdot K_{i,sf} \quad (13)$$

where

$K_{pwm\ sf}$ series filter pulse width modulation (PWM) modulator gain.

The $K_{pwm\ sf}$ gain is equal to the inverse peak value of the triangular carrier.

Aiming to track the current reference, a PI+pole controller was designed, which ensures a crossover frequency of 5 kHz and a phase margin of 70°. The frequency response of the current loop is shown in Fig. 15, including the open-loop transfer function ($OLT\ F_i$), controller transfer function ($H_{i,sf}$), and compensated loop transfer function ($OLT\ F_i + H_{i,sf}$).

B. PAF Control

Fig. 16 shows the control block diagram of the shunt active filter controller.

The PAF control scheme is formed by three identical load voltage feedback loops, except for the 120° phase displace-

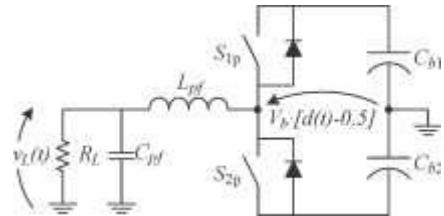


Fig. 17. Single-phase equivalent circuit of PAF.

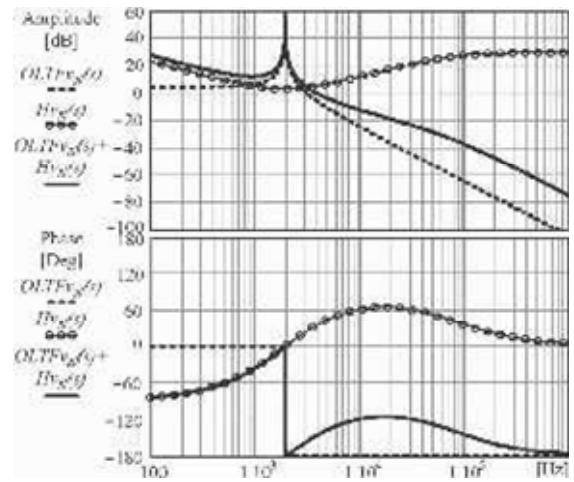


Fig. 18. Voltage loop frequency response of the SAF.

ments from the references of each other. The voltage loops are responsible for tracking the sinusoidal voltage reference for each load output phase in order to control the load voltages independently.

The voltage loop transfer function is obtained through the analysis of the single-phase equivalent circuit shown in Fig. 17. The dynamic model is obtained through the circuit analysis using average values related to the switching period. Through small signal analysis and by using Laplace, the voltage loop transfer function is given by

$$G_V(s) = \frac{V_b}{L_{pf}C_{pf}} \cdot \frac{1}{s^2 + s \cdot \frac{1}{C_{pf}R_L} + \frac{1}{L_{pf}C_{pf}}} \quad (14)$$

where $G_{pf}(s) = V_L(s)/D(s)$.

The open-loop transfer function ($OLT\ F v_{pf}$) is given by

$$OLT\ F v(s) = G_{pf}(s) \cdot K_{pwm\ pf} \cdot K_{v\ pf} \quad (15)$$

where

$K_{pwm\ pf}$ shunt filter PWM modulator gain.

Aiming to track the voltage reference, a proportional integral derivative (PID)+additional pole controller was designed, which ensures a crossover frequency of 4 kHz and a phase margin of 35°.

The voltage loop frequency response is shown in Fig. 18, including the open-loop transfer function ($OLT\ F v_{pf}$),

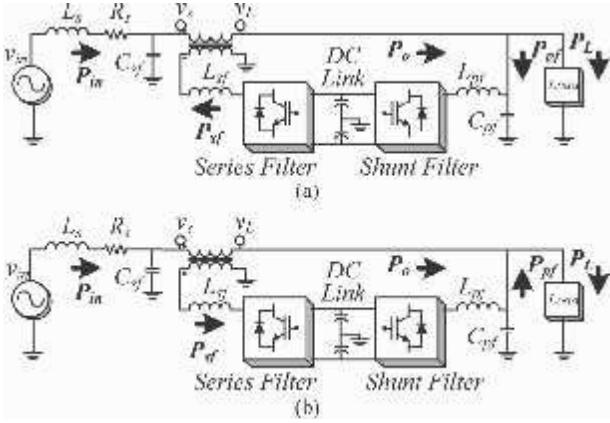


Fig. 19. Power flow of iUPQC. (a) $v_s < v_L$. (b) $v_s > v_L$.

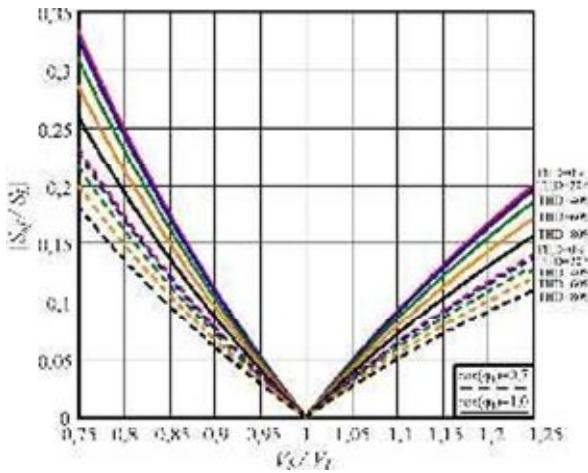


Fig. 20. Normalized apparent power of the SAF.

controller transfer function (Hv_{pf}), and compensated loop transfer function ($OLTF v_{pf} + Hv_{pf}$).

VI. POWER FLOW

The active power flow of the iUPQC is shown in Fig. 19. In Fig. 19(a), the grid voltage v_s has a lower amplitude than the load voltage v_L . In this case, the SAF delivers active power to the load, while the parallel active filter consumes active power. In Fig. 19(b), the grid voltage v_s has a higher amplitude than the load voltage v_L . In this case, the SAF consumes active power, while the PAF filter delivers active power to the load. In an ideal situation when v_s is equal to v_L , there is no active power flow through the SAF. The power drained from the electrical grid is equal to the sum of the load power and the iUPQC power losses.

In this paper, the output voltage v_L is kept in phase with the fundamental component of the input voltage v_{in} ; thus, the SAF operates with reactive power only when there are harmonics on the input voltage v_{in} because the fundamental component of the coupling transformer voltage is always in phase with the current drained from the utility grid i_s .

In steady state, assuming a sinusoidal and balanced utility grid voltage and disregarding the dual UPQC losses, the ap-

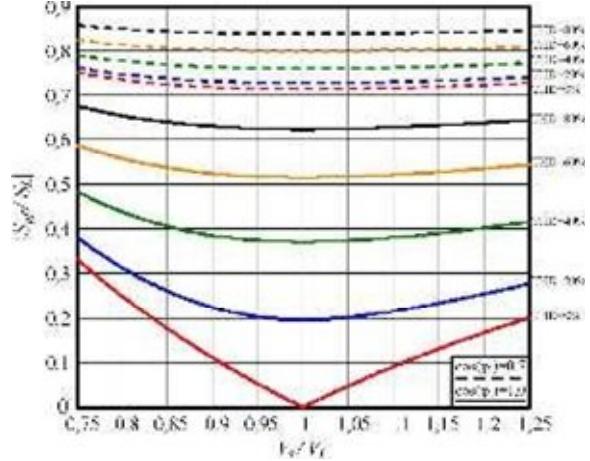


Fig. 21. Normalized apparent power of the PAF.

to the apparent power of the load are given by (16) and (17), respectively, represented in Figs. 20 and 21

$$\frac{S_{sf}}{S_L} = \frac{\cos(\phi_1) \cdot 1 - \frac{V_L}{V_S}^2}{1 + TDH i^2} \quad (16)$$

$$\frac{S_{pf}}{S_L} = \frac{\cos^2(\phi_1) \cdot \frac{V_L}{V_S} \cdot \frac{V_L}{V_S}^2}{1 + TDH i^2} + 1 \quad (17)$$

where $\cos(\phi_1)$ is the displacement factor and $TDH i^2$ is the total harmonic distortion of the output current.

These equations are obtained through the analysis of the complex power of SAF S_{sf} and PAF S_{pf}

$$\dot{S}_{sf} = (\dot{V}_s - \dot{V}_L) \cdot \dot{I}_s \quad (18)$$

□

$$\dot{S}_{Pf} = \dot{S}_L - \dot{V}_L \cdot \dot{I}^\square. \quad (19)$$

Increasing T_{HD} and decreasing η ratio will decrease

This analysis shows that it is possible to design a SAF with power capacity lower than the nominal load power. By changing the transformers ratio, it is possible to use power switches with lower current capacity. On the other hand, PAF is always designed for nominal load power since it has to process the total load reactive power.

VII EXPERIMENTAL RESULTS

A 2500-W prototype was built in order to obtain the experimental results for the proposed iUPQC. The prototype uses two back-to-back converters manufactured by SEMIKRON. The passive filters were designed according to the specifications of Table I. The prototype is shown in Fig. 22.

The precharge method and the precharge sequence are an important and not trivial design step of the iUPQC due to the power flow characteristics of the system. During the startup, the voltage supplied to the load cannot be distorted, and the iUPQC coupling in the circuit shall not affect the load. The precharge method developed allows the startup of the iUPQC with no need of load power disconnection. The used precharge sequence is shown in Fig. 23. The precharge circuit has three

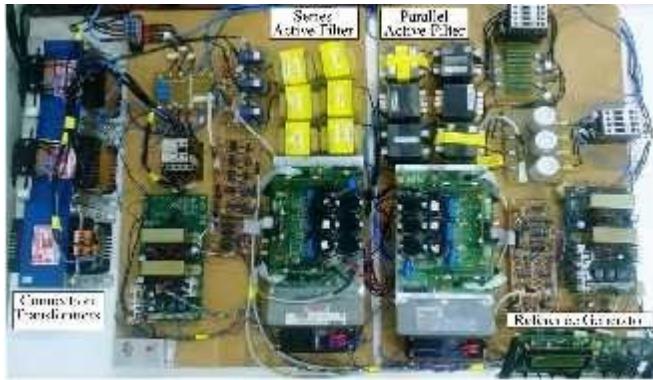


Fig. 22. Dual UPQC prototype.

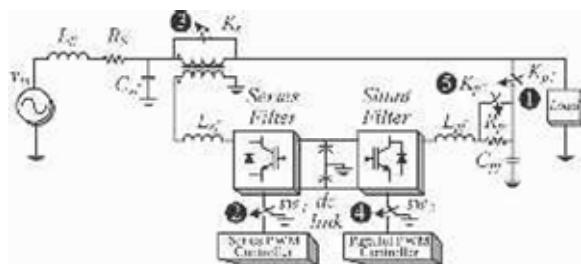
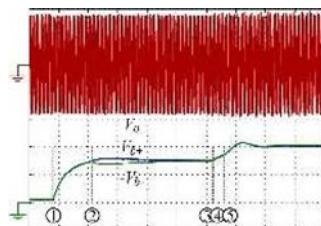


Fig. 23. Precharge sequence of the iUPQC.



VIII. CONCLUSION

In order to emulate a harmonic distorted load current, a three-phase rectifier with capacitive filter and two single-phase rectifiers with RL load connected to phases A and B, respectively, was used.

In order to emulate a distorted grid voltage and to evaluate the harmonic compensation of the grid voltage, a FCATH 450-38-50 programmable ac power source manufactured by SUPPLIER Inc. was used. The power source supplies a three-phase voltage source with 20% of the third harmonic in phase A, 10% of the fifth harmonic in phase B, and 10% of the seventh harmonic in phase C.

Fig. 25(a) shows the currents and voltages in the source and load. It is possible to see that the currents drained from the source are sinusoidal, balanced, and synchronized with the source voltage, with power factors of 0.980, 0.994, and 0.994 for phases A, B, and C, respectively. The THDs of the load currents are 32.1%, 32.1%, and 65.1%, respectively, while the THDs of the source currents are 1.06%, 1.80%, and 1.34%. The THDs of the source voltage are equal to 20.0%, 10.8%, and 10.4% for phases A, B, and C, respectively, while the load voltages have THDs equal to 0.53%, 0.69%, and 0.38%, respectively.

Fig. 25(b) shows the currents through the PAF. The PAF indirectly supplies the load harmonic currents because the SAF only drains the fundamental current component from the source.

In a similar way, Fig. 25(c) shows the voltages synthesized by the SAF. The SAF indirectly processes the harmonic grid voltages because the PAF imposes a synchronized sinusoidal voltage on the load.

In order to verify the dynamic response of the iUPQC, Fig. 26(a) shows the source and load voltages during a voltage interruption in phase A. Fig. 26(b) shows the source currents during a fault in phase A. It is possible to see that the source currents in the other phases have the amplitudes increased in order to keep the nominal power of the load.

Fig. 26(c) shows the load voltages and the load currents during a load step from 50% to 100%. The load voltages and the load currents are shown in Fig. 26(d) during a load step from 100% to 50%.

Fig. 26(e) shows the dc link voltages and the load current in phase A during a load step. The voltages in capacitors C_{L1} and C_{L2} remained balanced even during the load steps.

The experimental results confirm the efficacy of the proposed scheme to control the iUPQC.

The results obtained with the iUPQC confirms that the proposed ABC reference frame control works very well and that it was able to compensate the nonlinear load currents and also ensure the sinusoidal voltage for the load in all three phases. The control also had a great performance during the load steps and voltage disturbances at the source.

The main advantages of this proposed control in relation to the other proposed schemes were the utilization of sinusoidal references for both series and shunt active filter

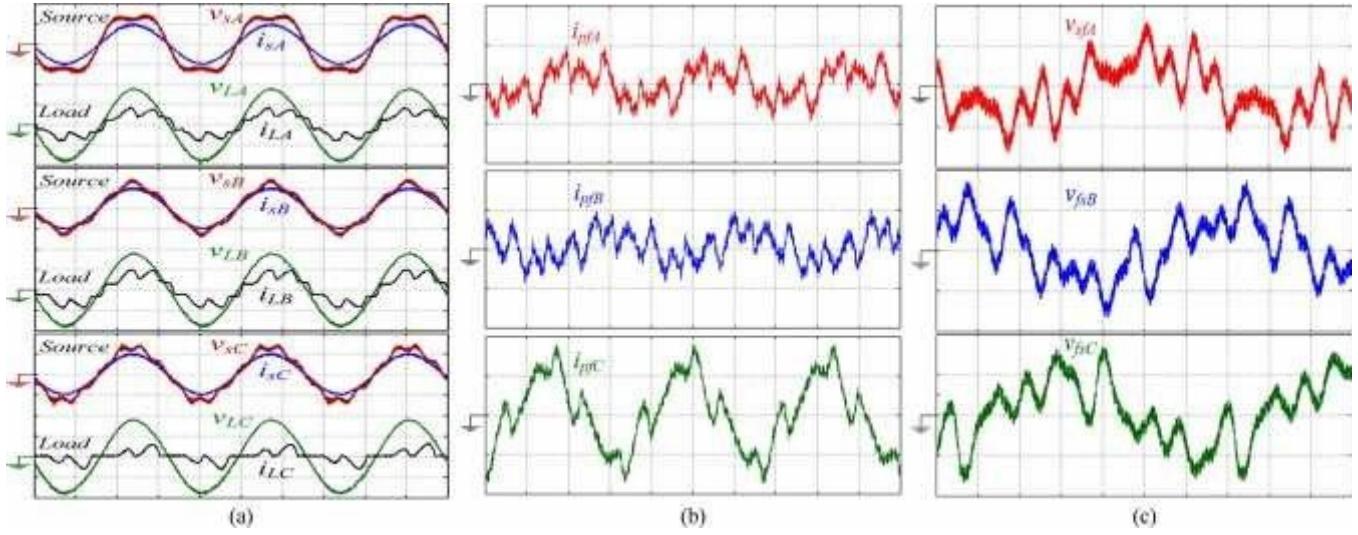


Fig. 25. (a) Source and load voltages (100 V/div and 5 ms/div), and source and load currents (10 A/div and 5 ms/div). (b) PAF currents (6 A/div and 5 ms/div). (c) SAF voltages (30 V/div and 2.5 ms/div).

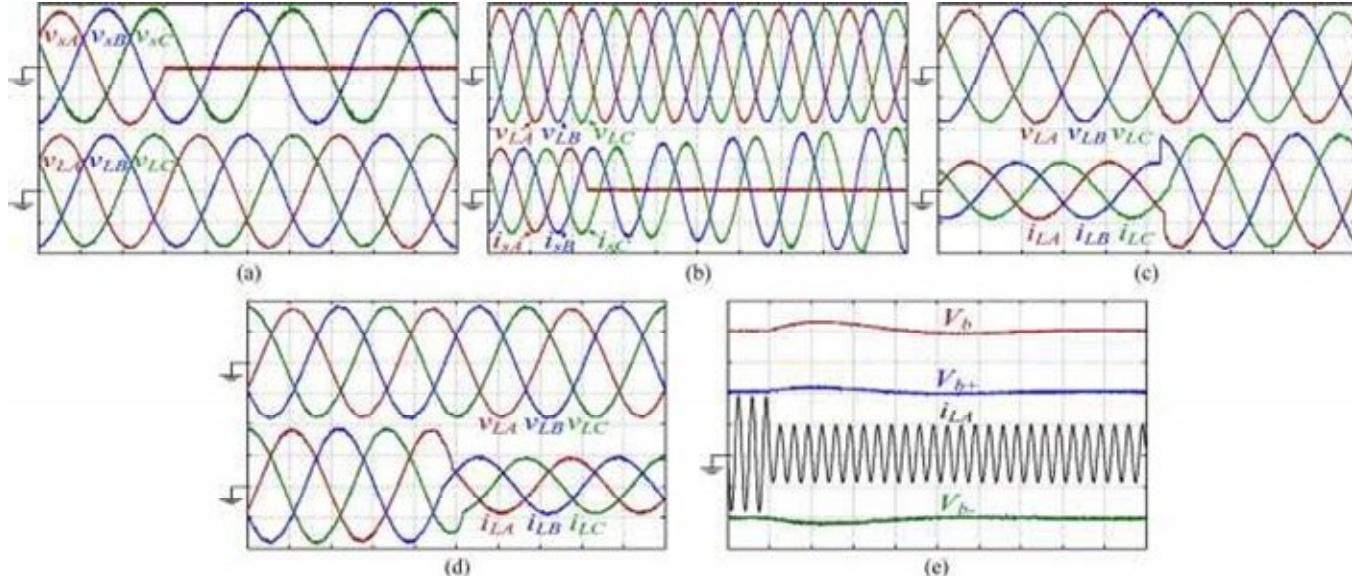


Fig. 26. (a) Source voltages and load voltages (100 V/div and 5 ms/div) during a voltage dip in phase A. (b) Load voltages (100 V/div and 10 ms/div) and source currents (5 A/div and 10 ms/div). (c) Load voltages (100 V/div and 5 ms/div) and load currents (5 A/div and 5 ms/div) during a load step from 50% to 100%. (d) Load voltages (100 V/div and 5 ms/div) and load currents (5 A/div and 5 ms/div) during a load step from 100% to 50%. (e) DC link voltages (100 V/div and 50 ms/div) and load current (5 A/div and 50 ms/div) during a load step from 100% to 50%.

controls without the need for complex calculations or coordinate transformations.

The iUPQC references do not have harmonic contents, and the only requirement is the synchronism with the grid voltage. Another positive aspect of the iUPQC in low-voltage applications (distribution system network) is the noninterference of the leakage impedance voltage of the SAF connection transformer in the load voltage compensation because the load voltage is directly controlled by the PAF. On the other hand, the leakage impedance interferes in the current loop bandwidth, decreasing its frequency response under distorted grid voltages.

The results validate the proposed iUPQC control scheme, proving that the power quality can be meaningfully better with a simple control method which uses only synchronized sinusoidal references.

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