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Single Phase Fifteen Level Inverter using seven switches for Industrial Applications

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***Abstract*—This paper proposes a new solar power generation system, which is composed of a dc/dc power converter and a new seven-level inverter. The dc/dc power converter integrates a dc–dc boost converter and a transformer to convert the output voltage of the solar cell array into two independent voltage sources with mul- tiple relationships. This new seven-level inverter is configured using a capacitor selection circuit and a full-bridge power converter, con- nected in cascade. The capacitor selection circuit converts the two output voltage sources of dc–dc power converter into a three-level dc voltage, and the full-bridge power converter further converts this three-level dc voltage into a seven-level ac voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility. The salient features of the proposed seven-level inverter are that only six power electronic switches are used, and only one power electronic switch is switched at high frequency at any time. A prototype is developed and tested to verify the performance of this proposed solar power generation system.**

***Index Terms*—Grid-connected, multilevel inverter, pulse-width modulated (PWM)inverter.**

I. INTRODUCTION

THE extensive use of fossil fuels has resulted inthe global problem of greenhouse emissions. Moreover, as the supplies of fossil fuels are depleted in the future, they will become increasingly expensive. Thus, solar energy is becoming more important since it produces less pollution and the cost of fossil fuel energy is rising, while the cost of solar arrays is decreasing. In particular, small-capacity distributed power generation systems using solar energy may be widely used in residential applications in the near future [1],[2].

The power conversion interface is important to grid-connected solar power generation systems because it converts the dc power generated by a solar cell array into ac power and feeds this ac power into the utility grid. An inverter is necessary in the power conversion interface to convert the dc power to ac power [2]–[4]. Since the output voltage of a solar cell array is low, a dc–dc power converter is used in a small-capacity solar power generation system to boost the output voltage, so it can match the dc bus voltage of the inverter. Efficiency of the power conversion interface is important to in- sure that there is no waste of the energy generated by the solar cell array. The active devices and passive devices in the inverter produce a power loss. The power losses due to active devices include both conduction losses and switching losses [5]. Con- duction loss results from the use of active devices, while the switching loss is proportional to the voltage and the current changes for each switching and switching frequency. A filter in- ductor is used to process the switching harmonics of an inverter, so the power loss is proportional to the amount of switching harmonics.

The voltage change in each switching operation for a multilevel inverter is reduced in order to improve its power conversion efficiency [6]–[15] and the switching stress of the active devices. The amount of switching harmonics is also attenuated, so the power loss caused by the filter inductor is also reduced. Therefore, multilevel inverter technology has been the subject of much research over the past few years. In theory, multilevel inverters should be designed with higher voltage levels in order to improve the conversion efficiency and to reduce harmonic content and electromagnetic interference (EMI).

Conventional multilevel inverter topologies include the diode-clamped [6]–[10], the flying-capacitor [11]–[13], and the cascade H-bridge [14]–[18] types. Diode-clamped and flying-capacitor multilevel inverters use capacitors to develop several voltage levels. But it is difficult to regulate the voltage of these capacitors. Since it is difficult to create an asymmetric voltage technology in both the diode-clamped and the flying-capacitor topologies, the power circuit is complicated by the increase in the voltage levels that is necessary for a multilevel inverter. For a single-phase seven-level inverter, 12 power electronic switches are required in both the diode-clamped and the flying-capacitor topologies. Asymmetric voltage technology is used in the cascade H-bridge multilevel inverter to allow more levels of output voltage [17], so the cascade H-bridge multilevel inverter is suitable for applications with increased voltage levels. Two H-bridge inverters with a dc bus voltage of multiple relationships can be connected in cascade to produce a single-phase seven-level inverter and eight power electronic switches are used. More recently, various novel topologies for seven-

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level inverters have been proposed. For example, a single-phase seven-level grid-connected inverter has been developed for a photovoltaic system [18]. This seven-level grid-connected in- verter contains six power electronic switches. However, three dc capacitors are used to construct the three voltage levels, which results in that balancing the voltages of the capacitors is more complex. In [19], a seven-level inverter topology, con- figured by a level generation part and a polarity generation

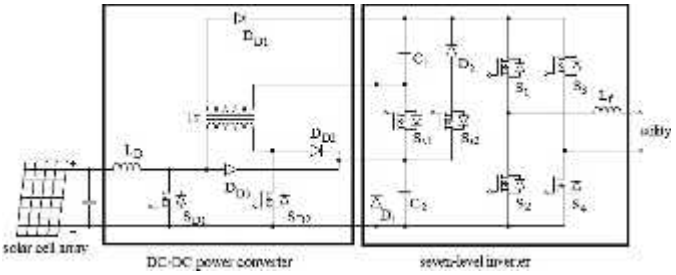

Fig. 1. Configuration of the proposed solar power generation system.

part, is proposed. There, only power electronic switches of the level generation part switch in high frequency, but ten power electronic switches and three dc capacitors are used. In [20], a modular multilevel inverter with a new modulation method is applied to the photovoltaic grid-connected generator. The modular multilevel inverter is similar to the cascade H-bridge type. For this, a new modulation method is proposed to achieve dynamic capacitor voltage balance. In [21], a multilevel dc-link inverter is presented to overcome the problem of partial shading of individual photovoltaic sources that are connected in series. The dc bus of a full-bridge inverter is configured by several individual dc blocks, where each dc block is composed of a solar cell, a power electronic switch, and a diode. Controlling the power electronics of the dc blocks will result in a multilevel dc-link voltage to supply a full-bridge inverter and to simultaneously overcome the problems of partial shading of individual photovoltaic sources.

This paper proposes a new solar power generation system. The proposed solar power generation system is composed of a dc/dc power converter and a seven-level inverter. The seven-level inverter is configured using a capacitor selection circuit and a full-bridge power converter, connected in cascade. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Since only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage, the switching power loss is reduced, and the power efficiency is improved. The inductance of the filter inductor is also reduced because there is a seven-level output voltage. In this study, a prototype is developed and tested to verify the performance of the proposed solar power generation system.

II. Circuit Configuration

Fig. 1 shows the configuration of the proposed solar power generation system. The proposed solar power generation system is composed of a solar cell array, a dc–dc power converter, and a new seven-level inverter. The solar cell array is connected to the dc–dc power converter, and the dc–dc power converter is a boost converter that incorporates a transformer with a turn ratio of 2:1. The dc–dc power converter converts the output power of multiple relationships, which are supplied to the seven-level inverter. This new seven-level inverter is composed of a capacitor

the solar cell array into two independent voltage sources with circuit determine the discharge of the two capacitors while the two capacitors are being discharged individually or in se- ries. Because of the multiple relationships between the voltages of the dc capacitors, the capacitor selection circuit outputs a three-level dc voltage. The full-bridge power converter further converts this three-level dc voltage to a seven-level ac voltage that is synchronized with the utility voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility, which produces a unity power factor. As can be seen, this new seven-level inverter contains only six power electronic switches, so the power circuit is simplified.

III. DC–DC Power Converter

As seen in Fig. 1, the DC–DC power converter incorporates a boost converter and a current-fed forward converter. The boost converter is composed of an inductor L_D , a power electronic switch S_{D1} , and a diode, D_{D3} . The boost converter charges capacitor C_2 of the seven-level inverter. The current-fed forward converter is composed of an inductor L_D , power electronic switches S_{D1} and S_{D2} , a transformer, and diodes D_{D1} and D_{D2} . The current-fed forward converter charges capacitor C_1 of the seven-level inverter. The inductor L_D and the power electronic switch S_{D1} of the current-fed forward converter are also used in the boost converter.

Fig. 2(a) shows the operating circuit of the dc–dc power converter when S_{D1} is turned ON. The solar cell array supplies energy to the inductor L_D . When S_{D1} is turned OFF and S_{D2} is turned ON, its operating circuit is shown in Fig. 2(b). Accordingly, capacitor C_1 is connected to capacitor C_2 in parallel through the transformer, so the energy of inductor L_D and the solar cell array charge capacitor C_2 through D_{D3} and charge capacitor C_1 through the transformer and D_{D1} during the off-state of S_{D1} . Since capacitors $C1$ and $C2$ are charged in parallel by using the transformer, the voltage ratio of capacitors C_1 and C_2 is the same as the turn ratio (2:1) of the transformer. Therefore, the voltages of C_1 and C_2 have multiple relationships. The boost converter is operated in the continuous conduction mode (CCM). The voltage of C_2 can be represented as

$$V_{c2} = \frac{1}{1 - D} V_s \qquad (1)$$

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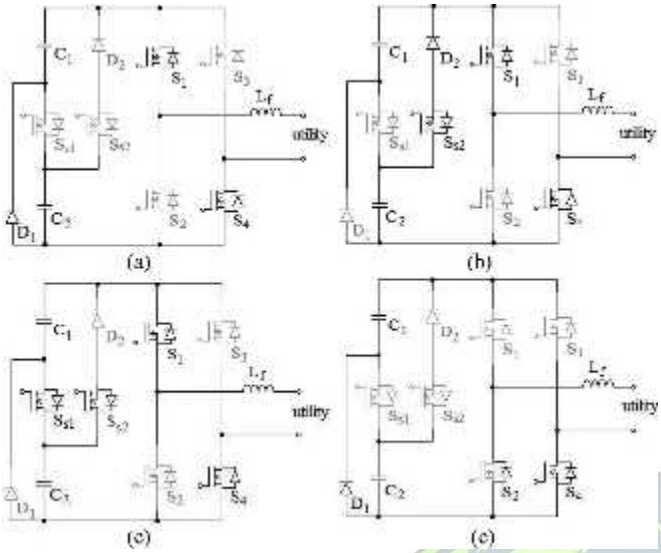

Fig. 3. Operation of the seven-level inverter in the positive half cycle, (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

represented as

$$V_{c1} = \frac{1}{2(1-D)} V_s . \quad (2)$$

Mode 1: The operation of mode 1 is shown in Fig. 3(a). Both S_{S1} and S_{S2} of the capacitor selection circuit are OFF, so C_1 is discharged through D_1 and the output voltage of the capacitor selection circuit is $V_{dc}/3$. S_1 and S_4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is $V_{dc}/3$.

Mode 2: The operation of mode 2 is shown in Fig. 3(b). In the capacitor selection circuit, S_{S1} is OFF and S_{S2} is ON, so C_2 is discharged through S_{S2} and D_2 and the output voltage of the capacitor selection circuit is $2V_{dc}/3$. S_1 and S_4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is $2V_{dc}/3$.

Mode 3: The operation of mode 3 is shown in Fig. 3(c). In the capacitor selection circuit, S_{S1} is ON. Since D_2 has a reverse bias when S_{S1} is ON, the state of S_{S2} cannot affect the current flow. Therefore, S_{S2} may be ON or OFF, to avoiding switching of S_{S2}. Both C_1 and C_2 are discharged in series and the output voltage of the capacitor selection circuit is V_{dc}. S_1 and S_4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is V_{dc}.

Mode 4: The operation of mode 4 is shown in Fig. 3(d). Both S_{S1} and S_{S2} of the capacitor selection circuit are OFF.

The output voltage of the capacitor selection circuit is $V_{dc}/3$.

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It should be noted that the current of the magnetizing induc- tance of the transformer increases when S_{D2} is in the ON state. Conventionally, the forward converter needs a third demagne- tizing winding in order to release the energy stored in the mag- netizing inductance back to the power source. However, in the proposed dc–dc power converter, the energy stored in the mag- netizing inductance is delivered to capacitor C_2 through D_{D2} and S_{D1} when S_{D2} is turned OFF. Since the energy stored in the magnetizing inductance is transferred forward to the output capacitor C_2 and not back to the dc source, the power effi- ciency is improved. In addition, the power circuit is simplified because the charging circuits for capacitors C_1 and C_2 are in- tegrated. Capacitors C_1 and C_2 are charged in parallel by using the transformer, so their voltages automatically have multiple relationships. The control circuit is also simplified.

IV. Seven-Level Inverter

As seen in Fig. 1, the seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, which are connected in cascade. The operation of the seven- level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the power electronic switches and diodes are assumed to be ideal, while the voltages of both capacitors C_1 and C_2 in the capacitor selection circuit are constant and equal to $V_{dc}/3$ and $2V_{dc}/3$, respectively. Since the output current of the solar power generation system will be controlled to be sinusoidal and in phase with the utility voltage, the output current of the seven-level inverter is also positive in the positive half cycle of the utility. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes, as shown in Fig. 3. Only S_4 of the full-bridge power converter is ON. Since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the antiparallel diode of S_2 to be switched ON for continuous conduction of the filter inductor current. At this point, the output voltage of the seven- level inverter is zero.

Therefore, in the positive half cycle, the output voltage of the seven-level inverter has four levels: V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, and 0.

In the negative half cycle, the output current of the seven-level inverter is negative. The operation of the seven-level inverter can also be further divided into four modes, as shown in Fig. 4. A comparison with Fig. 3 shows that the operation of the capacitor selection circuit in the negative half cycle is the same as that in the positive half cycle. The difference is that S_2 and S_3 of the full-bridge power converter are ON during modes 5, 6, and 7, and S_2 is also ON during mode 8 of the negative half cycle. Accordingly, the output voltage of the capacitor selection circuit is inverted by the full-bridge power converter, so the output voltage of the seven-level inverter also has four levels: $-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, and 0.

In summary, the output voltage of the seven-level inverter has the voltage levels: V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, and $-V_{dc}$.

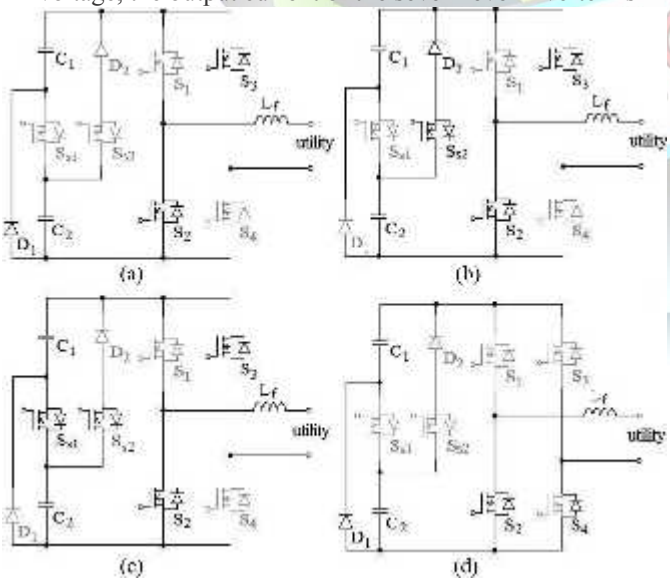
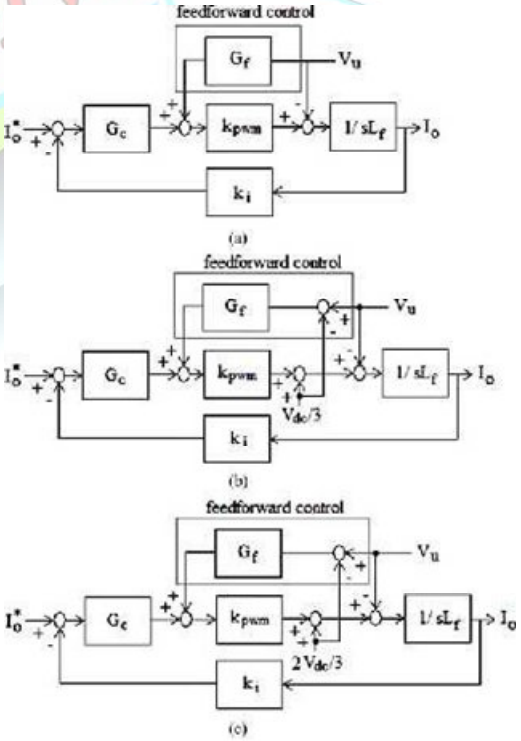


Fig. 4. Operation of the seven-level inverter in the negative half cycle: (a) mode 5, (b) mode 6, (c) mode 7, and (d) mode 8.

inverter can be controlled to trace a reference current. Accordingly, the output voltage of the seven-level inverter must be



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changed in accordance with the utility voltage.

In the positive half cycle, when the utility voltage is smaller than $V_{dc}/3$, the seven-level inverter must be switched between modes 1 and 4 to output a voltage of $V_{dc}/3$ or 0. Within this voltage range, S_1 is switched in PWM. The duty ratio d of S_1 can be represented as

$$d = v_m / V_{tri} \quad (3)$$

where v_m and V_{tri} are the modulation signal and the amplitude of carrier signal in the PWM circuit, respectively. The output voltage of the seven-level inverter can be written as

$$v_o = d \cdot V_{dc}/3 = k_{pwm} v_m \quad (4)$$

where k_{pwm} is the gain of inverter, which can be written as

$$k_{pwm} = V_{dc}/3V_{tri}. \quad (5)$$

Fig. 5(a) shows the simplified model for the seven-level inverter when the utility voltage is smaller than $V_{dc}/3$. The closed-loop transfer function can be derived as

$$I_o = \frac{k_{pwm} G_c/L_f}{s + k_i k_{pwm} G_c/L_f} I_o - \frac{1/L_f}{s + k_i k_{pwm} G_c/L_f} V_u \quad (6)$$

where G_c is the current controller and k_i is the gain of the current detector.

The seven-level inverter is switched between modes 2 and 1, in order to output a voltage of $2V_{dc}/3$ or $V_{dc}/3$ when the utility voltage is in the range $(V_{dc}/3, 2V_{dc}/3)$. Within this voltage range, S_{S2} is switched in PWM. The duty ratio of S_{S2} is the same as (3). However, the output voltage of seven-level inverter can be written as

$$v_o = d \cdot V_{dc}/3 + V_{dc}/3 = k_{pwm} v_m + V_{dc}/3. \quad (7)$$

The closed-loop transfer function can be derived as

$$I_o = \frac{k_{pwm} G_c/L_f}{s + k_i k_{pwm} G_c/L_f} I_o - \frac{1/L_f}{s + k_i k_{pwm} G_c/L_f} (V_u - V_{dc}/3). \quad (8)$$

The seven-level inverter is switched between modes 3 and 2 in order to output a voltage of V_{dc} or $2V_{dc}/3$, when the utility voltage is in the range $(2V_{dc}/3, V_{dc})$. Within this voltage range, S_{S1} is switched in PWM and S_{S2} remains in the ON state to avoid switching of S_{S2}. The duty ratio of S_{S1} is the same as (3). However, the output voltage of seven-level inverter can be written as

$$v_o = d \cdot V_{dc}/3 + 2V_{dc}/3 = k_{pwm} v_m + 2V_{dc}/3. \quad (9)$$

Fig. 5(c) shows the simplified model for the seven-level inverter when the utility voltage is within this voltage range. The closed-loop transfer function can be derived as

$$I_o = \frac{k_{pwm} G_c/L_f}{s + k_i k_{pwm} G_c/L_f} I_o - \frac{1/L_f}{s + k_i k_{pwm} G_c/L_f} (V_u - 2V_{dc}/3). \quad (10)$$

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TABLE I
STATES OF POWER ELECTRONIC SWITCHES FOR A SEVEN-LEVEL INVERTER

	S_{S1}	S_{S2}	S_1	S_2	S_3	S_4
positive half cycle						
$\|v_u\| < V_{dc}/3$	off	off	PWM	off	off	on
$2V_{dc}/3 > \|v_u\| > V_{dc}/3$	off	PWM	on	off	off	on
$\|v_u\| > 2V_{dc}/3$	PWM	on	on	off	off	on
negative half cycle						
$\|v_u\| < V_{dc}/3$	off	off	off	on	PWM	off
$2V_{dc}/3 > \|v_u\| > V_{dc}/3$	off	PWM	off	on	on	off
$\|v_u\| > 2V_{dc}/3$	PWM	on	off	on	on	off

As seen in (6), (8), and (10), the second term is the disturbance. Hence, a feedforward control, which is also shown in Fig. 5, should be used to eliminate the disturbance, and the gain G_f should be $1/k_{pwm}$.

In the negative half cycle, the seven-level inverter is switched between modes 5 and 8, in order to output a voltage of $-V_{dc}/3$ or 0, when the absolute value of the utility voltage is smaller than $V_{dc}/3$. Accordingly, S_3 is switched in PWM. The seven-level inverter is switched in modes 6 and 5 to output a voltage of $-2V_{dc}/3$ or $-V_{dc}/3$ when the utility voltage is in the range $(-V_{dc}/3, -2V_{dc}/3)$. Within this voltage range, S_{S2} is switched in PWM. The seven-level inverter is switched in modes 7 and 6 to output a voltage of $-V_{dc}$ or $-2V_{dc}/3$, when the utility voltage is in the range $(-2V_{dc}/3, -V_{dc})$. At this voltage range, S_{S1} is switched in PWM and S_{S2} remains in the ON state to avoid switching of S_{S2}. The simplified model for the seven-level inverter in the negative half cycle is the similar to that for the positive half cycle.

Since only six power electronic switches are used in the proposed seven-level inverter, the power circuit is significantly simplified compared with a conventional seven-level inverter. The states of the power electronic switches of the seven-level inverter, as detailed previously, are summarized in Table I. It can be seen that only one power electronic switch is switched in PWM within each voltage range and the change in the output voltage of the seven-level inverter for each switching operation is $V_{dc}/3$, so switching power loss is reduced. Figs. 3 and 4 show that only three semiconductor devices are conducting in series in modes 1, 3, 4, 5, 7, and 8 and four semiconductor devices are conducting in series in modes 2 and 6. This is superior to the conventional multi-level inverter topologies, in which at least four semiconductor devices are conducting in series. Therefore, the conduction loss of the proposed seven-level inverter is also reduced slightly. The drawback of the proposed seven-level inverter is that the voltage rating of the full-bridge converter is higher than that of conventional multilevel inverter topologies.

The leakage current is an important parameter in a solar power generation system for transformerless operation. The leakage current is dependent on the parasitic capacitance and the negative terminal voltage of the solar cell array respect to ground [22], [23]. To reduce the leakage current, the filter inductor L_f should be replaced by a symmetric topology and the

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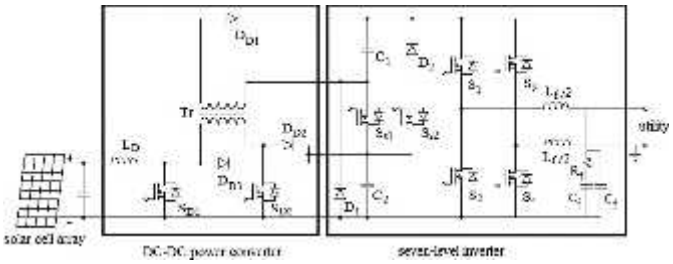

Fig. 6. Configuration of the proposed solar power generation system for suppressing the leakage current.

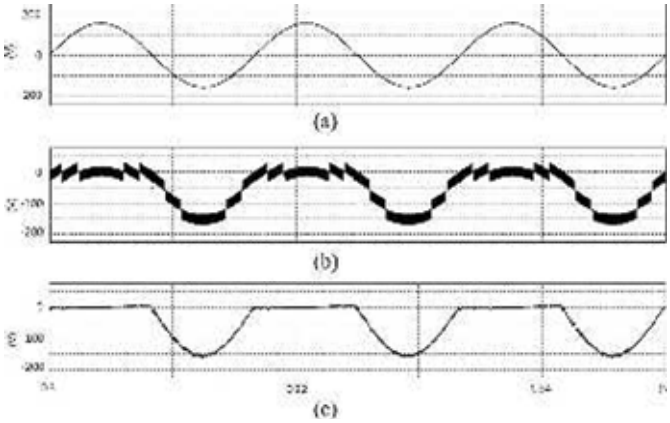

Fig. 7. Simulation results of the proposed solar power generation system: (a) utility voltage, (b) negative terminal voltage for adding the symmetric filter in- ductor, and (c) negative terminal voltage for adding the symmetric filter inductor and the extra filter C_f–R_f–C_f.

solar power generation system is redrawn as Fig. 6. Fig. 7 shows the simulation results of the proposed solar power generation system. Fig. 7(b) is the negative terminal voltage of the solar cell array for the seven-level inverter with the symmetric filter inductor of 0.95 mH. As seen in Fig. 7(b), this voltage contains a high-frequency ripple. The peak-to-peak value of the high- frequency ripple is about 30 V, which is much smaller than that of a full-bridge inverter with unipolar switching [22], [23]. This high-frequency ripple will result in a leakage current of solar cell array. If the leakage current of solar cell array is too high to be accepted, an extra filter C_f–R_f–C_f, as shown in Fig. 6, can be added. Since the switching of S_4 is synchronized with the utility voltage, the extra filter C_f–R_f–C_f is only added in the power-electronic leg (S_1, S_2). Fig. 7(c) shows the negative terminal voltage of a solar cell array for the seven-level inverter with the symmetric filter inductor and the extra filter C_f–R_f–C_f of 1 μF–25 Ω–1 μF. As seen in Fig. 7(c), the high-frequency ripple is attenuated effectively, so the leakage current can be further reduced.

V. Control Block

The proposed solar power generation system consists of a dc– dc power converter and a seven-level inverter. The seven-level inverter converts the dc power into high quality ac power and feeds it into the utility and regulates the voltages of capacitors C_1 and C_2 . The dc–dc power converter supplies two independent

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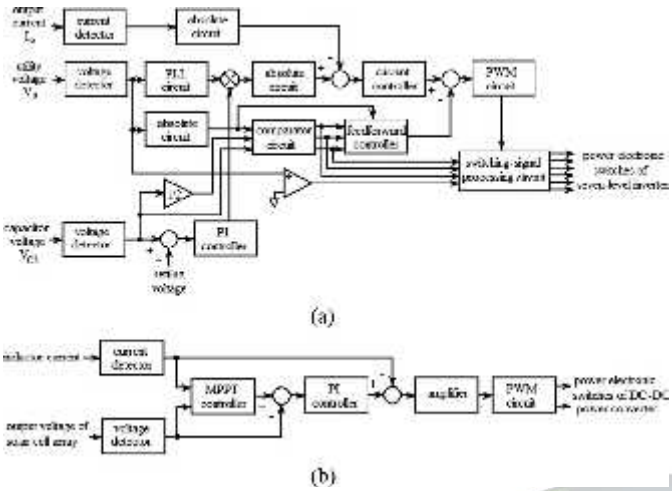

Fig. 8. Control block: (a) seven-level inverter and (b) dc–dc power converter.

voltage sources with multiple relationships and performs maximum power point tracking (MPPT) in order to extract the maximum output power from the solar cell array.

A. Seven-Level Inverter

Fig. 8(a) shows the control block diagram for the seven-level inverter. The control object of the seven-level inverter is its output current, which should be sinusoidal and in phase with the utility voltage. The utility voltage is detected by a voltage detector, and then sent to a phase-lock loop (PLL) circuit in order to generate a sinusoidal signal with unity amplitude. The voltage of capacitor C_2 is detected and then compared with a setting voltage. The compared result is sent to a PI controller. Then, the outputs of the PLL circuit and the PI controller are sent to a multiplier to produce the reference signal, while the output current of the seven-level inverter is detected by a current detector. The reference signal and the detected output current are sent to absolute circuits and then sent to a subtractor, and the output of the subtractor is sent to a current controller. The detected utility voltage is also sent to an absolute circuit and then sent to a comparator circuit, where the absolute utility voltage is compared with both half and whole of the detected voltage of capacitor C_2 , in order to determine the range of the operating voltage. The comparator circuit has three output signals, which correspond to the operation voltage ranges, (0, V_{dc} /3), (V_{dc} /3, 2V_{dc} /3), and (2V_{dc} /3, V_{dc}). The feed-forward control eliminates the disturbances of the utility voltage, V_{dc} /3 and 2V_{dc} /3, as shown in (6), (8), and (10). The absolute value of the utility voltage and the outputs of the compared circuit are sent to a feed-forward controller to generate the feed-forward signal. Then, the output of the current controller and the feed-forward signal are summed and sent to a PWM circuit to produce the PWM signal. The detected utility voltage is also compared with zero, in order to obtain a square signal that is synchronized with the utility voltage. Finally, the PWM signal, the square signal, and the outputs of the compared circuit are sent to the switching-signal processing circuit to generate the control signals for the

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power electronic switches of the seven-level inverter, according to Table I.

The current controller controls the output current of the seven- level inverter, which is a sinusoidal signal of 60 Hz. Since the feed-forward control is used in the control circuit, the current controller can be a simple amplifier, which gives good tracking performance. As can be seen in (6), (8), and (10), the gain of the current controller determines the bandwidth and the steady- state error. The gain of the current controller must be as large as possible in order to ensure a fast response and a low steady-state error. But the gain of the current controller is limited because the bandwidth of the power converter is limited by the switching frequency.

B. DC–DC Power Converter

Fig. 8(b) shows the control block diagram for the dc–dc power converter. The input for the DC-DC power converter is the out- put of the solar cell array. A ripple voltage with a frequency that is double that of the utility appears in the voltages of C_1 and C_2 , when the seven-level inverter feeds real power into the utility. The MPPT function is degraded if the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltages in C_1 and C_2 must be blocked by the dc–dc power converter to provide improved MPPT. Accordingly, dual control loops, an outer voltage control loop and an inner current control loop, are used to control the dc–dc power converter. Since the output volt- ages of the DC-DC power converter comprises the voltages of C_1 and C_2 , which are controlled by the seven-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop controls the inductor current so that it approaches a constant current and blocks the ripple voltages in C_1 and C_2 . The perturbation and observation method is used to provide MPPT [24]. The output voltage of the solar cell array and the inductor current are de- tected and sent to a MPPT controller to determine the desired output voltage for the solar cell array. Then the detected output voltage and the desired output voltage of the solar cell array are sent to a subtractor and the difference is sent to a PI controller. The output of the PI controller is the reference signal of the in- ner current control loop. The reference signal and the detected inductor current are sent to a subtractor and the difference is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The PWM circuit generates a set of complementary signals that control the power electronic switches of the dc–dc power converter.

VI. Experimental Results

To verify the performance of the proposed solar power gener- ation system, a prototype was developed with a controller based on the DSP chip TMS320F28035. The power rating of the pro- totype is 500 W, and the prototype was used for a single-phase utility with 110 V and 60 Hz. Table II shows the main parameters of the prototype.

Figs. 9 and 10 show the experimental results for the seven-level inverter when the output power of solar power generation system is 500 W. Fig. 9 shows the experimental results for the

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TABLE II
PARAMETERS OF THE PROTOTYPE

DC-DC power converter	
input voltage	70V
inductor	1mH
PWM frequency	15360Hz
seven-level inverter	
capacitor C_1, C_2	1000μF
filter inductor	1.9 mH
PWM frequency	15360Hz

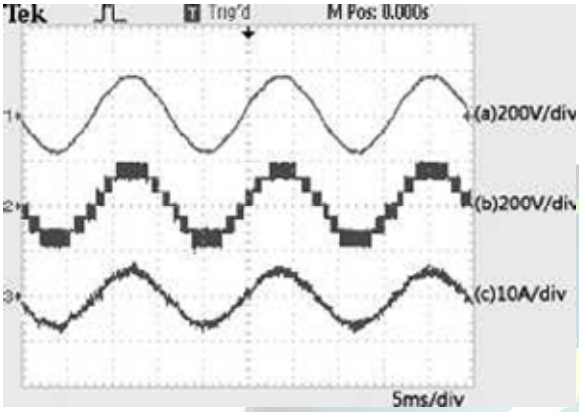

Fig. 9. Experimental results for the ac side of the seven-level inverter: (a) utility voltage, (b) output voltage of seven-level inverter, and (c) output current of the seven-level inverter.

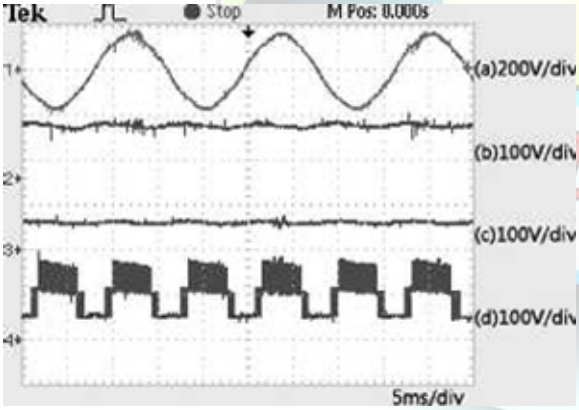

Fig. 10. Experimental results for the dc side of the seven-level inverter: (a) utility voltage, (b) voltage of capacitor C2, (c) voltage of capacitor C1, and (d) output voltage of the capacitor selection circuit.

AC side of the seven-level inverter. Fig. 9(b) shows that the output voltage of the seven-level inverter has seven voltage levels. The output current of the seven-level inverter, shown in Fig. 9(c), is sinusoidal and in phase with the utility voltage, which means that the grid-connected power conversion interface feeds a pure real power to the utility. The total harmonic distortion (THD) of the output current of the seven-level inverter is 3.6%. Fig. 10 shows the experimental results for the dc side of the seven-level inverter. Fig. 10(b) and (c) show that the voltages of capacitors C_2 and C_1 of the capacitor selection circuit have multiple relationships and are maintained at 60 and 120 V, respectively. Fig. 10(d) shows that the output voltage of the capacitor selection circuit has three voltage levels (60, 120, and 180 V). Fig. 11

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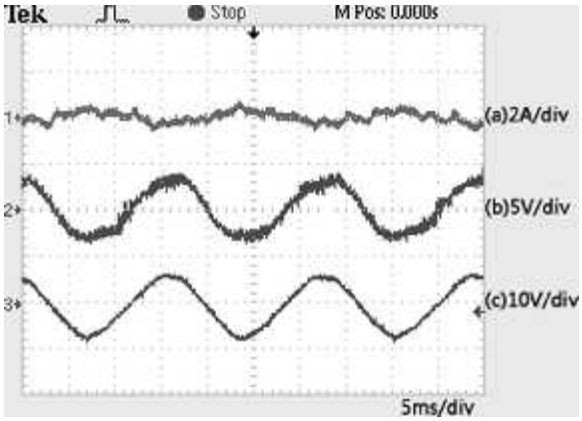

Fig. 11. Experimental results of the dc–dc power converter: (a) ripple current of inductor, (b) ripple voltage of capacitor C2, and (c) ripple voltage of capacitor C1.

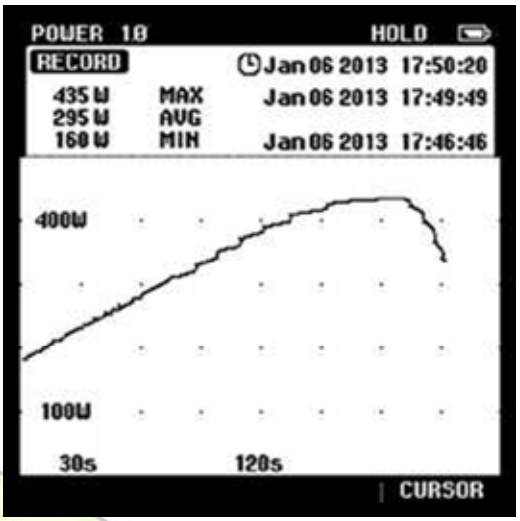

Fig. 12. Output power scan of the solar cell array.

shows the experimental results for the dc–dc power converter. Fig. 11(b) and (c) shows that the ripple voltages in capacitors C_1 and C_2 of the capacitor selection circuit are evident. However, the ripple current in the inductor of the dc–dc power converter is less than 0.5 A when the average current of inductor is 8 A, as shown in Fig. 11(a). Therefore, the ripple voltages in C_1 and C_2 are blocked by the dc–dc power converter. Fig. 12 shows the output power scan for the solar cell array when the output voltage changes from 40 to 70 V. Fig. 13 shows the experimen- tal results for the beginning of MPPT for the dc–dc converter. Fig. 13 shows that the output power of the solar cell array is almost constant when maximum power tracking is achieved and its value is very close to the maximum power shown in Fig. 12. Fig. 14 shows the experimental results for the power efficiency of the proposed solar power generation system. The solar cell array was replaced by a dc power supply to simplify the adjustment of output power in the experimental process. With higher step-up gain of the dc–dc power converter, there is lower power efficiency. Hence, the higher input voltage of solar power generation system will result in better power efficiency

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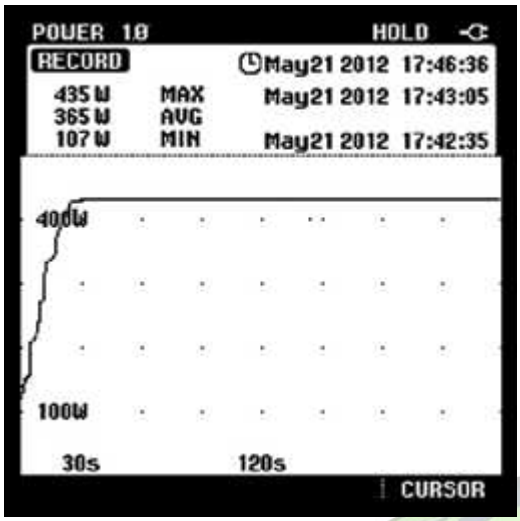

Fig. 13. Experimental results for the MPPT performance of the proposed solar power generation system.

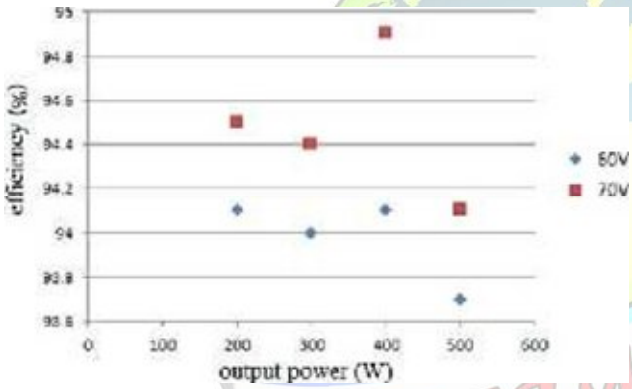

Fig. 14. Experimental results for the power efficiency of the proposed solar power generation system.

of the dc–dc power converter. Since a transformer is used in the dc–dc power converter of the proposed solar power generation system, this degrades the power efficiency of the proposed solar power generation system. However, the power transferred by the transformer is less than one third of the solar output power in the proposed dc–dc power converter, and the energy stored in the magnetizing inductance of the transformer is transferred forward to the output capacitor. Hence, the degradation of power efficiency caused by use of the transformer in the proposed solar power generation system is not serious.

VII. Conclusion

This paper proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The proposed solar power generation system is composed of a dc–dc power converter and a seven-level inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves

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the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Experimental results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor of unity. In addition, the proposed solar power generation system can effectively trace the maximum power of solar cell array.

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