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LOW POWER EXPLICIT TYPE PULSE TRIGGERED FLIPFLOP USING TSPC LATCH BASED ON SIGNAL FEEDTHROUGH SCHEME

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Abstract: In this brief, a low-power flip-flop (FF) design using an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem existing in conventional explicit type pulse-triggered FF (P- FF) designs. It helps to achieve better speed and power performance. Based on simulation results using Tanner EDA, the proposed design outperforms the conventional P-FF design explicit pulse data-close-to-output (ep-DCO) by 8.2% in data-to-Q delay. In the mean time, the performance edges on power and power- delay-product metrics are 22.7% and 29.7% respectively.

Keywords: Flip flop, Pulse triggered, True single phase clock, signal feed through

1. INTRODUCTION

Flip-flops are the basic memory elements for storing information. Hence, they are the fundamental building blocks for all sequential circuits. A single flip-flop can store only one bit of information. In digital designs nowadays often employ many FF-rich modules such as register file and shift register. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design [1], [2]. Flip- flops are used more often since they can all be synchronized to change only at the active edge of the enable signal. This enable signal for the flip-flops is usually the global controlling clock signal.

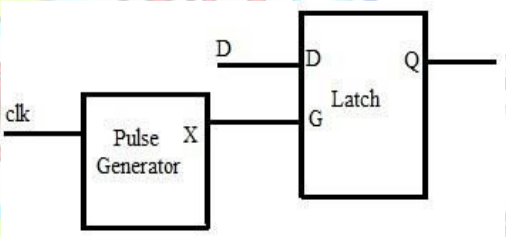

Fig (1)

In Pulse triggered flip flops, a short pulse around the rising (or falling) edge of the clock is created through a pulse generator circuit (Fig 1). This pulse acts as the clock input to a latch. Sampling of latch is done in this short window created by the pulse generator. Race conditions are thus avoided by keeping the opening time (i.e , the transparent period) of the latch very short. The combination of the glitch generation circuitry and the latch results in a positive edge-triggered register. The only type of flip flops which has time borrowing capability with negative set-up time is pulse triggered flip flops. In this brief, proposes a low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1" and "0," the design shortens the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data

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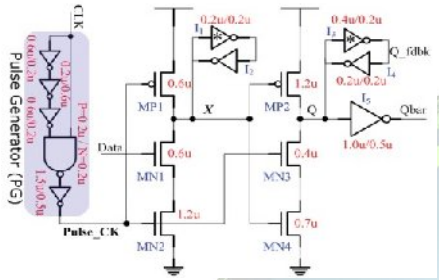
transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the explicit pulse generation circuitry, it forms a new P- FF design with enhanced speed and power-delay- product (PDP) performances.

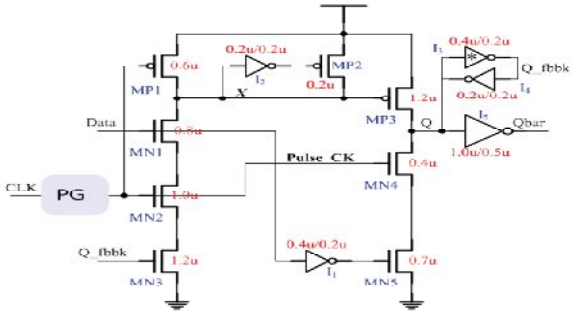
II. EXISTING METHOD

A.Conventional explicit typePFF



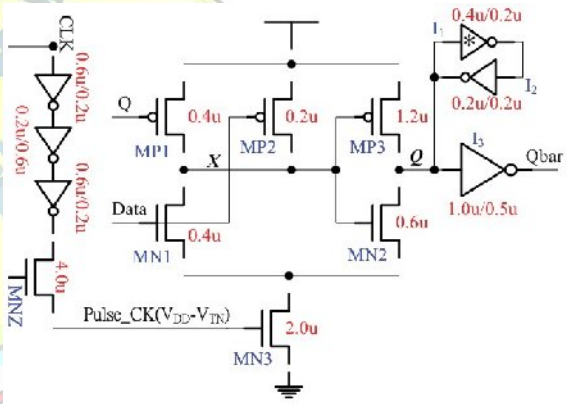
(a)

Fig (a) shows the schematic of the Explicit- Pulse Data-Close-to-Output flip-flop (ep-DCO) which is considered as one of the fastest flip-flops due to its semi-dynamic characteristics. The pulse generator of the Explicit-Pulse Data-Close-to-Output flip-flop uses the delay of three inverters to generate the pulse at the double edge of the clock. In the ep- DCO, there are two stages, the first stage is dynamic and the second stage is static. The clock pulse drives three transistors-MP1,MN2 and MN3. The input data is connected to MN1 and the circuit captures the data through MP2. When the flip-flop is transparent, the input data propagates to the output, after the transparent period, MN2 and MN3 will turn off because of the low voltage of the pulse at the same time, point X change to the high voltage because that MP1 is on at this time. So MN4 is off after the transparent period. Hence, any change at the input cannot be passed to the output. This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed [3]–[7].



(b)

Fig. (b) shows a conditional discharged (CD) technique[5]. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1". In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only. But this design face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1– MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.



(c)

Fig(c) shows the modified hybrid latch flip flop (MHLFF) [8] . It also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not pre discharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level- degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power [7].

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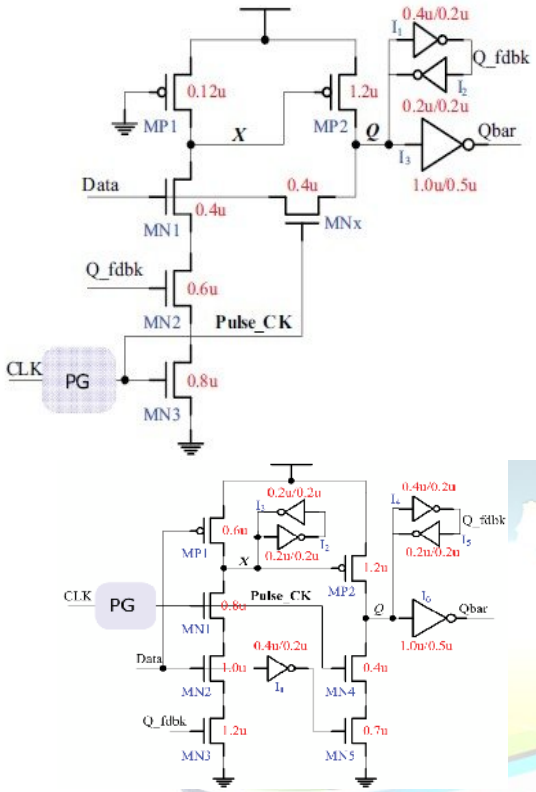

(d)

Fig: (d) Proposed P-FF design

Fig.(d) shows a similar P-FF design (SCDFF) using a static conditional discharge technique(15) . It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical pre charges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

III.PROPOSED TECHNIQUE

The proposed design introduces a signal feed-through technique to improve the delay. Mainly three major differences that lead to a unique TSPC latch structure and it makes the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [9], [10]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed- through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions.

The principles of FF operations of the proposed design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node X is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high. With the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened.

IV.PERFORMANCE ANALYSIS

The pulse width design is crucial to the correctness of data capture as well as the power consumption [11]-[14], the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width. Since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a 20-fF capacitor. An extra loading capacitance of 3 fF is also placed at the output of

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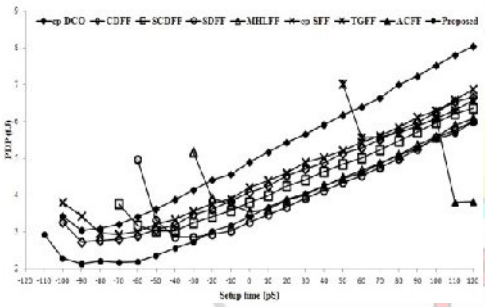
the clock buffer [7].

FF Designs	ep-DCO	CDFF	SCDFF	MHLFF	Proposed
Number of transistors	28	30	31	19	24
Layout area (μm^2)	77.86	89.70	89.16	78.94	69.13
Setup time (ps)	−83.8	−88.2	−44.8	1.5	−85.7
Hold time (ps)	110	123.5	122.6	95.7	120.1
Minimum D-to-Q delay (ps)	118.9	129.5	140.0	173.8	109.1
Average power (100% activity) μW	34.41	34.08	35.16	31.82	30.09
Average power (50% activity) μW	28.72	25.57	25.13	24.23	23.43
Average power (25% activity) μW	25.26	20.97	21.25	20.32	19.52
Average power (12.5% activity) μW	24.03	19.16	19.28	18.53	17.89
Average power (0% all-1) μW	29.70	17.08	17.25	16.75	16.06
Average power (0% all-0) μW	16.96	17.12	17.19	16.75	16.17
Optimal PDP (25% activity) pJ	3.03	2.72	2.98	3.58	2.13

Table I : Feature comparison of various FF designs



A .Power Consumption Performance of FF Designs

Table I summarizes the circuit features and the simulation results. For circuit features, although the proposed design does not use the least number of transistors, it has the smallest layout area. This is mainly attributed to the signal feed-through scheme, which largely reduces the transistor sizes on the discharging path. In terms of power behavior, the proposed design is the most efficient in five out of the six test patterns. The savings vary in different combinations of test pattern and FF design. For example, if a 25% data switching test pattern is used, the proposed design is more power-economical.

FF Designs	ep-DCO	CDFF	SCDFF	ep-SFF	TGFF	SDFF	ACFF	Proposed
(CLK, Data) = (0, 0)	51.48	53.53	58.97	48.76	40.05	39.78	58.07	52.42
(CLK, Data) = (0, 1)	57.94	51.51	52.02	54.75	51.04	45.09	58.48	52.76
(CLK, Data) = (1, 0)	59.87	59.56	65.31	61.76	63.66	46.38	84.77	59.03
(CLK, Data) = (1, 1)	66.43	67.96	74.66	71.24	74.53	53.19	85.45	70.54
Average	58.93	58.14	62.74	59.13	57.32	46.11	71.69	58.63

Table II: Leakage power comparison in standby mode

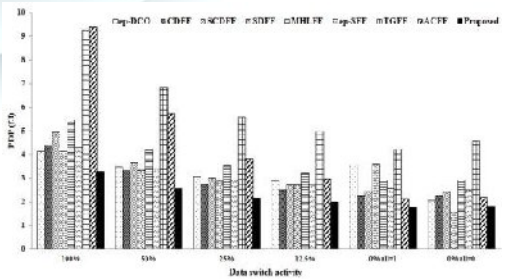
Referring to Table II, the leakage power consumption of the proposed design is very close to that of other P-FF designs. The MHLFF design is the one that suffers from a large dc power consumption because of a non full-swing internal node. Its dc (leakage) power consumption is much higher than others and is thus excluded from the comparison [7].

B. Timing Parameters of FF Designs

After the analysis of power performances, we then examine the timing parameters of these FF designs. In this brief, the set-up time is measured as the optimal timing (with respect to the clock edge) of applying input data to minimize the product of power and D-to-Q delay. In other words, its choice is based on the optimization of PDPDQ instead of the D-to-Q delay alone.

The PDP values of the proposed design are smaller than other designs in almost all setup time settings shown in Fig (d). For most P-FF designs, the minimum PDP values occur at negative setup times. This is because of the extra delay introduced by the pulse generator so that input data can be applied after the triggering edge of the clock.

(d) PDPDQ versus setup time settings



(e) C-to-Q delay versus hold time settings.

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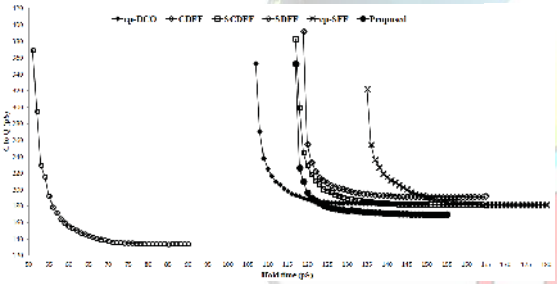
The measured setup and hold times of the proposed design are –85.7 and 120.1 ps, respectively. All but one P-FF designs under comparison exhibit similar timing parameters. The exception is the MHLFF design, which has a slightly positive setup time and a shorter hold time than its counterparts because of a simpler pulse generator. A longer hold time mainly affect the design of the driving logic. If P-FFs are adopted in the entire design, the hold time constraint can be easily satisfied because of a prolonged clock-to-Q delay property in P-FF designs. Introducing an input delay buffer is also a simple measure to alleviate the hold time requirement.

Fig (f) shows the PDP_{DQ} performance under different data switching activities. The proposed design outperforms others in all but the case of SDFF at 0% switching activity (all zero). The PDP_{DQ} values obtained under the test pattern with 25% switching activity are also listed in Table I.



(f)

V.CONCLUSION

In this brief, presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor.

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