HYBRID 1 BIT FULL ADDER DESIGN EMPLOYING C MOS LOGIC AND TRANSMISSION LOGIC GATES

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Abstract:. In this paper, a hybrid 1-bit full adder design employing both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic is reported. The design was first implemented for 1 bit and then extended for 32 bit also. The circuit was implemented using Cadence Virtuoso tools in 180- and 90-nm technology. Performance parameters such as power, delay, and layout area were compared with the existing designs such as complementary pass-transistor logic, transmission gate adder, transmission function adder, hybrid pass-logic with static CMOS output drive full adder, and so on. For 1.8-V supply at 180-nm technology, the average power consumption (4.1563 μW) was found to be extremely low with moderately low delay (224 ps) resulting from the deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates. Corresponding values of the same were 1.17664 μW and 91.3 ps at 90-nm technology operating at 1.2-V supply voltage. The design was further extended for implementing 32-bit full adder also, and was found to be working efficiently with only 5.578-ns (2.45-ns) delay and 112.79-μW (53.36-μW) power at 180-nm (90-nm) technology for 1.8-V (1.2-V) supply voltage. In comparison with the existing full adder designs, the present implementation was found to offer significant improvement in terms of power and speed.

***Keywords:* Carry propagation adder, high speed, hybrid design, low power**

I. INTRODUCTION

Increased usage of the battery-operated portable devices, like cellular phones, personal digital assistants (PDAs), and notebooks demand VLSI, and ultra large-scale integration designs with an improved power delay characteristics. Full adders, being one of the most fundamental building block of all the afore mentioned circuit applications, remain a key focus domain of the researchers over the years [1], [2]. Different logic styles ,each having its own merits and bottlenecks, was investigated to implement1-bit full adder cells [3]–[11]. The designs, reported so far, may be broadly classified into two categories: 1) static style and 2) dynamic style. Static full adders are generally more reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart [3], [4].Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS) [3], dynamic CMOS logic [4], complementary pass-transistor logic (CPL) [5], [6], and transmission gate full adder (TGA) [7], [8] are the most important logic design

styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation [9]. These designs exploit the features of different logic styles to improve the overall performance of the full adder.

The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers [3]. Another complementary type smart design is the mirror adder [4] with almost same power consumption and transistor count (as that of [3]) but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing32 transistors [5], [6]. However, CPL is not an appropriatechoice for low-power applications. Because of its high switching activity

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of intermediate nodes (increased switching power), high transistor count, static inverters, and overloading of its inputs are the bottleneck of this approach. The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only20 transistors for full adder implementation [7], [8]. However, the other drawbacks of CPL like slow-speed and high-power consumption remain an area of concern for the researchers. Later, researchers focused on the hybrid logic approach which exploited the features of different logic styles in order to improve the overall performance. Vesterbacka [10] reported a 14-transistor full adder employing more than one logic style for their implementation. Similarly, the hybrid pass-logic with static CMOS output drive full adder (HPSC) was proposed by Zhang *et al.* [11]. In such HPSC circuit, XOR, and XNOR functions were simultaneously generated by pass transistor logic module by using only six transistors, and employed in CMOS module to produce full-swing outputs of the full adder but at the cost of increased transistor count and decreased speed. Although the hybrid logic styles offers promising performance, most of these hybrid logic adders suffered from poor driving capability issue and their performance degrades drastically in the cascaded mode of operation if the suitably designed buffers are not included. and the delay of the circuit (224 ps), in 180-nm technology, were comparable with the other hybridized implementations and better with respect to other full CMOS implementation, respectively. For 90-nm technology operated at 1.2-V power supply, the corresponding values are 1.17664 μW (average power consumption), 91.3 ps (delay), and 25.84 μm^2 (layout area excluding buffer). The design was verified and proved to be also promising for 32-bit carry propagation adder.

DESIGN APPROACH OF THE PROPOSED FULL ADDER

The proposed full adder circuit is represented by three blocks as shown in Fig. 1(a). Module 1 and module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the output carry signal (C_{out}). Each

mod- ule is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail.
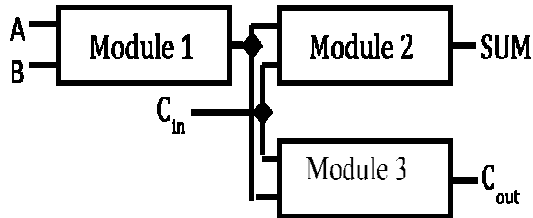
A. Modified XNOR*Module*

In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. Fig. 1(b) shows the modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors Mp1and Mn1 [Fig. 1(b)]. Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3 [Fig. 1(b)]. Various XOR/XNOR topologies have already been reported in [7]. The XOR/XNOR uses four transistors but at the cost of low logic swing. To the contrary, the XOR/XNOR reported in [7] uses six transistors to get better logic swing compared with that of 4 T XOR/XNOR . In this paper also, the XNOR module employed 6 T, but having different transistor arrangement than that of 6 T XOR/XNOR [7]. The modified XNOR presented in this paper offers low-power and high-speed (with acceptable logic swing) compared with 6T XOR/XNOR [7].

B.CarryGeneration Module

In the proposed circuit, the output carry signal is imple- mented by the transistors Mp7, Mp8, Mn7, and Mn8 as shown in Fig. 1(c). The input carry signal (C_{in}) propagates only through a single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8, and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal.

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(a)Schematic structure of proposed full adder.
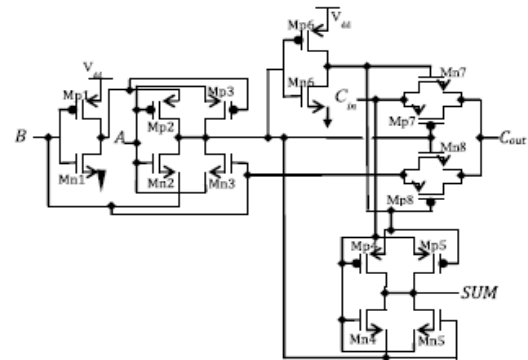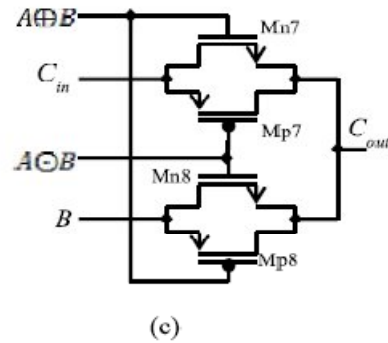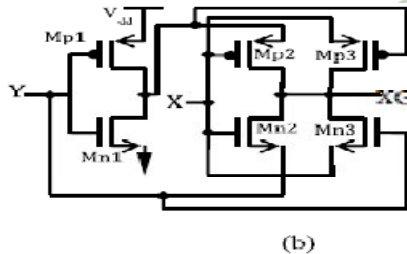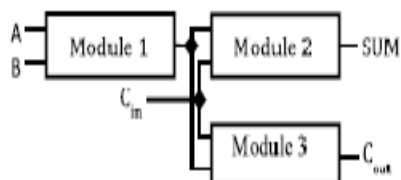

(b)XNOR module

Fig2.Detail circit daigram of proposed full adder

OPERATION OF THE PROPOSED FULL ADDER WITHSIMULATION TEST BENCH SETUP

Fig. 2 shows the detail diagram of the proposed full adder. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem, which has been removed using two pass transistors Mp3 and Mn3. pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6) realize the second stage XNOR module to implement the complete SUM function. Analyzing the truth table of a full adder, the condition for C_{out} generation has been deducted as follows:If, $A = B$, then $C_{out} = B$; else, $C_{out} = C_{in}$

The parity between inputs A and B is checked by $A \quad B$ function. If they are same, then C_{out} is same as B, which is implemented using the transmission gate realized by transistors Mp8 and Mn8. Otherwise, the input carry signal (C_{in}) is reflected as C_{out} which is implemented by another transmission gate consisting of transistors Mp7 and Mn7 It is likely that a single bit adder cell designed for optimum performance may not perform well under deployment to real-time conditions. This is because when connected in cascaded form, the driver adder cells may not provide proper input signal level to the driven cells. The cumulative degradation in signal level may lead to faulty output and the circuit may malfunction under low supply voltages. To analyze the success of the proposed full adder during its actual use in VLSI applications, a practical simulation environment is setup as shown in Fig. 3. To provide a realistic environment, buffers are added at the input and the output of the test bench]. The inputs to the adder cell, are fed through the buffers to incorporate the effect of input capacitance and the outputs are also loaded with buffers to ensure proper loading condition. The proposed full adder is simulated using several test bench setups. These test benches are having the common prototype of three buffers at the input and two buffers at the output (Fig. 3). They only differed in the number of stages of adder cells used in between the input and output of the simulation setup. The number of stages varied starting from two and increased gradually. It was observed that the carry propagation delay from the input to the output started rising significantly in the order of two after the third stage (explained in detail in Section IV-B). Therefore, the three-stage simulation test bench is selected for simulation purpose. Further, the behavior of performance parameters (power and delay) could be measured from the second adder cell by using this test bench. This offered the tested adder cell to have the output and input capacitances of adjacent adder cells as its input and output capacitance; allowing a real time simulation environment for cascaded approach. Numerous random signal patterns were applied at the inputs and the worst case simulation results of the second full adder cell was accounted for analysis and comparison. The performance analysis of the proposed full adder was performed with variation in supply voltage both for 180- and 90-nm technology.

The simulation of the proposed full was carried out using both 90- and 180-nm technology and compared with the other potential adder designs reported in [1] with special emphasis on the hybrid design approach [1], [2].

TABLE I

TRANSISTOR SIZES OF PROPOSED FULL ADDER

Transistor Name	180nm technology		90nm technology	
	Width (W) (nm)	Length (L) (nm)	Width (W) (nm)	Length (L) (nm)
Mn1, Mn6	400	180	120	90
Mp1, Mp6	800	180	240	90
Mn2, Mn3	400	180	120	90
Mp2, Mp3	800	180	360	90
Mn4, Mn5	400	180	120	90
Mp4, Mp5	400	180	120	90
Mn7, Mn8	400	180	360	90
Mp7, Mp8	400	180	600	90

PERFORMANCE ANALYSIS OF THEPROPOSED FULL ADDER

TABLE II
SIMULATION RESULTS FOR FULL ADDERS IN 180 nm
TECHNOLOGY WITH 1.8 V SUPPLY

Design	Average Power (µw)	Delay (ps)	PDP (fJ)	Transistor Count	Reference
C-CMOS	6.2199	292.1	1.816832	28	[4,18]
Mirror	6.0797	281.61	1.712104	28	[18]
CPL	7.71985	183.97	1.42022	32	[5, 6]
TFA	8.2491	287.1	2.368316	16	[21]
TGA	8.4719	293.9	2.8989	20	[7, 8]
14 T	12.7217	381.7	4.85587	14	[10]
10 T	14.3449	132.595	1.902062	10	[24]
HPSC	6.3798	273.7	1.74615	22	[11]
Majority Based	6.3227	185.4	1.17222	--	[23]
24T	15.91	314.2	4.998	24	[1]
FA_Hybrid	5.978	252.3	1.508	24	[2]
FA_DPL	19.56	226.6	4.432	22	[19]
FA_SR-CPL	20.78	220.65	4.585	20	[19]
Proposed	4.1563	224	0.931	16	[Present]

TABLE III
SIMULATION RESULTS FOR FULL ADDERS IN 90 nm
TECHNOLOGY WITH 1.2 V SUPPLY

Designs	Average Power(µW)	Delay (ns)	PDP(fJ)	Transistor Count	Reference
C-CMOS	1.5799	0.1269	0.200489	28	[4,18]
Mirror	1.5701	0.1226	0.19249	28	[18]
CPL	1.7598	0.0791	0.1392	32	[5,6]
TFA	1.7363	0.3198	0.55526	16	[21]
TGA	1.7619	0.2317	0.40823	20	[7,8]
14T	3.3297	0.3389	1.12843	14	[10]
10T	---	---	---	10	[24]
HPSC	1.56	0.2207	0.34429	22	[11]
Majority Based	1.5751	0.0939	0.1479	--	[23]
24T	7.707	0.1406	1.0836	24	[1]
FA_Hybrid	6.21	0.143	0.888	24	[2]
FA_DPL	7.34	0.254	1.864	22	[19]
FA_SR-CPL	7.4	0.167	1.235	20	[19]
Proposed	1.17664	0.0913	0.107427	16	[Present]

of existing full adders (from literature) are given in Tables II and III for 180-nm and 90-nm technology, respectively.For comparison in a common environment, the proposed fulladderas well as the other reported ones, as cited in Tables I–III, were simulated using the common test bench. The simulation was performed for varying supply voltage ranging from 0.8 to 2.5 V (0.6–1.5 V) in 180-nm (90-nm) technology. The performance result of 10 T full adder is unavailable in Table III, because it is nonoperable with1.2 V at 90-nm technology . The majority-based adder, reported by Navi et al. [23], included capacitors in their design, hence avoided to maintain the uniformity of the comparison. The proposed hybrid full adder has also been compared with other hybrid full adders reported in [1], [2], and [19]. The circuit of the hybrid full adder reported in [1], [2], and [19] were resimulated in cadence virtuoso tools in 180- and 90-nm technology, so this paper can be authentically compared. The proposed hybrid adder requires only 16 transistors whereas the other hybrid adders [1], [2], require more than 20 transistors. The average power consumed by the proposed full adder is significantly lower than that of other hybrid full adders. The use of less number of transistors in this paper also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid full adder is significantly improved in comparison with the earlier hybrid adders. The detailed comparison of the proposed full adder with other hybrid full adders [1], [2], in 180- and 90-nm technology isrepresented in Tables II and III, respectively.The performance of the proposed full adder in terms of power consumption and propagation delay with variation in supplied voltage was carried out (not shown here) and the corresponding comparison of the PDP (with the other existing designs) is shown in Fig. 4. The optimization of power consumption and propagation delay of the proposed full adder is explained in detail with necessary mathematical calculations in Sections IV-A and IV-B.A. Calculation of Power ConsumptionPower consumption of the hybrid full adder can be broadly classified into two categories: 1) static power and 2) dynamic and short-circuit power .

With an aim to optimize both power and delay of the circuit, the power-delay product (PDP), that is, the energy consump- tion has been minimized in the proposed case. It was observed that in the present design, the power consumption could be minimized by mainly sizing the transistors in inverter circuits; while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from Cin to Cout . The transistor sizes of the proposed full adder circuit are given in Table I for both the technologies (90 and 180 nm). Power consumption, propaga- tion delay, and PDP of the proposed full adder along with that
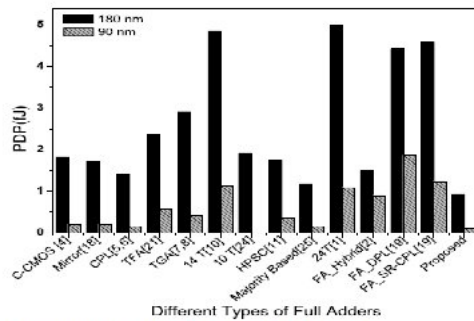
Fig. 4. Comparison of PDP of various full adder designs.

Static power, originated from biasing and leakage currents, in most of the CMOS-based implementations is fairly low when compared with its dynamic counterpart [3]. In this paper,with an aim to minimize the static power further, the weak inverters having large channel width of 800/240 nm (in 180/90-nm technology) for Mp1 and Mp6, respectively, and 400/120 nm (180/90-nm technology) for Mn1 and Mn6, respectively (Fig. 2), was incorporated deliberately. The over-all static power in 180-nm technology was found to be2.139 nW for 1.8-V supply which is very low when comparedwith the overall dynamic power (4.1563 μW). To the contrary, the static power in 90-nm technology at 1.2-V supply was found to be 0.936 nW which is also lower than the corre-sponding dynamic power (1.17664 μW) but the ratio (of static power:dynamic power) increased. This increase in static power is possibly due to the increase in the subthreshold conduction current and gate leakage [3].The dominant component of the power consumption, thedynamic power, arises because of charging and discharging of the load capacitances. The load capacitance, Cload, can be expressed as a combination of a fixed capacitance, Cfix, and a variable capacitance, Cvar, as follows:Cload = Cfix + Cvar . (1) In this expression, Cfix is the technology-dependent(principally originated from diffusion capacitance) andinterconnect dependent capacitances. The interconnect dependent capacitance is minimized by efficient layout design in this case. On the other hand, Cvar is composed of the input capacitances of subsequent stages and a part of the diffusion capacitance at the gate output and can therefore be taken care of by proper sizing of the transistors.For every low-to-high logic transition in an adder, Cloadincurs a voltage change V , drawing energy (Cload ∗ V ∗VDD) from the supply voltage VDD. For each node j belongsto N , these transitions occur at a fraction α j of the clock frequency fc . So the total dynamic switching power can be calculated by summing over all N nodes in the circuitIt is clear from (2) that the transistor size could be an effective parameter for reducing dynamic power consumption. Also, the inverters have to be weak and the transmission gates have to be

strong. Initially, the transistor sizes were chosen on the theoretical background of the design. Subsequently, they were varied (through simulations) in the vicinity of the previously set values to obtain the best performance in terms of power and delay. The optimized transistor sizes of the proposed full adder are already summarized in Table I.It was observed that the static power of the developed circuit varied from 56.38 to 392.4 pW for variation in supply voltage from 0.8 to 2.5 V in 180-nm technology. In contrast, the dynamic power varied from 114.08 nW to 6.125 μW for the same voltage variation. Considering the similar kind of implementation using 90-nm technology with a voltage range of 0.6–1.5 V, the dynamic power consumption was found to be reduced dramatically while the static powerconsumptionHence, such cascaded full adders (proposed design) oper- ating in carry propagation mode (carry propagation adder) loaded with capacitance C L can be represented by its equiva- lent R–C circuit as shown in Fig. 5(b).Assuming the voltage source, Vin , to be a step waveform (for simplicity), the delay τpd (m) of the cascaded proposed full adders, can be evaluated by simplifying it into a first- order circuit having a time constant, τ , and applying the Elmore delay approximation [3] as follows: increased in comparison with the 180-nm case [Fig. 4(b)].It is worth mentioning here that at 180-nm technology, thetakes place after 2.5 V. So voltage was varied from 0.8 to 2.5 V in 180-nm node. On the other hand, at 90-nm technology, the threshold voltage is 0.6 V and the MOSFET break down occurs at 1.5 V. So, the voltage was varied from 0.6 to 1.5 V in the 90-nm case.B. Calculation of Propagation DelayBecause adder is the fundamental computational unit in most of the systems, its delay predominantly governs the overall speed performance of the entire system. Also, the speed of response of an adder is mainly dependent on the propagation delay of the carry signal which is usually minimized by reducing path length of the carry signal. In the present design, the carry signal is generated by controlled transmission of the input carry signal and either of the input signals A or B(when A = B). As the carry signal propagates only throughthe single transmission gate, the carry propagation path isminimized leading to a substantial reduction in propagation delay. The delay incurred in the propagation is further reducedIt is seen from (3) that the propagation delay of the proposed adder increases rapidly with the increase in the length of the adder chain (increases as the square of m). The simulation results incorporating the gradual increase in the number of stages of full adders also validated this second order rise in delay with increase in the number of stages [Fig. 6(a)]. The simulation results [given in Fig. 6(a)] were measured for no load capacitance (180-nm technology) and the worst case carry propagation delay is represented here. Incorporation of

the load capacitance increased the delay but the nature of the graph remained the same. To minimize the overall delay, the buffers were included at appropriate stages of full adder chain. For efficient incorporation of buffers at appropriate stages, analytical evaluation was performed by extracting capacitance and resistance values from the postlayout simulation results.adder, operating in the carry propagation mode, the speed per- formance of the adder deteriorates with increase in the number of adder stages. Similar observations were also reported in case of other transmission gate-based approaches.

C. Calculation of Area of 1-bit Adder

. The layout area (excluding buffer) in the present design is higher (6.55%) than that of TFA which is also comprised 16 transistors [21]. When compared with the best design in terms of area (10 T)
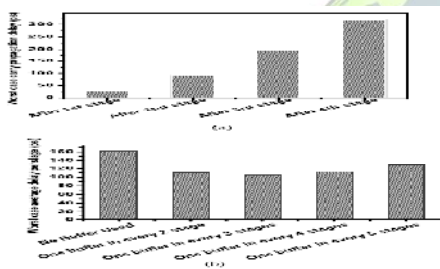

Fig. 6. (a) Total carry propagation delay for different stages (without load capacitance). (b) Variation of average delay with introduction of buffers at different stages.
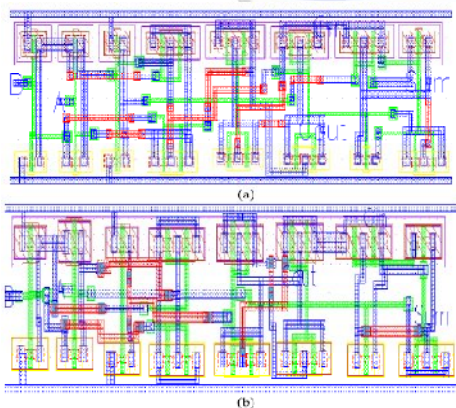

Fig. 7. (a) Layout of the 1-bit full adder in 180-nm technology. (b) Layout of the 1-bit full adder in 90-nm technology.

V. PE RFORMANCE OF 32-bit FUL L ADDE R

A 32-bit carry propagation adder [Fig. 8(a)] is implemented as an extension of the proposed 1-bit full adder. It is a noncarry
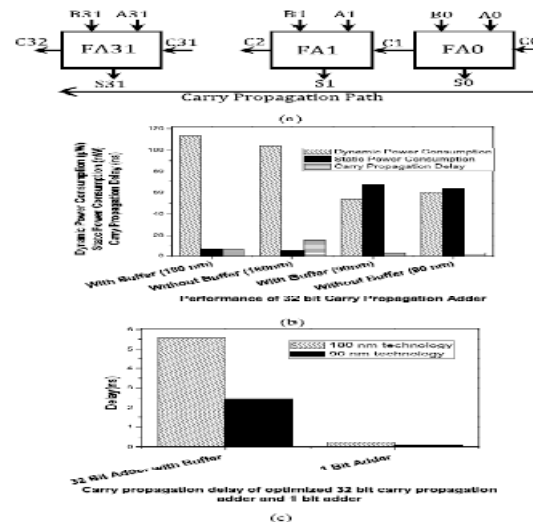

Fig. 8. (a) 32-bit full adder using 1-bit full adder. (b) Performance (power and delay) of 32-bit carry propagation adder with and without buffer with supply voltage of 1.8 V/1.2 V for 180 nm/90 nm. (c) Behavior of carry propagation delay when extended from proposed 1-bit full adder to 32-bit carry propagation adder.

CONCLUSION

In this paper, a low-power hybrid 1-bit full adder has been proposed the design has been extended for 32-bit casealso.The simulation was carried out using standard Cadence Virtuoso tools with 180/90-nm technology and compared with other standard design approaches like CMOS, CPL, TFA, TGA, and other hybrid designs.The simulation results established that the proposed adder offered improved PDP compared with the earlier reports. The efficient coupling of strong transmission gates driven by weak CMOS inverters lead to fast switching speeds (224 ps at 1.8-V supply), for a layout area of 102.94 μm2 (in 180-nm technology) excluding buffer. The proposed full adder offered 20.56% improvement with respect to the best reported design in terms of PDP (180-nm technology at 1.8 V). Corresponding PDP improve- ment was 27.36% when the same design was implemented in90-nm technology at 1.2-V power supply. The proposed full adder was further used to implement a 32-bit carry propagation adder having buffers at appropriate adde rstages (after three stages).

ACKNOWLEDGEMENT

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