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SRAM Performance Enhancement Using Sense Amplifier Based Design Technique

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Abstract: SRAM cells are known to be highly sensitive to process variations due to the extremely small device sizes. Local random variations in device characteristics can easily lead to Read disturb, Write failure, or Read access failure in SRAM cell. Transient negative bit-line voltage technique is presented to improve write-ability of SRAM cell. Capacitive coupling is used to generate a transient negative voltage at the low-going bit-line during Write operation without any on-chip or off-chip negative voltage source. In this work Read assist sense amplifier based design technique is presented to reduce read failure of SRAM cell. Furthermore, "false read" before write operation, common to conventional 6T designs due to bit-select and word line timing mismatch, is eliminated using the Read assist sense amplifier based design technique. Tran-NBL able to achieve higher reduction in write failure compared to lower cell supply voltage while preserving the benefits of bit-line based control and eliminating the need for additional voltages. The design of Transient Negative Bit Line Voltage Scheme and sense amplifier based design technique for 6T SRAM has been implemented and corresponding result was obtained using DSCH tool. Simulation analysis of the proposed SRAM design with state-of-art designs demonstrates show better performance in terms of area power and delay.

Keywords: Column-decoupled, differential/domino read,half-select, low power 8T, SRAM, stability

I. INTRODUCTION

SRAM cells are known to be highly sensitive to process variations due to the extremely small device sizes. Local random variations in device characteristics can easily lead to Read disturb (cell flipping during Read), Write failure, or Read access failure (increase in Read delay resulting in incorrect sensing) in SRAM cells as in Figure 1. Conflicting requirements imposed by Read/Write operations and cell disturbs make it difficult to simultaneously mitigate the various failure, a conventional 6 T SRAM cell with the node L storing '1'. In order to write '0' to the node , the voltage at that node needs to be pulled down to the trip-point of inverter associated with the node R (i.e., PR–NR) while the word-line (WL) is still enabled. If PL becomes stronger and/or SL becomes weaker, due to process variations, the discharge of the node L gets more difficult. Further, if PR and SR become weaker and NR becomes stronger, the trip-point of the PR–NR reduces. Hence, node may not drop below the trip-point of PR –NR , resulting in a Write failure. In general, stronger access devices(SR/SL) and/or weaker pull-up devices (PR/PL) improve the write-ability of the cell.

II. PREVIOUS WORK

A. SRAM Write And Read Capability At Low Voltage

The write capability is enhanced by negative write biasing without any reduction in the cell current for the other port. The result shows 12% better improvement with just 1.9% area overhead .This technique has been verified successfully on 65nm and 45nm SRAM chip and improved 120mV lower at 95% yield of minimum operation voltage than a conventional one. The read capability is enhanced by cell current boosting and word line voltage lowering schemes.

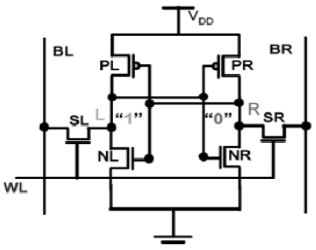

Figure 1. Circuit diagram for 6T SRAM

In a static random-access memory (SRAM) cell, a mismatch in the strength between the neighboring transistors, caused by intra-die variations, can result in the failure of the cell. For example, a cell failure can occur due

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to an increase in the cell access time (access time failure), unstable read (flipping of the cell data while reading) and/or write (inability to successfully write to a cell) operations (read/write failure) or failure in the data holding capability of the cell (flipping of the cell data with the application of a supply voltage lower than the nominal one) at the standby mode (hold failure in the standby mode). There can also be hard failures (caused by open or short) or soft failures due to soft error. A failure in any of the cells in a column of the memory will make that column faulty. In a memory, the redundant columns are used to improve the fault tolerance of the memory and when a column is detected as a faulty one, it gets replaced by an available redundant column. Thus if the number of faulty columns in a memory chip is larger than the number of available redundant columns, then the chip is considered to be faulty (a similar argument holds for the memory designed with the row redundancy).

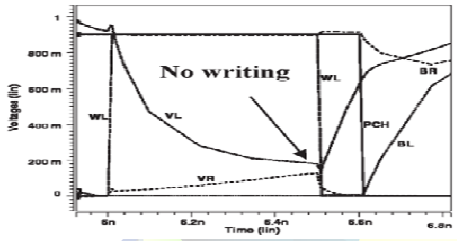

Figure 2 Write failure

In figure 2 while writing a "0" to a cell storing "1," the node VL gets discharged through BL to a low value (VWR) determined by the voltage division between the PMOS PL and the access transistor AXL. If VL cannot be reduced below the trip point of the inverter PR - NR (VTRIPWR) within the time when word-line is high (TWL), then a write failure occurs. The discharging current (IL) at node L is the difference in the ON currents of the access transistor AXL (IAXL) and the PMOS PL (IPL). Hence, a strong PMOS and a weaker access transistor can significantly slow down the discharging process, thereby causing a write failure. Thus while designing the cell, the beta ratio between the access transistor and the PMOS needs to be designed (by upsizing the access and downsizing the pull up transistors) in such a way (BR_{nax}-pup > 1) that under nominal conditions, the write time is less than the word-line turn-on time. However, the variation in the device strengths due to random variations in process parameters can increase the write time.

III. Proposed Work

A. *Transient Negative Bit-Line Voltage Technique*

The proposed Tran-NBL, shown in Figure 4 includes two boosting capacitors connected to bit-lines. The other end of the capacitors, which can be implemented using MOSFET gate capacitances, is connected to the BIT_EN signal. The signal NSEL is used for column selection. BIT_EN and NSEL are generated based on pre-charge signal (synchronized with word-line signal), Read/Write (WR) signal, and column select (CS) signals

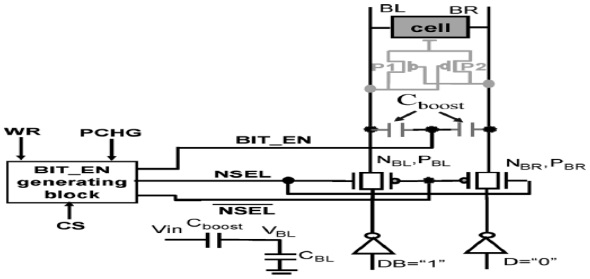

Figure 3 Proposed transient negative bit-line scheme

In the proposed scheme, the latching action of the cross-coupled inverter pairs starts as soon as V_L falls below the trip-point of PR–NR. Even when the voltage of the BL returns to '0' after the latching action is kicked off, the Write operation gets completed correctly. The NSEL and BIT_EN signals are asserted along with the pulse, and de-asserted midway through the pulse. This turns OFF the pass transistors, N_{BL}/P_{BL} and N_{BR}/P_{BR} , leaving bit-lines BL and BR floating at 0 and 1, respectively. Next, the high-to-low transition of BIT_EN causes an under-shoot at the bit-lines BL and BR due to capacitive coupling through the boosting capacitors. As the bit-line BL is floating at 0, this causes a temporary negative voltage at bit-line BL. The transient negative voltage at BL results in a transient increase in the discharging current of the access transistor SL, thus facilitating the pull-down of the node L voltage.

In the proposed scheme the delay difference between the low-to-high transition at WL and high-to-low transition at BIT_EN signal is designed to be 50% of word-line pulse width. The proposed scheme remains effective across a large range of variation of this delay. However, if the high-to-low transition of the BIT_EN signal arrives too early, the proposed scheme can result in a higher Write failure. If BIT_EN arrives too late, the proposed scheme approaches the conventional scheme.

The generations of the BIT ENABLE and NSEL signals as shown in Figure 5 are the key control logic in the

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proposed scheme. Key control logic means the signal control the specific operation of the circuit. In this proposed scheme BIT ENABLE signal control the write operation. It means when BIT ENABLE signal is enable, write operation is performed. NSEL signal control the read operation.

B. Sense Amp Based Design

The 8T-CDC cell together with read-assist sense amp designs can mitigate the read disturb problem both for selected and half-selected designs.

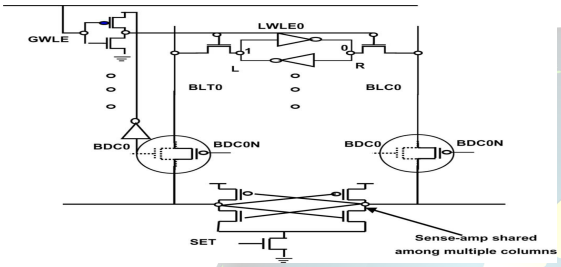

Figure 4 Gated 8T-CDC cell design combined with read-assist sense Amplifier

Hence the sense amplifier "sees" the full BL capacitance during a read operation; it discharges the capacitance to GND, and the cell data is "written back". This helps minimize the amount of read disturb charge induced onto the cell from the bit lines. It can be readily seen from the waveforms in Fig. 8 that discharging the BL capacitance completely to GND during a read operation has the effect of reducing the V_{NOISE} curve dramatically. In fact a typical sense-amplifier scenario for a weak cell flipping during read disturb under the impact of process variation, the storage nodes of the cell flip due to noise injected from the bit lines (L in dashes and R in dots).

C. 8t Column Decoupled Cell

A 8T-CDC SRAM cell (inside dashed rectangle) with a gated word line which enables the decoupling of the column/half-select condition hence eliminating half select stability fails. A localized gated inverter consisting of two additional transistors, T1 and T2, effectively perform a logical "AND" operation between the column select signal (BDT0) and the decoded row, or global word line, GWLE. The output of the inverter is the local word line signal (LWLE0). The local word line is ON only when both the column and row are selected (i.e., for fully selected cells only); hence, as illustrated in the waveforms of Fig. 8, LWLE0 of the selected columned turns ON while LWLE1 of the half-selected column remains low.

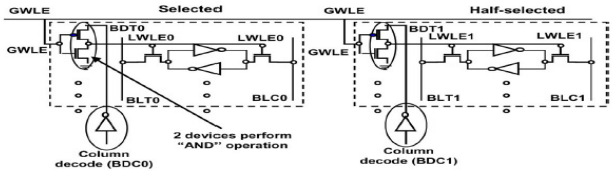

Figure 5 Column-select decoupled 8T-CDC cell

This ensures that the local word line for only the selected cells is activated, thereby effectively protecting the half-selected SRAM cells from the read disturb scenario that exists in 6T cell due to word line sharing. Alternatively, it is possible to swap the input and supply pairs of the gated inverter; however this comes at the cost of extra delay stage and power. The advantages of the 8T-CDC cell are as follows: 1) conforming with traditional 6T requirements in terms of (a) allowing the designer to integrate it in a column select fashion and (b) offering/maintaining SER protection while 2) maximizing array efficiency, 3) eliminating the read disturb to the unselected cells, and 4) reducing power with simplification in peripheral logic.

IV. Simulation Results

The analysis of the work is carried out in the DSCH tool. The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. Designers can create logic circuits for interfacing with these controllers and verify software programs using DSCH.

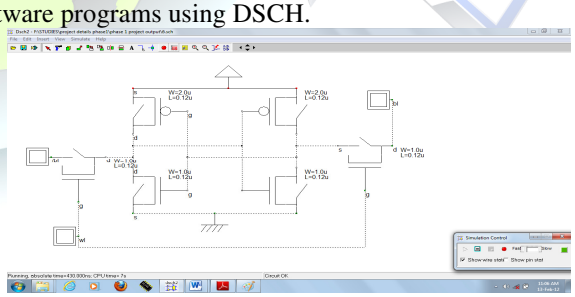

Figure 6 Schematic diagram of 6T SRAM cell design

The two control logic signals Bit ENABLE and N select signal are used to perform the write and read operation. In the Transient Negative Bit Line Voltage Scheme, control logic signals is used to control the write and read operation as in figure 6.

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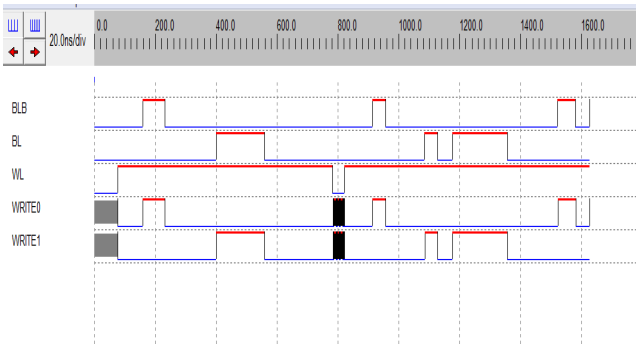

Figure 7 6T SRAM simulated output

Bit Enable and N select signals are generated based on pre charge (PCHG) signal, Read/Write (WR) signal and column select (CS) signal. When pre charge and column select signals are enabled, select signal is generated.

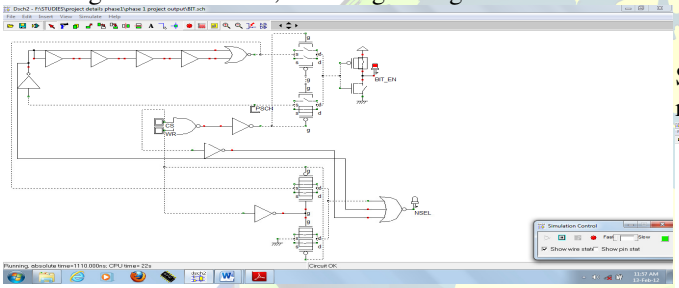

Figure 8 Transient Negative Bit Line Voltage Scheme

Capacitive coupling is used to generate a transient negative voltage at the low-going bit-line during Write operation. In the Transient Negative Bit Line Voltage Scheme, a control logic signal is used to control the write and read operation.

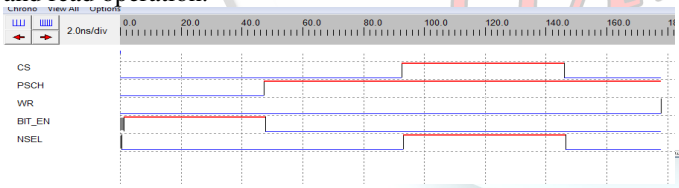

Figure 9 Generation of control logic signal

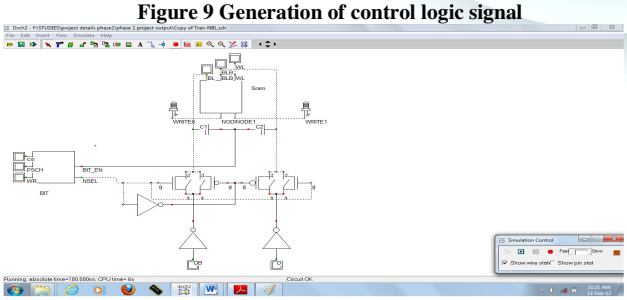

Figure 10 6T SRAM Design using Transient Negative Bit Line voltage scheme

A transient negative bit-line voltage technique is presented to avoid write-failure of SRAM cell. Capacitive coupling is used to generate a transient negative voltage at the low-going bit-line during Write operation. The transient negative pulse enhanced the access device strength to assist the Write operation. This design scheme also provided marginal improvement in Read access and Read disturb failures. The transient negative pulse enhanced the access device strength and assisted the Write operation.

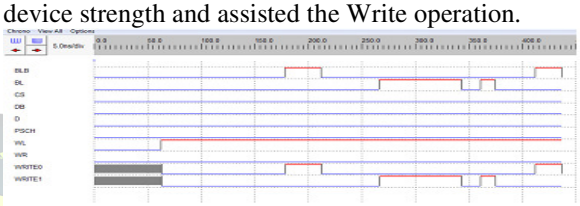

Figure 11 Simulated output for 6T SRAM Design using Transient Negative Bit Line voltage scheme

The design of Transient Negative Bit Line Voltage Scheme for 6T SRAM was implemented and corresponding result was obtained using DSCH..

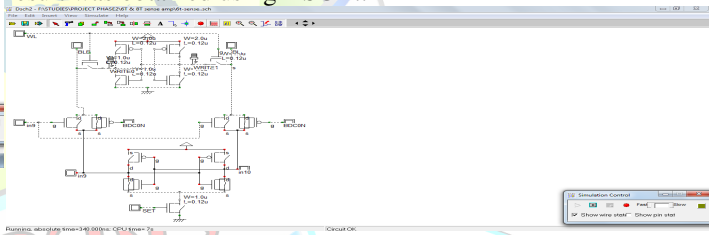

Figure 12 Schematic diagram of 6T SRAM cell design with sense amplifier based approach

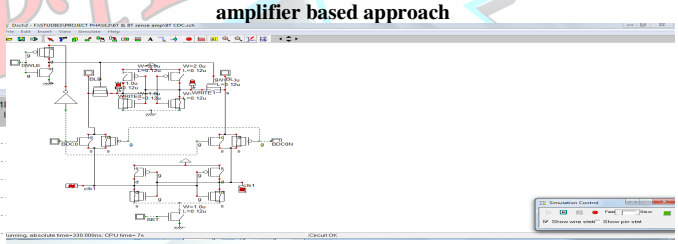

Figure 13 Schematic diagram of 6T SRAM cell design with 8T column decoupled cell based approach

The evaluation of 6T SRAM cell design is made with two techniques. One is with Sense amplifier approach and another is with CDC.

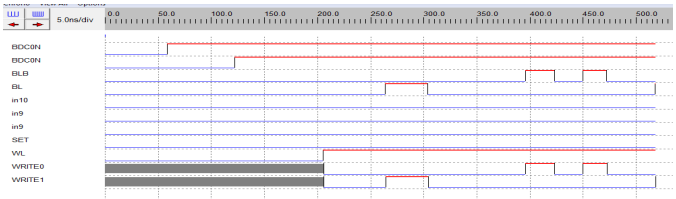

Figure 14 Simulated output for 6T SRAM with sense amplifier and 8T column decoupled cell based approaches

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TABLE 1 Performance analysis of SRAM design with various approaches

S.NO	PARAMETERS	POWER(mW)	AREA(nm)
1	SRAM design at low voltage	1.194	51.6
2	SRAM design with Transient Negative Bit line voltage	0.849	41.4
3	SRAM design with sense amplifier approach	0.798	36.8
4	SRAM design with column decoupled cell approach	0.681	32.4

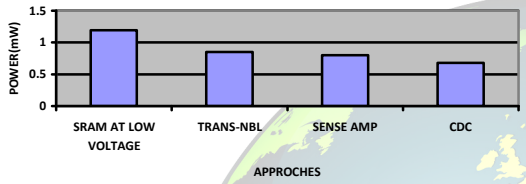

Figure 15 Power comparison

The figure 15 shows that significant power reduction that can be achieved when using 6T SRAM design with various approaches.

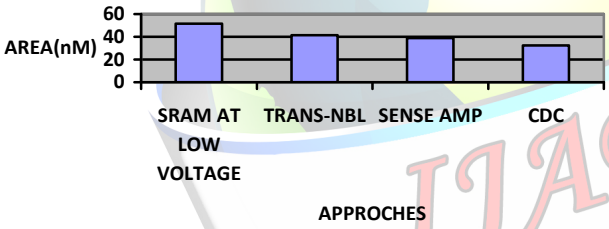

Figure 16 Area comparison

The figure 16 shows that significant area reduction that can be achieved when using 6T SRAM design with various approaches.

V. CONCLUSION

The design of sense amplifier based design technique for 6T SRAM and 8T column decoupled cell has been implemented and corresponding result was obtained using DSCH. Simulation analysis of the proposed SRAM design with state-of-art designs demonstrates show better performance in terms of area and power. The half-select free design enables enhanced voltage scaling capabilities, and 30%–40% power reduction in comparison to standard 6T techniques. This study involved a 90-nm read assist-based sense Amp design and a 65-nmdomino read-based design with dynamic supply capabilities. The design scheme also provided marginal improvement in Read access and Read disturb failures.

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