FPGA Implementation of Successive Cancellation Polar Decoder Architecture

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Abstract: Nowadays polar codes are becoming one of the most favourable capacity achieving Error Correction Codes (ECC) for their simple low encoding and decoding complexity, have received much attention in recent years; they probably achieve the theoretical capacity of discrete memoryless channels using the low complexity successive cancellation (SC) decoding algorithm. However, among the very few prior successive cancellation polar decoder designs, the required long code length makes the decoding latency high. As a new polar decoder, referred to as 2b-SC-Precomputation decoder, reduce the latency from (2n-1) to ((3n/4)-1) without performance loss. Furthermore, in our method, the decoding latency decreases rapidly with increasing throughput. Significant latency and throughput reductions are shown by simulation results and also report synthesis results for ASIC.

Keywords: Error Correction Codes (ECC), Successive Cancellation (SC), polar decoder, precomputation.

I. INTRODUCTION

Polar codes, as the first provable capacity-achieving codes over binary-input discrete memoryless channel (B-DMC) [1], have received significant attention among various forward error correction (FEC) codes. Due to their explicit structure and low-complexity encoding/decoding scheme, polar codes have emerged as one of the most important codes in coding theory. To date, many efforts have addressed several theoretical aspects of polar codes [2]–[9]. However, with the exception of [10]–[14], [19], not many publications have considered the VLSI design of polar decoders. In [10], an FPGA implementation of polar decoder based on the Belief-propagation (BP) algorithm was reported. Although BP decoder has particular advantages in parallel design, due to the requirement of large number of processing elements (PEs), the BP decoder is not attractive for practical applications. In [11], [12], [19], successive cancellation (SC) polar decoders were presented. These low-complexity architectures are suitable for area-stringent applications; however, due to the inherent serial nature of the SC algorithm, these SC decoders fall short due to long latency and low throughput. In [13], [14], a pre-computation scheme was applied to the SC algorithm, which succeeded in reducing the overall latency from (2n-2) to (n-1). However, considering the penalty of increased hardware, the SC-Precomputation decoder does not show significant improvement with respect to hardware efficiency.
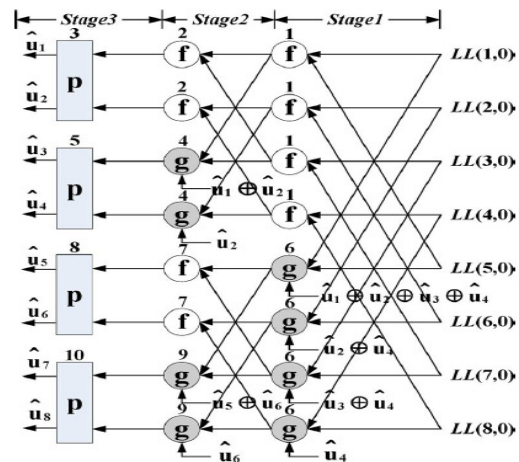
II. PROPOSED SYSTEM

Fig 1: Polar Decoder Architecture

The F node and g node are used to calculate the propagated LLR values. Here S2C is the block that performs the conversion from sign-magnitude form to 2's complement form, while C2S unit carries out the inverse conversion. Additionally, adder and subtractor are employed to carry out addition and subtraction between the two inputs. Finally, at the output end of the PE, *control* signal is used to determine the output as LLR (a) or LLR(b) ,which is propagated to the next stage.
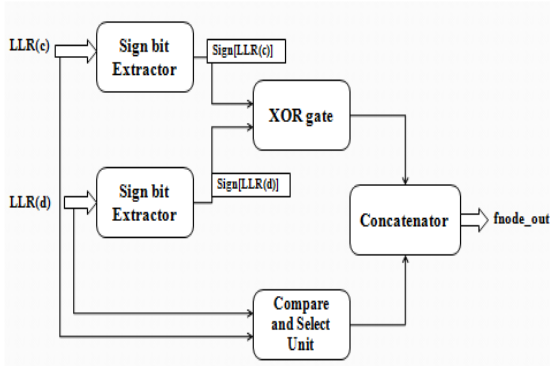
Fig 2: f-node architecture

$$\hat{u}_{2i-1} = \overline{frozen1}(sign(LLR(\hat{c})) \oplus sign(LLR(\hat{d})))$$

$$\hat{u}_{2i} = \overline{comp}\ \overline{frozen2}\ sign(LLR(\hat{d}))$$
$$+ comp\ \overline{frozen1}\ \overline{frozen2}\ sign(LLR(\hat{d}))$$
$$+ comp\ frozen1\ \overline{frozen2}\ sign(LLR(\hat{c})).$$

As shown in Fig. 2, nodes are used in stage-1 , and and nodes are used in other stages to calculate the propagated LLR values. For simplicity of hardware design, the functions of and nodes are always implemented by unified processing elements (PEs) [11], [12]. Fig. 2 and 3 shows the architecture of this PE based on the LLR version of (16) and (23) with min-sum approximation. Here S2C is the block that performs the conversion from sign-magnitude form to 2's complement form, while C2S unit carries out the inverse conversion. Additionally, adder and subtractor are employed to carry out addition and subtraction between the two inputs.
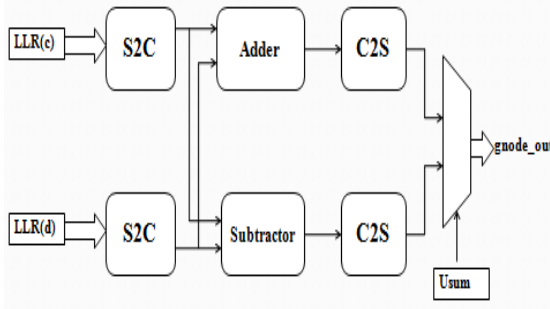

Fig 3: g-node architecture

The decision scheme in node has been described based on the LLR representation. To implement its function, a straightforward approach is to employ a sorting circuit and a signed adder. However, this method is too complex and is not hardware-efficient. After careful examination of Scheme-A, we observe that the node can be implemented with a very simple method, which is described as below.
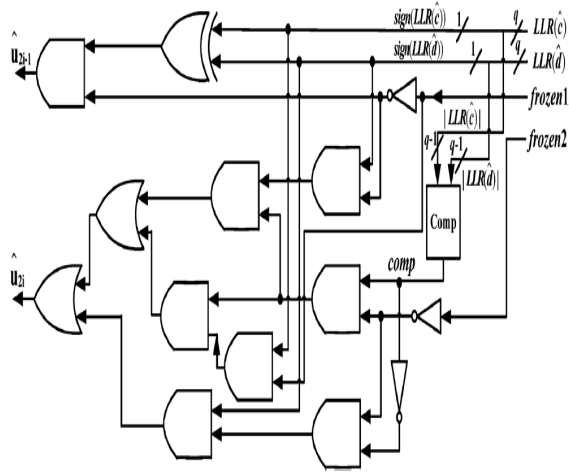

Fig 4: P-node architecture

III. EXPERIMENTAL RESULTS

3.1 Simulation Results

ModelSim tool is used to simulate the polar codes whether it is suitable or not then this tool is used to all the digital circuits. Run the polar codes and then finalize we check the operation of polar encoder. In this section, we consider the computational complexity of the SC decoding algorithm. In this section, three hardware architectures of the new 2b-SC algorithm are presented. According to Fig 5, the overall 2b-SC decoder mainly consists of three types of processing nodes: *f, g* and *p* nodes. Besides these nodes, a simple partial sum generator (PSG) is also needed to generate partial sum $\hat{u}_{sum}$. Since PSG block is similar to polar encoder with simple architecture, therefore in this section we focus on the architectures of *f, g* and *p* nodes. Here, u_{final1} and u_{final2} are output data.
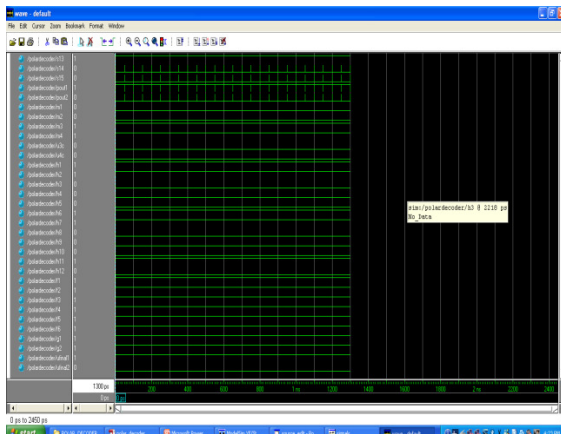
Fig 5: Result of polar decoder

3.2. Synthesized Report

Synthesis report gives the efficient usage of number of flip-flops used and bonded IOBs, number of slices used GCLKs and register used. Additionally, in order to demonstrate the advantage of the proposed architectures, we have implemented our designs for polar (1024, 512) code with Verilog HDL. Here tree-based 2b- SC- Precomputation architecture is selected for implementation.
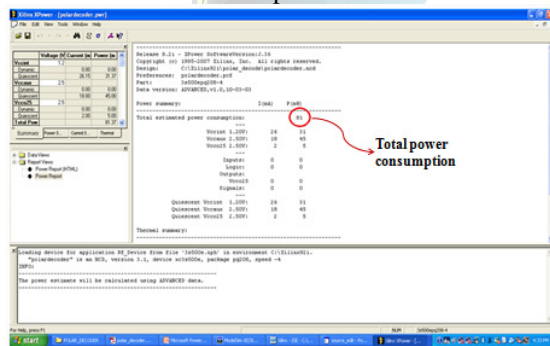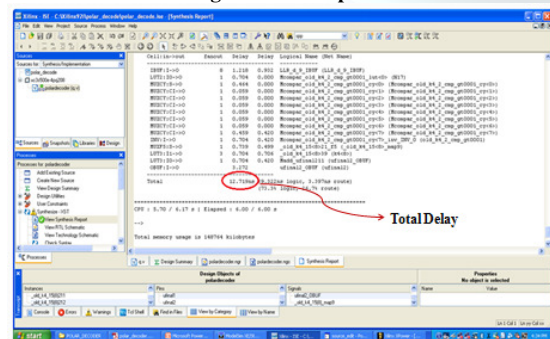

Fig 6: Power Report

Fig 7: Latency Report

3.3. Performance Analysis

In this section, we analyze hardware performance of the proposed 2b- SC architectures and compare them with the state-of-the-art designs. Table 1 lists the synthesis results of reported polar (1024, 512) SC decoders.

Performance Parameters	Proposed	Bo Yuan et al.,[2014]	C. Leroux et al.,[2013]	A. Mishra et al.,[2012]
Latency	12.719ns	76.7ns	208ns	156ns
Throughput	1.5Mb/sec	1.48Mb/sec	0.83Mb/sec	1.07Mb/sec
Power Consumption	81mW	-	-	-

Table 1: Performance analysis

IV. CONCLUSION AND FUTURE WORK

In this paper, a novel reformulation for the last stage of the SC decoding is proposed. Based on this reformulation, a reduced- latency 2b-SC decoding algorithm is presented. In addition, with the use of overlapped scheduling and precomputation approaches, the decoding latency of 2b-SC design is further reduced and also increased the throughput. It is shown that by this modification, significant latency and complexity reductions are achieved with no sacrifice in error performance. Comparison results have shown that the proposed architectures turn out to be very attractive for real-time applications. Polar coding is a recently discovered coding technique which is capable of achieving the symmetric capacity of binary discrete memoryless channels. This paper focuses on developing approaches for designing low-latency low-complexity channel decoder architectures for modern communication systems. Decoding latency (or throughput) and hardware complexity are the two main focuses of polar decoder design. In the future, it could like to extend my work in the following blocks in polar decoder architecture. First, two-stage estimator architecture will be introducing in polar decoder architecture which cancels the multi user interference and reduce the time consumption. Second, path decorrelator architecture will be designing, that is introducing between the p node and destination of polar decoder in communication system, which can be used to reduce the error in signal, power consumption and latency.

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