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Diminution of Harmonics in Cascaded Multilevel Inverter Using Particle Swarm Optimization Algorithmic Switching Angles

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Abstract: Harmonics are undesirable currents and voltages in the power supply system and the sources responsible for the undesirable harmonics are the nonlinear loads like rectifiers, inverters, solid state voltage regulators, cycloconverters and uninterrupted power supplies. This paper demonstrates how the Total Harmonic Distortion (THD) diminution in the output voltage of unique multilevel inverter is achieved. In multilevel inverters with a fundamental frequency switching strategy (each switch turning on and off once per output cycle), the optimum switching angles can be selected so that the output THD is minimized. To obtain the optimum switching angles, an optimization algorithm is applied to the output voltage. This paper deals with the analysis and simulation of a nine level inverter with new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter and can be extended to any number of levels. The harmonic reduction is achieved by selecting appropriate switching angles by particle swarm optimization algorithm. The functionality verification of a nine level inverter is done using MATLAB. To verify the simulation results, a nine level unique inverter based hardware prototype, including PIC microcontroller has been implemented. Both simulation and experimental results indicate superiority of this approach over the commonly used phase voltage THD minimization approach.

Index Terms-Particle swarm optimization (PSO), Unique Multilevel Inverter (UMLI), Total Harmonic Distortion (THD), Multilevel Inverter (MLI), THD diminution.

I. INTRODUCTION

Recently, elevated eminence power is desired for special applications to bring into being good quality results and for accurate evaluation. In this paper, an endeavor has been made to develop the superiority of power. An inverter of single phase nine level cascaded with identical dc supply is designed to reduce the harmonic components of the output voltage. Multilevel inverters persist obtains more concentration because of their high voltage operation ability, comparatively very small switching losses, elevated efficiency and very low electromagnetic interference (EMI),[3][4]. The desired output of a multilevel inverter is synthesized by several sources of dc voltages. With an increasing number of dc voltage sources, the inverter voltage waveform comes close to a sinusoidal waveform while using a low switching frequency scheme [3]. The low switching losses, due to several dc sources are used to create the total output voltage; all will produce low dv/dt compared to a single level inverter. Finally, the multilevel inverter equipment is a capable expertise for high power electric applications. Multilevel VSI using cascaded inverters with separate dc sources (SDCSs), compact but also requires the least number of output voltage levels without undue increase in power circuit complication.

An important key in designing an effective and efficient cascaded H-bridge multilevel inverter is to ensure that the total harmonic distortion (THD) in the output voltage waveform is small enough. The level of the dc sources was assumed to be equal and constant, most likely not to be case in application even if the sources are nominally equal. Generally three main types of multilevel inverters techniques without transformer; the flying capacitor inverter, the diode clamped inverter and the cascaded inverter. All share the same property, which is that the output filter can be dramatically reduced, and the usual bandwidth limit induced by the switching frequency can be reconsidered. Among these inverters, the flying capacitor inverter is difficult to be

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realized because each capacitor must be charged with different voltages as the voltage level increases.

This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed PWM technique. It has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge inverter for the same number of levels. The modes of operation of a nine level inverter are offered, this type of modes can be realized for increasing the levels. The inverter operation is controlled using switching angles based on PWM with help of pulse generator. The firing angles are obtained from solving the waveform equations using Genetic Algorithm. Simulation of the proposed inverter is performed using MATLAB. The response output of the proposed topology and the harmonic elimination method are verified experimentally.

II. NINE LEVEL INVERTER

2.1 Existing System of Nine Level Inverter

A single phase of this inverter made of four simple H-bridge inverters and each can produce three output voltages $+V_{dc}$, 0 or $-V_{dc}$, hence the whole inverter can generate nine voltage level. Every one of the H-bridge will be switched on and off only once each half cycle of the main harmonic. The output of inverter contains the harmonics produced by this way will be the main harmonic in addition to odd sine harmonics only. The diagram of conventional circuit of nine level cascaded inverter is shown in Figure 1. This multi-level inverter is made from several full-bridge inverters. The outputs for each different level of the full bridge inverters are connected in series so that the synthesized voltage waveform becomes the sum of the inverter outputs.

The firing angles of each switches α1, α2, α3, and α4 are calculated at different values of the main harmonics, for this reason we are able to reduce the values of the odd harmonics (5th, 7th, and 11th), using a selective harmonic elimination technique, [7][6]. All the undesired low order harmonics till the 11th harmonic are eliminated in the output voltage of the cascaded multilevel inverter.

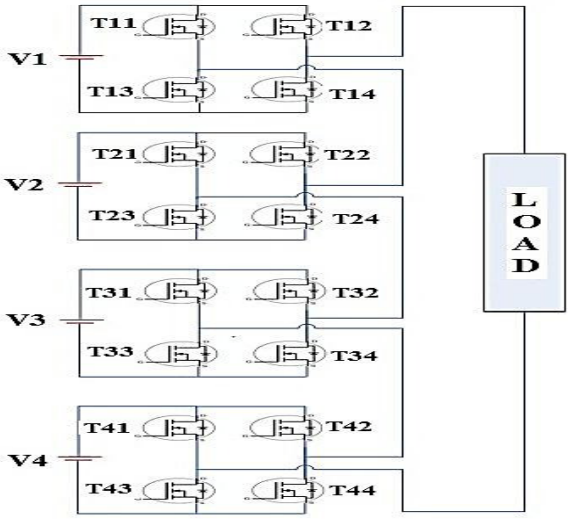

Figure 1 Conventional Nine level cascaded inverter

2.2 Proposed System of Nine Level Inverter

The proposed nine level inverter has the advantage of minimized number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. In the proposed inverter circuit consists of four dc source. The output terminal voltages of different level of inverters are connected in series. The ten switches, T1-T10, are combined differently and each inverter level can generate four different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series and produces the voltage waveform and will be the sum of the inverters outputs. A proposed single phase nine level inverter is shown in Figure 2.

The proposed inverter has four master switches in H-bridge configuration T1 to T4, and two slave switches T5, T6 and T7. The inverter performs the operation in three different mode of operation, namely powering mode, freewheeling mode and regenerating mode according to the polarity of the load voltage and current. These modes will be repeated irrespective of the number of the inverter output levels. The waveform of inverter output voltage and gating signals are shown in Figure.3.

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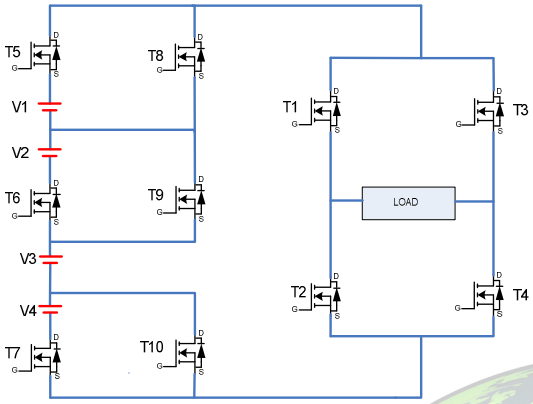

Figure 2 Power diagram of proposed Nine Level Inverter

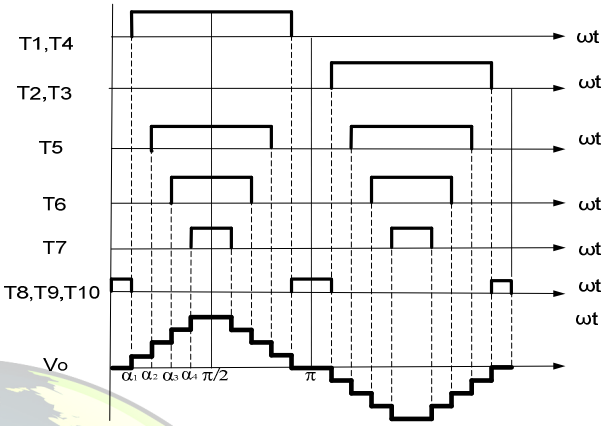

Figure 3 Output phase voltage waveform diagram

Like other conventional multilevel inverter, the number of levels proposed model can be extended to as required. The voltage level and switch states of proposed nine level inverter is summarized in Table 1.

Table 1 The Voltage level and switch states of proposed nine level Inverter

2.3 Calculating the Switching Angles

The switching angles of multilevel inverter are to be calculated and it will be equal to number of DC sources provided in the proposed inverter circuit. The DC source voltages are equal. The number of level is calculated from equation L = 2S+1, where S is the number of DC sources.

III. HARMONIC MINIMIZATION ANALYSIS

A programmed PWM technique is adopted to calculate the accurate switching angles to generate an output voltage with improved harmonic spectrum.

In order to obtain the fundamental output voltage without n harmonics, we are in need of n+1 equation. It can provide the control of the fundamental component beside the ability to eliminate or control the amplitudes of two harmonics, of necessity to be successive. This method of elimination will be presented for nine level inverter such that the solution for three angles is achieved.

The Fourier series expansion of the output voltage waveform, proposed inverter using fundamental frequency switching scheme shown in Fig.3 is equated below.

$$V(\omega t) = \frac{4Vdc}{\pi}\sum\left[\cos(n\alpha 1)+\cos(n\alpha 2)+\ldots+\cos(n\alpha S)\right]\left[\sin(n\omega t)\right] \quad (1)$$

Where n = 1, 3, 5, 7,...

Where s is the number of dc sources in the multilevel inverter.

Preferably, to determine the switching angles α_1, α_2, α_3,.... αs so that $Vo(\omega t)=V_1\sin(\omega t)$, fundamental voltage V_1 and a specific higher harmonics of $Vn(n\omega t)$ are equal to zero. To remove 5th, 7th, and 9th order harmonics, by solving the following equations the firing angles for each level can be calculated.

$$\left[\cos(\alpha 1)+\cos(\alpha 2)+\cos(\alpha 3)+\cos(\alpha 4)\right]=4Ma \quad (2)$$

O/P V_{out}	**Switch State**									
	T1	**T2**	**T3**	**T4**	**T5**	**T6**	**T7**	**T8**	**T9**	**T10**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
V_1	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
V_{1+2}	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
V_{1+2+3}	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
$V_{1+2+3+4}$	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
V_{1+2+3}	**0**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
V_{1+2}	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
V_1	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**

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$$[\cos(5\alpha 1)+\cos(5\alpha 2)+\cos(5\alpha 3)+\cos(5\alpha 4)]=0 \quad (3)$$

$$[\cos(7\alpha 1)+\cos(7\alpha 2)+\cos(7\alpha 3)+\cos(7\alpha 4)]=0 \quad (4)$$

$$[\cos(9\alpha 1)+\cos(9\alpha 2)+\cos(9\alpha 3)+\cos(9\alpha 4)]=0 \quad (5)$$

The modulation index Ma is given as

$$Ma = \frac{M}{S} \quad (6)$$

Where

$$M = \frac{V_1}{\left[\left(\frac{4V_{dc}}{\pi}\right)\right]} \quad (7)$$

and, where $0 \le Ma \le 1$.

The switching pulses are calculated from the above calculation. The solutions of the harmonic elimination equations by iterative numerical methods were considered to compute which give only one solution [8]. Polynomial equations will be solved using resultant such that all possible solution of (1) can be found. This procedure is known as elimination theory and uses the notion of resultants. Newton-Raphson method [6] is one approach to solving the set of nonlinear transcendental equations (1), is to use an iterative method, it is based on solving polynomial equations using the theory of resultants which produces all possible solutions [7]. Here the transcendental equations characterizing the harmonic content can be converted into polynomial equations. Finally the resultant method is employed to find the solutions. These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11th and 13th harmonics).

These are the non linear transcendental equations for eliminating lower order harmonics such as 5th and 7th order and get desired fundamental voltage [7]. For the given values of M (between 0 to 1), to get complete and all possible solutions of these equations for determining the switching angles and lower THD.

IV. Particle Swarm Optimization

Particle Swarm Optimization (PSO) is algorithms used to find optimal solutions to numerical and qualitative problems [6]. Russell Eberhart and James Kennedy introduced in 1995 motivated by social behavior of birds flocking or fish schooling and it can be easily implemented in most programming languages and has proven to be both very fast and effective when applied to a diverse set of optimization problem.

In PSO algorithm, the particles are "flown" through the problem space by following the current optimum particles. Every particle keeps track of its coordinates in the problem space, also which are associated with the best solution (fitness) that it has achieved till now. This implies that each particle has memory; this allows it to remember the best position on the feasible search space that has ever visited. This value is commonly called Pbest. Further another best value that is tracked by the particle swarm optimizer is the best value obtained so far by any particle in the neighborhood of the particle. The new location is commonly called Gbest. We should kwon the basic concept behind the PSO technique consists of change in the velocity (or accelerating) of each particle toward its Pbest and Gbest positions at each time step. It indicate that each particle strive to modify its current position and velocity according to the distance between its current position and Pbest, and further the distance between its current position and Gbest. Both the position and velocity vectors of the i^{th} particle of a d-dimensional search space can be represented as

$$Xi = (Xi\,1, Xi\,2, \ldots\ldots\ldots Xid) \quad (8)$$

&

$$Vi = (Vi\,1, Vi\,2, \ldots\ldots\ldots Vid) \quad (9)$$

On the basis of the value of the evaluation function, always the best previous position of a particle is recorded and represented as

$$Pbest\ i = (Pi\,1, Pi\,2 \ldots\ldots\ldots Pid) \quad (10)$$

If the g^{th} particle is the best among all particles in the group so far, can be represented as

$$Gbest = Pbest\ g = (Pg\,1, Pg\,2 \ldots\ldots Pgd) \quad (11)$$

The particle tries to modify its position using the current velocity and the distance from Pbest and Gbest . Further the modified velocity and position of each particle for fitness evaluation in the next iteration are calculated using the following equations

$$v_{id}^{k+1} = w \times v_{id}^{k} + C1 \times rand\,1 \times (Pbestid - x_{id}^{k}) + C2 \times rand\,2 \times (Gbestgd - x_{id}^{k}) \quad (12)$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (13)$$

Where w is the inertia weight parameter and it controls the global and local exploration capabilities of the particle. $rand_1$ and $rand_2$ are random numbers between 0 and 1. For the proposed method, C_1=2, C_2=2. Where a large inertia weight factor is used during initial exploration and its

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value is gradually reduced as the search proceeds. Here concept of time-varying inertial weight (TVIM) is given by.

$$w = (w\max \times w\min) \times \frac{iter\max - iter}{iter\max} + w\min \qquad (14)$$

$$w_{\max} = 0.9 \quad ; \quad w_{\min} = 0.4$$

Where iter $_{max}$ means maximum number of iterations.

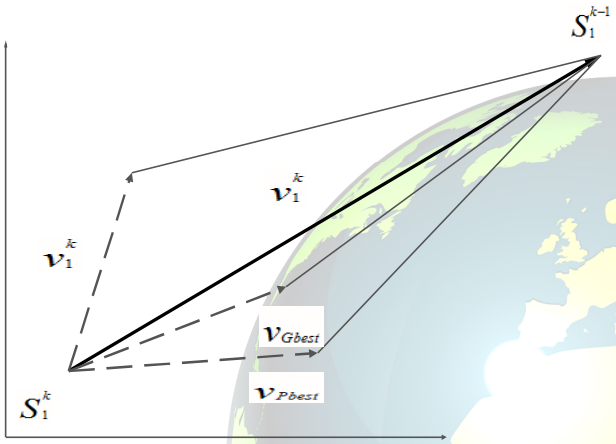

Figure 4 Concept of modification of searching point

V. The Proposed PSO Algorithm

The minimization of THD in multilevel inverters is achieved by using this PSO algorithm because of its simple in nature and easy to implement, computational efficient. The procedure for getting optimized results the objective function is taken as the THD equation is as follows

$$\%THD = \frac{\sqrt{(V_2^2 + V_3^2 + \ldots + V_n^2)}}{V_1} \qquad (15)$$

The proposed PSO algorithm is given as following steps:

Step1: create the random initial population size of switching angles by considering their limitation is 0 to π/2

Step2: initialize the velocity, Pbest, Gbest, iteration count for computing switching angles

Step 3: update the iteration count

Step 4: update the velocity and position according to the equations (8) & (9) for moving of particles in search space

Step 5: evaluate the fitness or objective function by using equation (15)

Step 6: update the values of Pbest and Gbest

Step 7: Is criterion achieved then go for next step otherwise repeat the step3 to step6 for best solution

Step 8: select the best solution of fitness value.

In this process the maximum iterations are 100 and the population size is 20 and using the decreasing inertia function with initial weight of 0.9 and final weight of 0.4. This proposed algorithm is mainly used to minimize the total harmonic distortion for selected initial random switching angles. For getting lower value of total harmonic distortion and minimization of lower order harmonics the objective function is taken as a total harmonic distortion equation.

For every iteration the value of the THD is updated for their suitable best values by changing the velocity and position of the current particles. Similarly the values of switching angles also updated for optimum values to get lower value of THD

Comparison of switches used and THDs in the phase voltage of both the system is summarized in table 2.

Table 2 Comparison of switches used and THDs

TYPE OF MULTILEVEL INVERTER	NO OF SWITCHES USED	THD $_{Phase}$ (%)
CASCADED H BRIDGE	16	10.27
CASCADED BRIDGE (Proposed)	10	9.03
% REDUCTION	37.50%	12.07%

VI. Simulation Results

The probability of the proposed approach is verified using software simulations. A simulation circuit of nine level inverter was created in MATLAB-Simulink software with new method with reduced number of switches is employed. The proposed inverter has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter. The schematic diagram of cascaded H bridge nine level inverter and proposed new nine level topology built in MATLAB-Simulink is illustrated in Fig. 5 and Fig. 6 respectively

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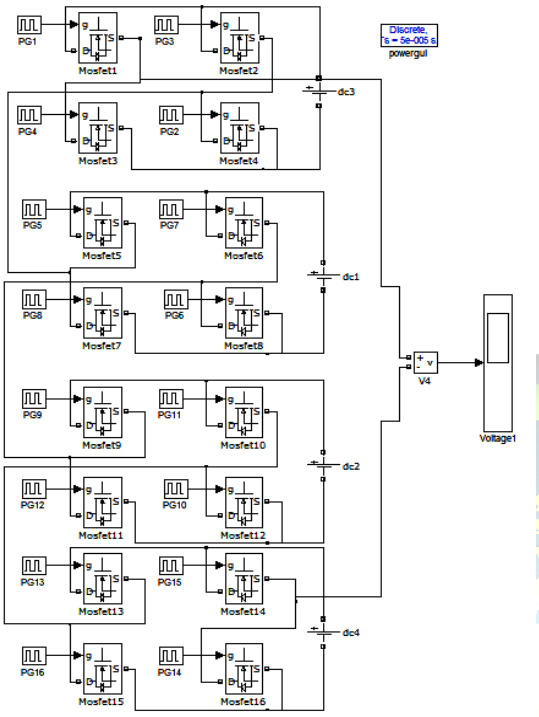

Figure 5 Simulation diagram for cascaded H bridge nine level cascaded inverter

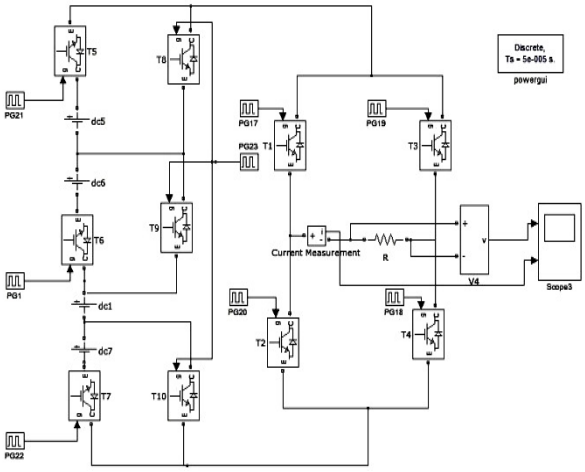

Figure 6 Simulation diagram for proposed nine level cascaded inverter

The proposed nine level inverter is simulated with the implementation of switch reduction scheme. The input voltage is given as 24V DC supply to the inverter and R and RL load. The output voltage waveform of nine level inverter is shown in Figure 7.

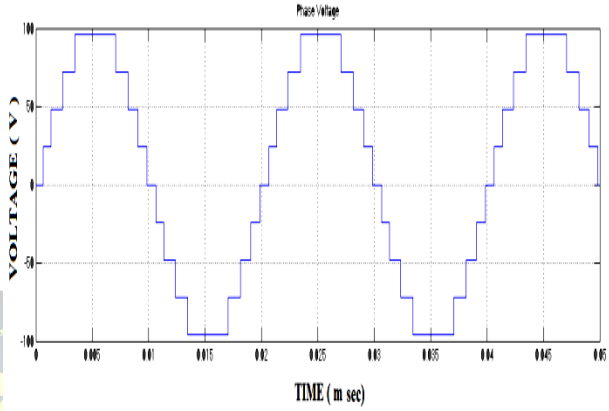

Figure 7 Output voltage waveform of nine level inverter

The output current waveform of nine level inverter on resistive load is shown in Figure 8.

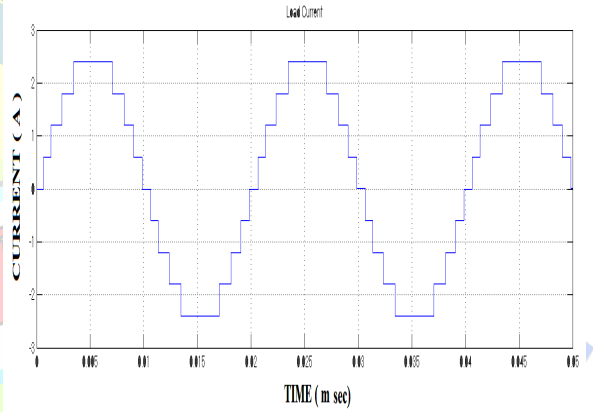

Figure 8 Output current waveform (Resistive Load)

The output current waveform of nine level inverter on inductive load is shown in Figure 9.

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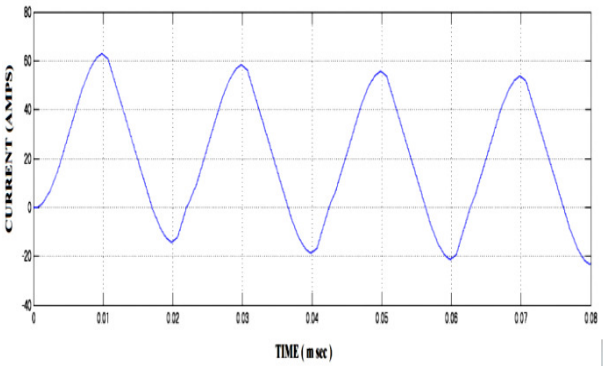

Figure 9 Output current waveform (inductive load)

The gate pulses generated from the control circuit for the switching devices shown in Figure 10.

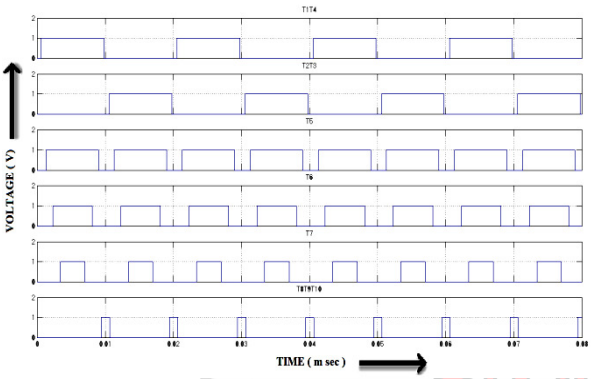

Figure 10 Gate pulse of switching devices

The frequency spectrum of output voltage is shown in Figure 11.

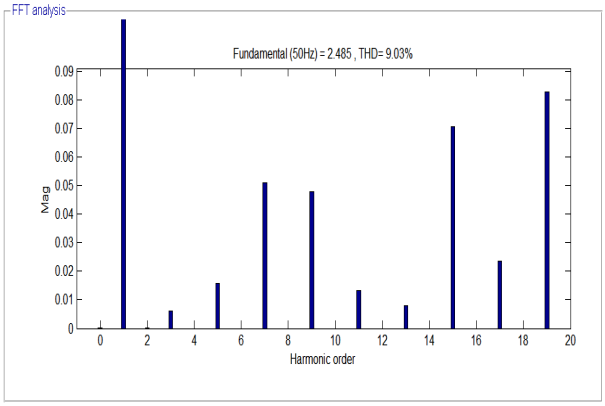

Figure 11 FFT analysis

VII. CONCLUSION

The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 9.03 at 96V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.11, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

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