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A Reliable Process-Sensitive Tolerant Hybrid Sense Ultra Power SRAM Amplifier

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Abstract: — Power consumption has become a critical design concern for many VLSI systems. In this proposed system we use Sense amplifiers are one of the very important peripheral components of CMOS memories. In a Hybrid Sense amplifier both current and voltage sensing techniques are used which makes it a better selection than a conventional current or voltage sense amplifiers. To increase the memory density, bit cells used reduce the area. Power consumption and speed is the important issue to minimize the power value by using cell read and stability value. This paper is also investigating the read static noise margin, write noise margin and read retention voltage. Tanner EDA tool is also used to observe the schematic solution. This method will decrease the power consumption and increase the stability of the SRAM cell.

Keywords: SRAM, Power gating, Voltage Sense Amplifier (VSA), Current Sense Amplifier (CSA), Dynamic Stability.

I. INTRODUCTION

In this paper we introduce some design techniques to reduce the power consumption and increase the stability f the cell. Each cell contains some transistors. Existing method we use 6T SRAM cell. Stability of the 6T SRAM cell is poor. Measuring the cell current by change cell structure. It will damage the circuit and reduce the stability and increase the losses. But in this method we accurately estimate the cell stability of the SRAM cell without modifying the cell structure. Existing system 32nm devices are used. The estimation results focused on the random manner. It will not display the final result. Random mismatches are occurs in the wafer. As the temperature is increases stability of the read mode and sleep mode deceases.

In the proposed method we use the Sense amplifiers are one of the most essential circuits in the periphery of CMOS memories. The performance of sense amplifier affects both memory access time and overall memory power dissipation. CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These goals are conflicting when it comes to sense amplifier design. In an integrated circuit a memory is attached to number of peripherals which would use the contents of the memory, but the potential developed at the output nodes of the memory (6T SRAM) is too low to drive the peripheral circuitry, hence the need of a sense amplifier comes into picture. It senses a low signal and amplifies it to appropriate level. But most of the techniques are not directly applied to the SRAM cell. But this paper estimates the read and writes stability.

II. BACKGROUND

A. Static Noise Margin

Read static and write noise margin are the extended definitions of the SNM. These two terms are defined as the, maximum tolerable noise injected onto the cell.

B. Read Retention Voltage

Supply read retention voltage is highly correlated. This technique can be used to extracts the cell read stability without changing the cell structure.6T SRAM cell read stability requires to sweeping the internal nodes in order to obtain the voltage transfer curvatures. Large are used to choose the Supply Read Retention Voltage.

6T SRAM cell structure we use two CMOS inverter. Word line used to control the circuit. 6T circuit are contains Pull up and Pull Down transistors. Other two transistors are called as the access transistors. Voltage division between the access transistor and driver transistor read stability to be low during the read operation. Leakage current is flows through the NMOS transistor. It will increase the source to supply voltage. More than one transistor is off means the path between the supply voltage to ground is equal.

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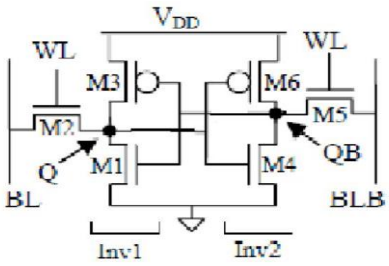

Fig.1. SRAM cell Write Stability

Random telegraph noise is occurs in 6T SRAM cell. The noise caused by the charge trapping or re trapping. SRAM transistor area will increases in the trapping method.Cell current is measured in two ways. Pull of NMOS devices and Pull down of NMOS devices Additionally we used as the access transistor.

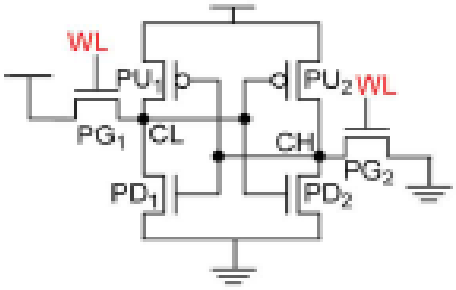

Fig.2. SRAM cell Read Stability

Most of the stable cells are measuring the pull down current. Implementing this technique in a COM SRAM chip extra cost for the area measurement without changing the cell structure. It is the biggest disadvantage 6T SRAM cell. Reduce the cost and Power dissipation and power gating Techniques.

Power gating is the circuit design techniques which reduce the static power. Inserting the power switches in the supply path and it widely used in the industrial side. There are the two implemented design schemes of power gating techniques. Coarse grain power gating in which the blocks are disconnected.

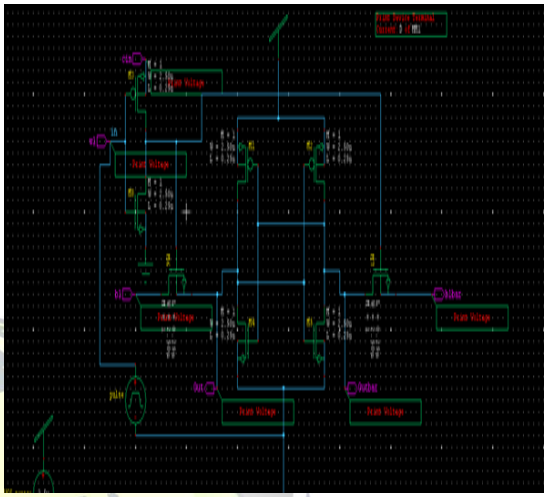

Fig.3. 8T SRAM Structure

The sleep transistor connected internally in the standard cell. With Sleep transistor inserted in series with the supply voltage or current source to reduce by power.

Power consuption of the MCML gte is independent of switching frequency, and it is given by
$P=V_{DD}*Iv$

Reducing the supply voltage is an effective method to lower the power consumption of MCML circuits.The operation of the MCML is based on the redicrecting or switching.

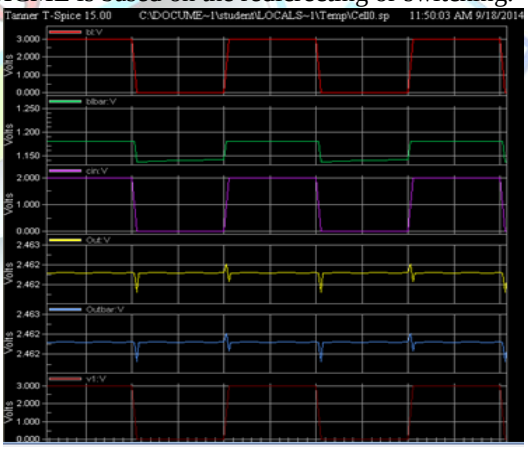

Fig 4:output Waveform 8T SRAM Cell

When applying the ON signal to the gate current source that will connects the bulk voltage to the bias voltage.

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III. HYBRID SENSE AMPLIFIER

Voltage Sense Amplifier (VSA) is a latch, made with two cross coupled CMOS inverters, providing full voltage swing (0 to V*dd*) at the output terminals with very less voltage at the input nodes. The voltage at the input of VSA should be greater than the offset for correct results and proper detection. If this is not the case then the bit line voltage swing becomes larger and directly affects the speed, power as well as the word line activation time. This architecture is a popular choice due to its simple design. Moreover it is differential type circuit same as that of a 6T SRAM cell, so it can be directly and easily used with the SRAM cell. Current Sense Amplifier (CSA) is generally used for high Speed applications.

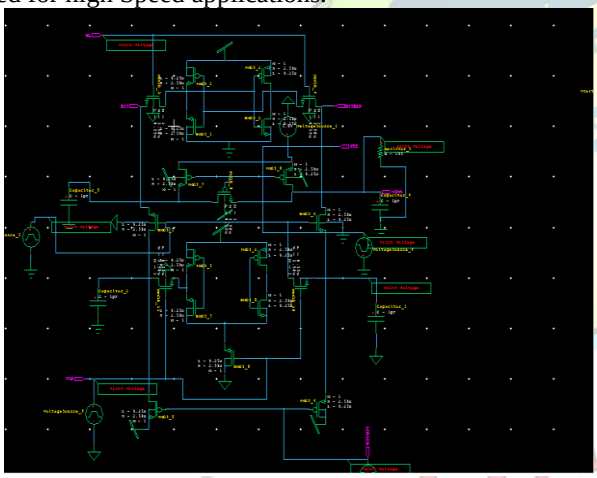

Fig 5 Shows the Hybrid Sense amplifier SRAM circuits

Current mode sense amplifier is efficient in power and speed. Even though we need more efficient in speed and power consumption use hybrid mode sense amplifier. Hybrid mode sense amplifier combines the operation of voltage and current mode. Hybrid Sense amplifier works in three phases.

First phase is offset cancellation phase. In this phase offset is cancelled by making the bit line precharge to equal potential. During this phase word line is inactive. Sense a and sense b is active. Output of M3 and M4 are tied to V_{DD}.

Second phase is access phase. In this phase the word line is get activated and sense b signal is deactivated. During the evaluation phase amplifier signal goes high making offset cancellation better cancellation is obtained.

P6 and P7 bit lines are pre charging. It will operate based on signal write enable. P8 and P9 write bar to make connection between memory cell and latch. P13 and P14are equalize the delay.

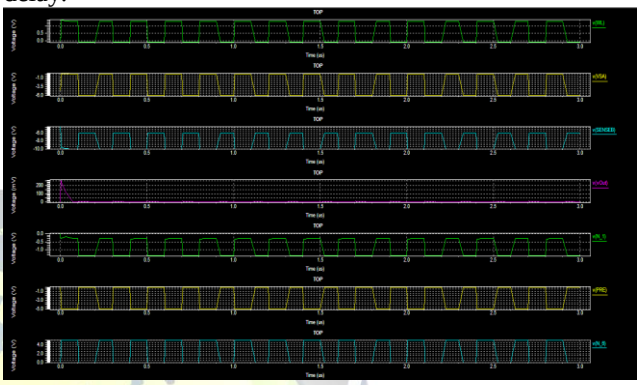

Fig.6 shows output waveform of hybrid sense amplifier

M1 has more threshold voltage than M2, hence BITB line charges slowly than bit BIT line.

IV. CONCLUSION

Standby power is the biggest drawback of the CMOS circuits. The active power consumption of the circuits can reduce the near threshold value. While the standby power is large. We use the hybrid sense amplifier to reduce the standby power of the circuit. It will increase the speed and efficiency of the SRAM cell. The Hybrid sense amplifier circuit 512 columns are analyzed by using 25nm technology.

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