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Design and Development of FPGA Based Flaw Exposure on Industrial Oil Pipeline Images

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Abstract: The image processing based flaw exposure algorithm developed on Hardware. The software based image processing has complexity in real time processing. The oil pipeline industry needs the weak spot detection in pipeline to avoiding the explosion and leakage. So we need the hardware solution blown away the problem. The trendy VLSI (Very Large Scale Integration) provides the Spartan 3E Embedded Development board for implementing this algorithm. This flaw exposure algorithms accuracy is high. The oil pipeline weak spot (flaw) detected by the flaw edge detector and dilation operator. Algorithm is implemented on FPGA by converting the image into text format. The proposed system is using Spartan 3E Embedded development board and Xilinx Platform Studio (XPS), before that the image can be converted into text file. After, completing the process the output can be converted into image using Visual basic software.

Keyword: Flaw, FPGA (Field Programmable Gate Array), Spartan 3E, XPS, Flaw edge detector

I. INTRODUCTION

The image processing is one of the fields in the world. These can be processed in medical, satellite and industrial domains. Most of the image processing algorithm implemented in software only. The software is also creating the complexity in real time implementation. Software processed in serial manner [1].The modern VLSI technology is attractive solution for image processing [2].

The hardware technology overcomes the software problems. In this way provides possible implementation in real time [2] image works. Low power, efficiency output, area efficient was offered by FPGA. The FPGA has processing the algorithm with required time consumption, due to the architecture in pipelining and parallel processing [3].Efficient performance in FPGA compared to DSP(Digital Signal Processor) and microcontrollers. FPGA should be manufactured by several vendors, like that Xilinx (Virtex, Spartan), Quartus (Altera), Actel. The major image processing algorithms are processing on Spartan 3E, Virtex series, Altera [4]. The prewitt, Roberts, Sobel edge detector on FPGA board does not suitable for the noisy input images. The latency time is increased it decreasing the performance of edge detection in real time. The advantage of canny edge detector is suitable for noise images but it hardware processing time is high.

To improving the flaw exposure algorithm the Flaw edge detector detects the edge in the images. To removing the unwanted edge the dilation operator used. These FPGA Provides the faster execution. FPGA supports HDL (Hardware Description Language).The HDL code may be written in handle-C, Verilog, VHDL. However, Handle-C based platform provides less coding lines compared to Verilog and VHDL [7].

In oil pipeline system weak spots can be identified by the Non-destructive testing, and eddy current method sensors and image analysis. But these methods are time consuming and more power consumption and less accuracy output. Modern technology FPGA hardware provides affordable solution for implementing the flaw exposure algorithm, The method improve the accuracy and less time and power consumption. These paper testing the crack from web source oil pipeline images. The crack and weak spot detection is to avoiding the explosion and leakage of oil.

The discussing the exposure of flaw by using flaw edge detector to detect the edge in text file input and filtered the unwanted details by dilation operator. The algorithm is in Spartan 3E Embedded Development Kit with XPS development tools .The advantage of development tool which is automatically generate the own peripheral and block diagram of the system. It automatically crate plat generation of the algorithm. It needs the less procedure for dumping the code on board. The output of image stream had viewed by Visual basic window.

The section I in paper discussed the existing and literature survey points are remembered. The section II and III will discussing the related work of existing and proposed system algorithms and flow chart works. The Experimental results are discussed in section IV. Finally, we will discuss of flaw exposure algorithm and future enhancement of this proposed system.

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II. EXISTING SYSTEM

In existing of flaw exposure algorithm is in image processing level only. The paper target the Hardware solution using FPGA.The FPGA based system mostly implemented on real time video and image processing. In real time processing it gives excellent output and fast processing.

The FPGA based real time object detection system which having expected results. The MATLAB Simulink model like edge detection, Median filtering and edge enhancement techniques which automatically generate HDL code for FPGA implementation, These are giving area efficient and low power operation. It also offers the multiple work at a time also possible. The existing system VHDL based coding methods somewhat difficult approach, so we can using the handle c HDL code.

III. PROPOSED SYSTEM

The proposed system using Flaw edge detector and dilation closing operator to enhancing the flaw result in the image. The Flaw edge detector process the text file input detect the edged as in form of text file.

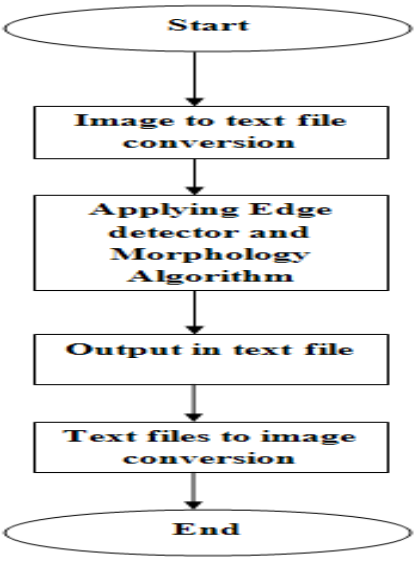

Figure1: Flow chart of proposed system

Again the text files to separate flaw pixel to applying the dilation. After completion of this process we need to convert the text file into image.

A. Algorithm:

Step1: Image to text files conversion

Step2: Write the HDL code and simulate it. After successful completion of code to configure the device.

Step3: Dump into Spartan 3E board.

Step4: FPGA processing the algorithm, converting the text file into image.

Step1 procedure: The text files conversion procedure is shown in the figure1 flow chart. In first step to pick the image from the file, after that it can be converted into Gray image. Third step print the each pixel value into text input and it can be stored as header file.

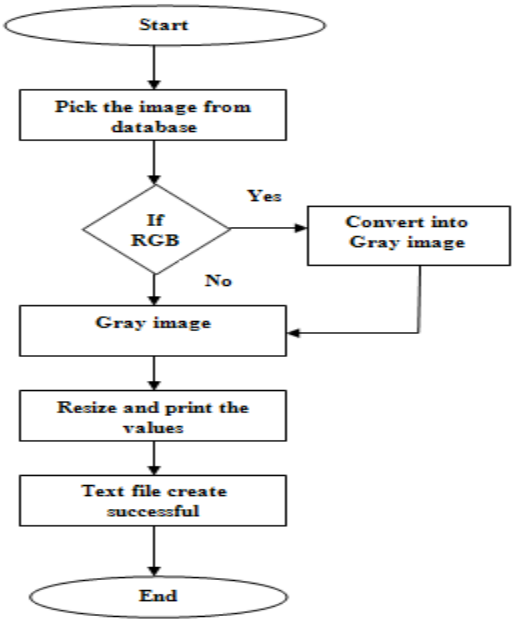

Figure2: Flow chart of Text files conversion

The resultant image of text file is shown in figure 3and figure4.

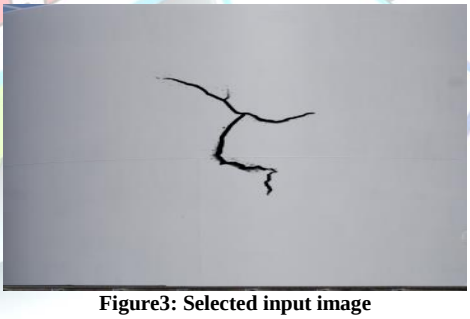

Figure3: Selected input image

Step2 & 3 Procedure: Writing the code and simulate it and dump into FPGA board. The Step 2&3 procedure is shown in figure 5.

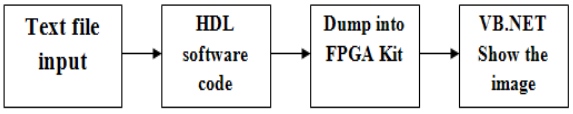

Figure 4:Step3 and 4 Block diagram

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FPGA Spartan 3E having following benefits, such that it supports Verilog, VHDL, Handle-C structure of coding. It performs JTAG programming. The FPGA can be process these flaw detection algorithm using LUT (Look up Table), Flip-Flops, Memories like RAM, ROM, SRAM. The image processing application Spartan 3E embedded development board offers better solutions. The Spartan 3E embedded development board Kit diagram is given in figure 6.

Figure5: Spartan 3E Embedded development kit

Step 4 Procedures: The fourth step to convert text file into image. That block diagram is shown in figure 7.

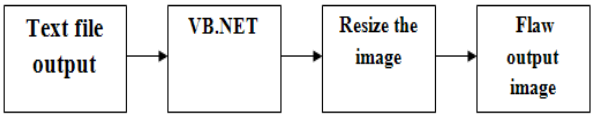

Figure6: Step4 Block diagram

B. Hardware Work Flow: The edge detection is one of the parts of image processing application. The edge detection is representing edges in the images. Proposed system is under categorized into computer vision. The computer vision detects the faults in machine parts, leakage detection, oil pipeline crack and weak spot detection.

The proposed system flaw edge detector which using the horizontal gradient and vertical gradient to detect the edges in the image, combined it to calculate the final edge in the text file. The edge resulting some unwanted portion to calculate the required output by applying dilation operation is to the text file edge output. The hardware two blocks RAM are used, one can be act as input buffer, other block RAM act as output buffer.

The Block RAM input buffer the header file (text data of image) and executable linkable file (algorithm) code. Then processing algorithm the text file output stored in block RAM output buffer. It can read text value one by one and visual basic window display text file data into image.

IV. EXPERIMENTAL RESULTS

In the flaw detection algorithm we check the test bench waveform for each eight bit input. The Register transfer level diagram is also referred the expected result of flaw exposure algorithm are given in the below figure8. The input image loading is given below. The text box shows the reading pixel value at a time.

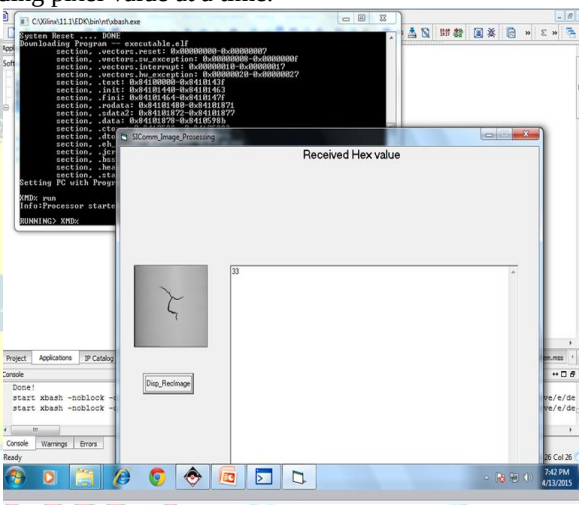

Figure7: Input image (Text to image conversion)

After completion of image loading we process the algorithm on text file and final flaw on text file obtained and converted by image using VB window.

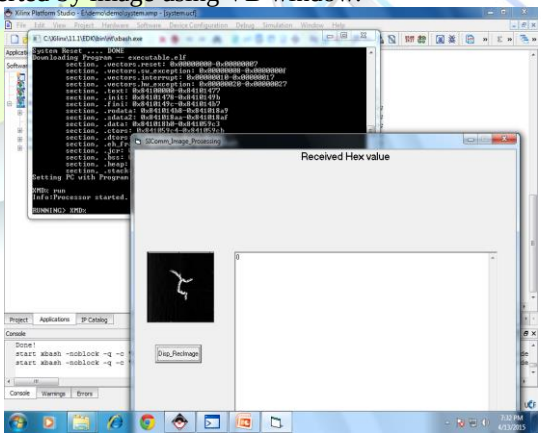

Figure8: Expected Flaw exposure output

The final dilation exposure output is in figure9.The execution summary of algorithm is shown below. Here I have given only the input and output flaw image diagram only.

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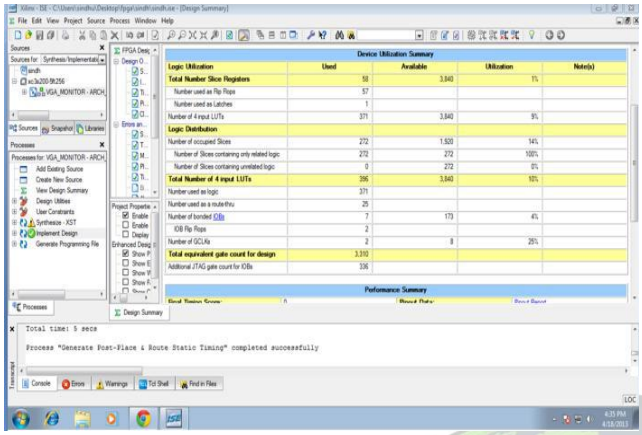

Figure9: Execution summary

V. CONCLUSION

The flaw exposure algorithm on oil pipeline images are successfully implemented on Hardware and also these flaw exposure algorithm needs the low latency time and improving the performance of edge detection of flaw identification in the text file .The proposed algorithm aims to reducing the processing time of flaw exposure algorithm, to convert the text file into image the visual basic software used instead of MATLAB, if the project is implemented in real time.

These flaw exposure algorithm implemented in Spartan 3E Embedded development board and future scope implement these flaw detection algorithm on different FPGAs and comparing the memory utilization, speed and time performance. These presented paper getting the expected accuracy result. When, will improving the result using Virtex 5, Altera giving fast execution time. Replacing the edge detection into clustering methods improve results more.

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