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Design and Implementation of Truncated Multiplier in FIR Filter

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Abstract: Low-cost finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multiplier. This multiplier design is usually considered where the maximum absolute error is no more than 1 unit of least position. And also this truncated multipliers offer significant improvement in area, delay and power. The proposed method jointly consider the deletion, reduction, truncation and rounding of partial product bits in order to minimize the number of full adders and half adders during tree reduction. In addition, the truncated multiplier design also has smaller delay due to the smaller bit width in the final carry-propagate adder. In previous papers truncation error is reduced by adding error compensation circuits in fixed width multiplier to get a précised output. But here, there is no need of error compensation circuits and the final output will be precised. The proposed filter using truncated multiplier will be designed using Verilog HDL and synthesis using ISE Simulator (ISIM) and simulate it using MODELSIM ALTERA 6.4a (Quartus II 9.2i).It achieves best area and power result when compared with previous FIR design approaches.

Keywords: low power and area truncated multiplier, DSP, VLSI design, FIR filter Design, partial products.

I. INTRODUCTION

MULTIPLICATION of two numbers generates a product with twice the original bit width. It is usually desirable to truncate the product bits to the required precision to reduce area and cost, leading to the design of truncated multipliers or fixed-width multipliers. Fixed-width multipliers, a subset of truncated multipliers, compute only n most significant bits (MSBs) of the $2n$-bit product for $n \times n$ multiplication and use extra correction/compensation circuits to reduce truncation errors.

There are, in general two truncated multiplier design methods, namely constant and variable corrections, depending on how to compensate the error introduced due to the elimination of the least significant partial product (PP) bits.

In some applications like the design of FIR filter in digital Signal processing (DSP) we need truncated multipliers with accuracy of faithful rounding which means that the maximum absolute error after truncation is less than 1 unit of least position (ulp). In these applications, we need to control the computational accuracy of every individual hardware component, including multipliers, so that the total computation error meets the final target precision.

Finite impulse response (FIR) digital filter is one of the fundamental components in digital signal processing and communication systems. It is also widely used in many portable applications with limited area and power budget.

The proposed system presents a truncated multiplier design that can achieve faithful rounding results. Unlike previous related papers that manage to add some compensation circuits to reduce the truncation error, our new approach jointly considers the tree reduction, truncation, and rounding of the partial product bits during the design of fast parallel truncated multipliers so that the final truncated product satisfies the precision requirement.

II. TREE REDUCTION OF PARALLEL MULTIPLIERS

A tree based multiplier design usually consists of following major steps, i.e., PP (partial product) generation, PP deletion, PP reduction, truncation, rounding and final carry propagate addition. PP generation produces PP bits from the multiplicand and the multiplier. The goal of PP deletion and reduction is to delete some PP's and compress it, which is to be summed up by the final addition.

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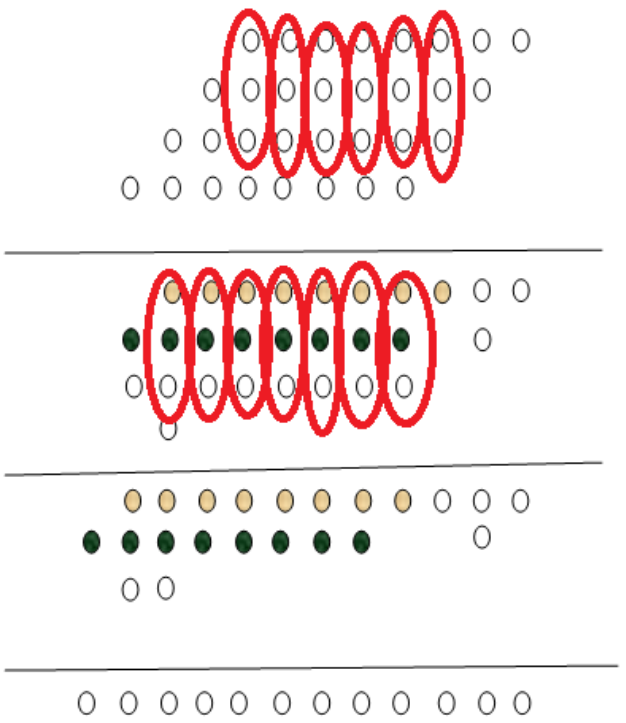

Figure 1 Major steps

Here we achieve around 33% area optimization and 20% Fmax enhancement with the same performance.

The two most famous reduction methods are Wallace tree and Dadda tree reductions. Wallace tree reduction manages to compress the PPs as early as possible, whereas Dadda reduction only performs compression whenever necessary without increasing the number of carry-save addition (CSA) levels. Here we design a multiplier based on Wallace tree only.

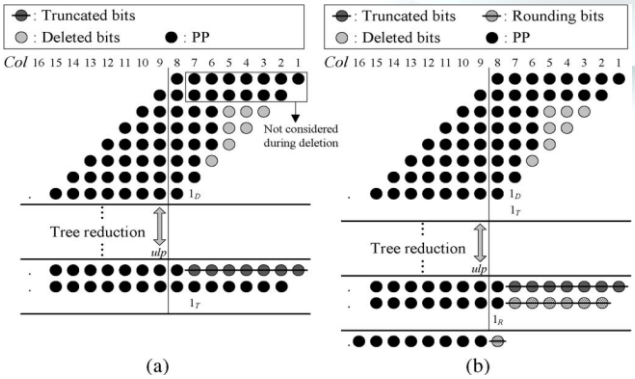

Figure 2 proposed optimization

III. Deletion, Reduction, And Truncation

In the first step, we perform the deletion that removes all the unnecessary PP bits that do not need to be generated, as shown by the gray dots in Fig. 2 for an example of 8×8 unsigned fractional multiplication with eight product bits truncated. In this step, we delete as many PP bits as possible, for as long as deletion error E_D is bounded by $-1/2$ ulp $\leq E_D \leq 0$. After injection of a correction bias constant of 1/4 ulp, as shown by 1*D* in Fig.2 (a)

$$\frac{-1}{4}ulp < E_D \leq \frac{1}{4}ulp$$

The deletion error after the bias adjustment is note that the deletion of PP bits starts from column 3 by skipping the first two rows of PP bits because after applying reduction, the resultant two rows will be removed in the subsequent truncation and rounding processes to be described later.

After the deletion of PP bits, we perform the per-column reduction of Scheme 2, as mentioned in Section II, and generate two rows of PP bits. After reduction, we perform the truncation that further removes the first row of $n - 1$ bits from column 1 to column $n - 1$, as shown by the crossed gray dots in Fig.2.This step of truncation introduces truncation error as

$$\frac{1}{2}ulp < E_T \leq 0$$

Again, after injecting another bias constant of 1/4 ulp, as shown by 1*T* in Fig.2, the adjusted truncation error is bounded by

$$\frac{-1}{4}ulp < E_T \leq \frac{1}{4}ulp$$

IV. Rounding And Final Addition

After deletion, reduction, and truncation, the PP bits are added using a CPA to generate the final product of *P* bits, as shown in Fig. 2(b). Note that the bits in column 2 to column $n - 1$ [as highlighted by crossed spotted dots in Fig. 2(b)] can be safely removed before CPA because these bits are the only bits left in the columns after the deletion and truncation processes, and thus, they do not affect the carry bit to column $n + 1$ (the column with a weighting of 1 ulp) during the rounding process. Before the final CPA, we add a bias constant of 1/2 ulp, which is shown as 1*R* in Fig. 2, in order to achieve the round-to nearest rounding with the rounding error.

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$$\frac{-1}{2}ulp < E_R \leq \frac{1}{2}ulp$$

The bit at column n after the final CPA is also removed during the rounding process. Thus, the total error for the design of the faithfully rounded truncated multiplier is bounded by

$$-\text{ulp} < E = (E_D + E_T + E_R) \leq \text{ulp}$$

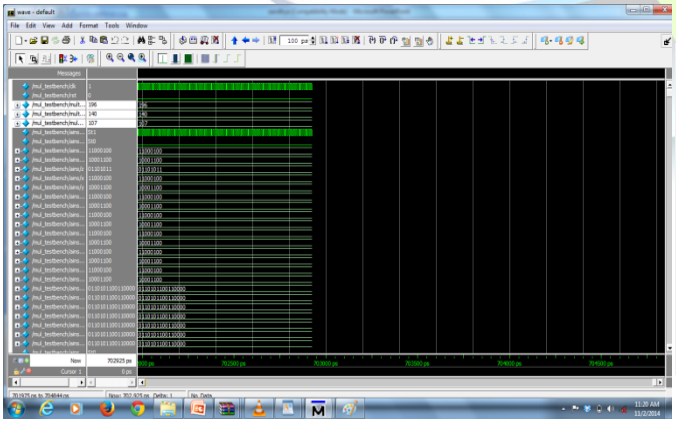
Note that the proposed truncated multiplier design achieves faithful rounding because the total error is no more than 1 ulp. Furthermore, the three bias constants, i.e., $1D$, $1T$, and $1R$, can be collected into a single constant bit to be added at column $n + 1$, without increasing the overall height of the PP matrix.

V. Multiplier In Fir Filter

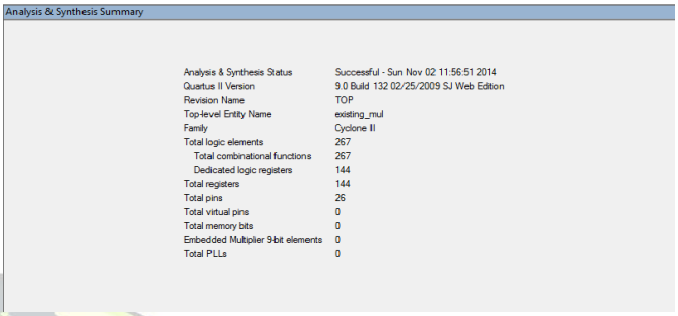
IN FIR filter design filter coefficients in the form of fraction numbers. For any digital filter design corresponding coefficients will be used as a integer after fraction number into binary conversion. This will lead quantization error and during multiplication truncation error will occur**.** Here the truncation error is reduced by adding error compensation circuits in fixed width multiplier to get the precise output. So the area and Complexity of the process is increased. So to overcome this problem we design FIR filter based on direct truncation with tree based (Wallace tree) this will surely reduce the area used in FIR filter.

VI. Experimental Results

A. Model Sim Output: Direct Truncation



B. Quartrus Ii 9.0 Web Edition Output Area Utilization Report



C. Power Analsis

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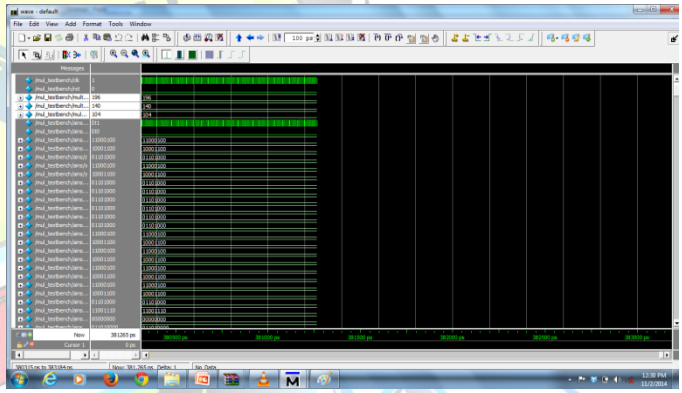
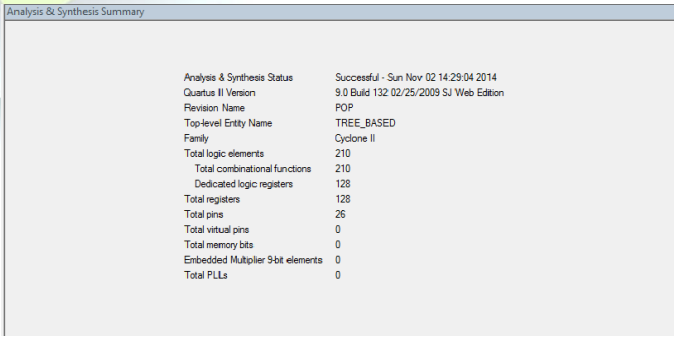
D. Modelsim Output Tree Based Truncation



E. Quartus Ii 9.0 Web Edition Output Area Utilization Report



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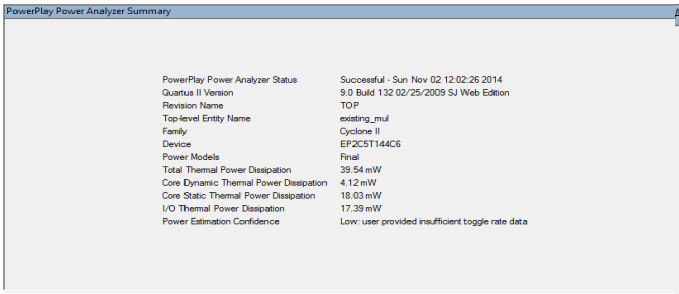
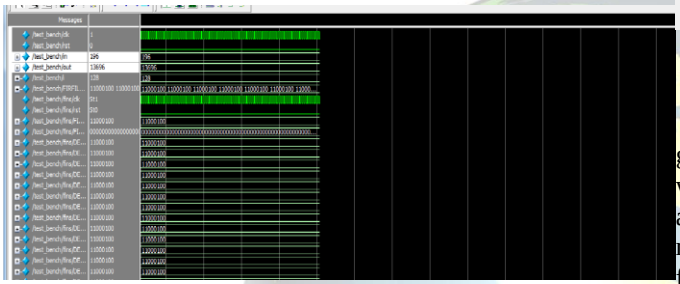
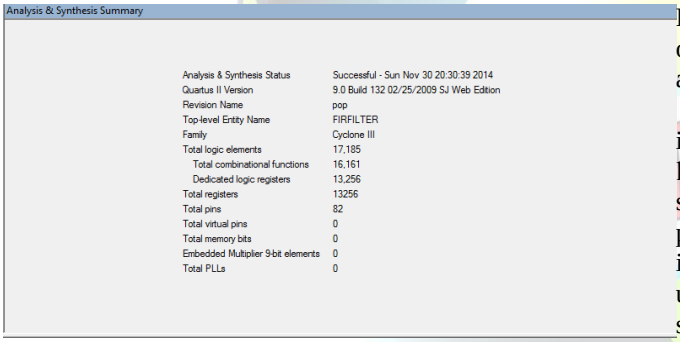
F. Power Analysis



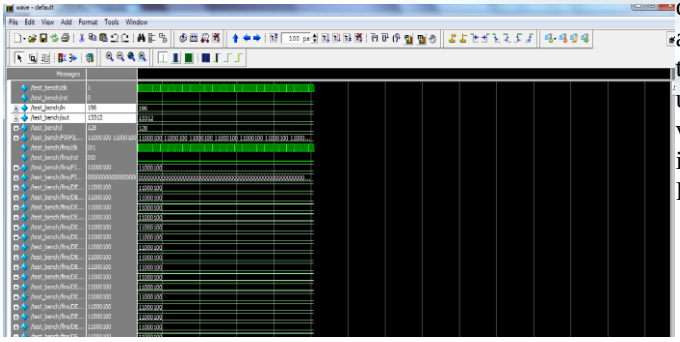
G. FIR Filter Output Direct Truncation



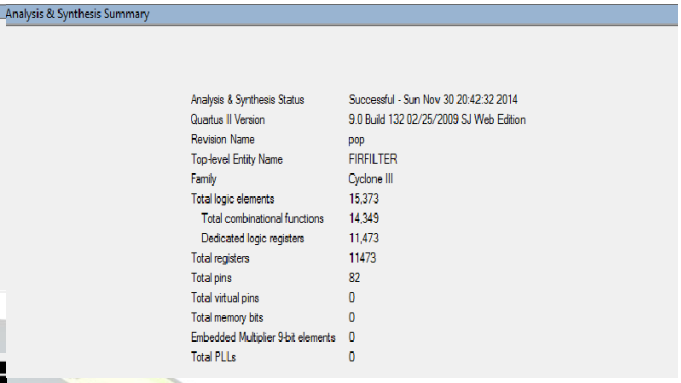
H. Area Utilisation



I. TREE BASED TRUNCATION



J. Area Utilisation



VII. CONCLUSION AND FUTURE WORK

It is concluded that tree based truncation in FIR filter gives better hardware complexity and power optimization with reduced delay. This method avoids the use of a large area in terms of logic elements. *Modelsim* based simulation results of an implementation of truncated multiplier in FIR filter showed the feasibility of this approach. QUARTUS II based hardware synthesis report of truncated multiplier in FIR filter consumes estimated power of 39.54 mW and occupies an area of 210 nm which is less when compared to a direct truncation multiplier.

Field programmable gate arrays were actually invented only for prototyping the digital design which is later to be used in IC's. But in recent days FPGA's are started to use as a product in many fields. So Field programmable gate arrays are ideally suited for the implementation of truncated multiplier in FIR filter which is used for signal processing applications. However, there are several issues that need to be solved. When performing software simulation of truncated multiplier, calculations are carried out with decimal point. But in FPGA only integer arithmetic points are used which is unjustified, and measures to be taken to account for this. Many techniques have been used to efficiently use floating point (IEEE 754 format) values into for digital implementation. Then only we can implement truncated multiplier in VLSI.

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BIOGRAPHY

First author Sandhya.S. received her BE Degree in Electronics and Communication Engineering from Tagore Engineering college,Chennai and she doing M.E in digital signal processing in GKM college of engineering and techonolgy. Her current research interest includes VLSI System design and Digital signal processing. She attended the many national and international conferences.

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