

Design and Implementation of Parallel Connected DC-DC Buck Converters

B.Nirmala^{#1}.S.Archana ^{#2}

^{#1}PG Scholar, ^{#2} Phd scholar, EEE Department, College of Engineering, Guindy,

Anna University, Chennai-25.

Abstract: In this paper, the design and implementation of parallel connected DC-DC buck converters are studied. It was proposed to develop a master-slave controller for parallel DC-DC buck converters which will enable equal sharing of load among the buck converters. The proposed control concept may lead to effective distribution of control implementation of parallel dc-dc converters which also may lead to redundancy. The advantages of this scheme are its simplicity in design, good voltage regulation, flexibility and rapid transient response to reduce the impact of very high frequency dynamics due to parasitic on the closed loop system. The effect of this current sharing scheme is to "Regulate the system output voltage".

Keywords: Parallel connected DC-DC buck converter, master slave control, current sharing

I. INTRODUCTION

converter circuit used for power management and voltage so as to reduce the current ripple, conduction losses, Lower regulator applications. In this project, Parallel dc-dc converters were analyzed, to study their output. Parallel DC-DC Converters are largely used in telecommunication power supplies, since a Parallel DC-DC converter helps in and inductance L_1 are for converter while S_2 and L_2 for providing an uninterrupted service. They operate under closed-loop feedback control to regulate output voltage, equalize the currents in the individual converters. A parallel DC-DC converter provides smooth acceleration control, high efficiency and fast dynamic response. To achieve the above advantages, three current sharing mechanisms are used namely, voltage mode control, current mode control and master-slave control. The control concepts are proposed to provide sharing of load currents between parallel connected converters. To control the switch, Pulse width modulation the second sub-circuit state is when the Switch is turned (PWM) is the most frequently used control method. A sawtooth signal is compared with a control signal to produce a series of pulses that control the states of the power electronic switches. The controlled system provides a more accurate and faster current limit under over load condition

II. PARALLEL CONNECTED BUCK

The parallel connection of switch mode converter is a well known strategy. It involves phase shifting of two or more buck converters connected in parallel and operating at the same switching frequency. Two buck converters are connected in parallel feeding a common resistive load as

shown in fig.1. Converters are connected in parallel to equalize the load currents in the individual converters. The The dc-dc buck converter is the simplest power two converters are working at the same switching frequency switching frequency for each phase to fast transient response.

> As per Fig 1, we use a parallel scheme, where switch S_1 converter2. The switches and diodes conduct in complementary fashion. If switch S_1 conducts, then diode D_1 will not conduct and vice versa.

> The circuit operates as below, the inductor current flows continuously over one switching period. The switch is either on or off according to the switching function q and this results in two circuit states. The first subcircuit state is when the switch is turned on, diode is reverse biased and inductor current flows through the switch, off and current freewheels through the diode.



Fig. 1 Block diagram of parallel connected buck converter



A.Modes of Operations

converters can be classified into two different modes of operation that are (a) Continuous conduction mode (CCM) and (b) Discontinuous conduction mode (DCM). According to the requirement a converter can be designed in any mode of operation. For this study the circuit has been designed to operate on CCM or DCM based on the Load provided to the Circuit.

Continuous conduction mode

Continuous Conduction Mode (CCM) of operation shown in a load resistance R. fig 2(a). The converter operating in CCM delivers larger current and the converter operating in DCM delivers lesser current compare to CCM. In CCM, each switching cycle T_{s} consists of two parts that is D_1T_s and D_2T_s (D_1+D ₂=1).During D₁T_S inductor current increases linearly and then in D_2T_2 Sit ramps down that is decreases linearly.

Discontinuous Conduction Mode

When the inductor current staying at zero and has a interval of time with no charge and discharge then it is said to be functioning in Discontinuous Conduction Mode (DCM) operation and the waveform of inductor current is illustrated in fig 2(b). At lighter load currents, the converter operates in DCM. The regulated output voltage in DCM does not have a linear relationship with the input voltage as in CCM. In DCM, each switching cycle is divided into of three parts that is D_1T_s , D_2T_s and D_3T_s ($D_1+D_2+D_3=1$). During the third mode i.e. in D_3T_s , inductor current stays at zero.



Fig.2 inductor current waveform of (a) CMC, (b) DCM

III. PARALLEL BUCK WITH VMC

All paragraphs must be indented. All paragraphs must be justified, i.e. both left-justified and right-justified.

In Voltage mode control (VMC) the Output voltage of the Based on the continuity of inductor current flow the dc-dc Convertor is again fed back to an error amplifier and compared with a reference voltage fed externally. The difference in Voltage is passed through a Control Unit and fed to a comparator. The Ramp Signal and the voltage difference fed produce the Pulse to control the Switch. Since only the output voltage from the converter is used to produce the pulse this method is called voltage Mode Controller.

The parallel buck converter based on voltage mode During the switching period, when the inductor current control is shown in fig 3; it consists of a capacitor C, flow is continuous of charge and discharge it is called controlled switch Sw (MOSFET) diode D, an inductor L, and





The analog PWM feedback logic controls the switching action. This is achieved by obtaining a control voltage Vcon as function of the output voltage V_0 and a reference signal V_{ref} in the form, Where K_p is the gain of proportional controller .An externally generated saw-tooth voltage defined as V_{ramp} is used to determine the switching instants.

> $V_{ramp(t)} = V_L + (V_U - V_L) * F^*(t/T_S)$ (1)

where Ts is the time period and $V_{\rm U}$ and $V_{\rm L}$ are upper and lower threshold voltages respectively. Here F(x) denotes the fractional part of (x), In voltage mode control, the controlled voltage V_{con} is then compared with the periodic saw-tooth wave Vramp, to generate the switching signal q [1, 0] is described by

If
$$V_{ramp} < V_{con}$$
 $q = 1$
 $V_{ramp} > V_{con}$ $q = 0$

The inductor current increases while the switch Sw is on i.e q=1 and falls while the switch S is off i.e. q=0.

IV. PARALLEL BUCK WITH CMC



There are two feedback loops in the Current-mode converter. controlled dc-dc converter, a current feedback loop and a voltage feedback loop. The inductor current is used as a feedback states.

Both the inductor currents and the output voltage controlled by this scheme. The control strategy is designed such that the inductor current I_{L1} , I_{L2} currents follows the sinusoidal line voltage. An analog multiplier generates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier. This modulation makes the current programming signal follow the shape of input voltage.

The signal acts as a reference current. It is compared with the switch current in a PWM comparator. The resulting pulses drive a MOSFET



Fig. 4 Block diagram of CMC

The control input signal is proportional to reference current i_{ref} . The reference current i_{ref} is a function of output of the controller to regulate the output voltage. The control voltage can be defined as,

(2)

 $V_{con} = V_{offset} - K_v(V_0 - V_{ref}) - K_i(i_1 - m i_2)$

V. PARALLEL BUCK WITH MSC

For the purpose of load current sharing Master slave control method is employed. To ensure the voltage regulation one converter is chosen as the master converter and the other as slave converter which is keeping the output current to be same as the master's by regulating their voltage reference through current sharing control loops. The output voltage loop acts as the reference for the current loop all the slave modules have the same controller structure and receive the current reference from the master module.

This method achieves current sharing by modifying the sensed current signal, hence no additional current sensing circuit is needed. The stability analysis of the entire parallel system is similar to the stability of an individual dc-dc buck



Fig. 5 Block diagram of MSC

In the master-slave control, the two converters, converter 1 and 2 are controlled via a simple pulse-width modulation (PWM) scheme, in which a control voltage V_{con} is compared with a saw tooth signal to generate a pulse-width modulated signal that drives the switch. The relationship between control voltage and PWM output is shown in fig 3. The saw tooth signal of the PWM generator is given by

 $V_{ramp} = V_L + (V_U - V_L)t \mod /T$ (3)

For Converter 1, the control voltage is derived from a voltage feedback loop, i.e.

$$V_{con1} = V_{offset} - K_{v1}(V_0 - V_{ref})$$

Where V_{offset} is a dc offset voltage that gives the steadystate duty cycle, V_{ref} is the reference voltage, and K_{v1} is the voltage feedback gain for converter 1.

(4)

For converter 2, an additional current error signal, which is proportional to the weighted difference of the output currents of the two converters, determines the control voltage.

The control voltage for converter 2 is $V_{con2}=V_{offset}-K_{v2}(V_0-V_{ref})-K_i(i_2-mi_1)$

 $V_{con2}=V_{offset}-K_{v2}(V_0-V_{ref})-K_i(i_2-mi_1)$ (5) where K_{v2} is the voltage feedback gain of converter 2, K_i is the current feedback gain, and m is a current weighting factor. When m=1, we expect equal current sharing



VI. RESULTS

The simulation results of parallel buck converter and the component values used in simulation circuit are shown in table 1

Parameters		Values	
Source voltage	Vs		12V
Output voltage	Vo		5.5V
Inductor	L		14.58µH
Capacitor	С		200µF
Resistor	R		50Ω
Ripple voltage	ΔV		2% of Vo
Ripple current	ΔI		8% of Io
Switching frequency F		25KHz	
Power rating	Р	Į,	560Mw

TABLE 1: Parameters of the Parallel Buck Converters

A . SIMULATION RESULTS Of voltage Control Mode Waveform of gate pulses

The switches will conduct when gate pulses given to both the converters. The gate pulses for switches are shown in fig 6.



Fig.8 waveform of output voltage

For the buck converters the output voltage is less than the input voltage. The output voltage obtained is 5.2volts dc supply and the output voltage waveform is shown in fig 8.





Fig.9.wave forms of gate pulses

Wave forms of inductor current





Fig.10a. waveform of inductor current (IL1)



Fig.10a. waveform of inductor current (I_{L2}) The inductor currents is equal for both converters as shown in fig 10a &10b the inductor current is 0.08Amps.

Waveforms of output voltage





Waveforms of inductor currents



COMPARISON OF THREE CONTROL MODES

Current mode control	Voltage mode control	Master-slave control
The circuit analysis is difficult	it has single feedback loop making	it has two feedback loops so that
because it <u>has_two</u> feedback loops.	design and circuit analysis easier	the circuit design and analysis is difficult compare to <u>cmc</u>
It provides a more accurate and	It is a very slow system, as the	It provides a good voltage regulation
faster current limit under overload conditions	respond is much longer of switching cycles.	and more_accuracy
the inductor current does not change	low-impedance power output	Reduce the ripple content in the
quickly when the input voltage	providing better cross-regulation for	inductor current and fast transient
changes, so the supply has good line transient performance.	multiple-output supplies.	response.
a current mode-controlled converter	It is less in reliability, stability, or	It has more reliability, stability and
is more reliable .	performance when several	redundancy
	converters in parallel supply with	
	one load	
It is very unstable when duty ratio	It can work over a wide range of	If the master converter is failed
exceeds 0.5 in the peak current	duty cycles	then the entire system will shutdown
mode- control.		

VII. CONCLUSION

Even though VMC is having simple design it can work over a wide range of duty cycles but it has less stability and reliability. Due to stability and reliability the CMC provides more accurate and faster current limit under overload [12]. Siri, K., Lee, C. Q. and Wu, T.-F. "Current distribution control for conditions but it becomes unstable when the duty ratio exceeds 0.5. Due to more stability and reliability MSC provides good voltage regulation and more accuracy due to which it reduces the ripple content in the inductor current and also it has faster transient response. The parallel connected buck converter using a master-slave approach control strategy implemented. When the buck converters are connected in parallel, the current is shared based on the current sharing ratio and the output voltage is regulated.

REFERENCES

- Olivier Trescases, Zdravko Lukic, Wai Tung Ng and Alecksandar [1]. Prodic, "A Low-Power Mixed-Signal Current-Mode DC-DC Converter Using a One-Bit delta-sigma DAC," IEEE Annual Applied Power Electronics Conference and Exposition, pp. 700-704, Mar. 2006.
- [2]. P. Li and B. Lehman, "A design method for paralleling current mode controlled DC-DC converters," IEEE Transactions on Power Electronics, Volume: 19, Issue: 3, May 2004, Pages: 748 – 756.
- S. K. Mazumder, M. Tahir, and S. L. Kamisetty, "Wireless PWM [3]. control of a parallel dc-dc buck converter," IEEE Trans. Power Electron., vol. 20, no. 6, pp. 1280-1286, Nov. 2005
- G.-P. Liu, Y. Xia, J. Chen, D. Rees, and W. Hu, "Networked [4]. predictive control of systems with random network delays in both forward and feedback channels," IEEE Trans. Ind. Electron., vol. 54, no. 3, pp. 1282-1297, Jun. 2007.
- [5]. Banerjee S. Nonlinear modeling and bifurcation in boost converter. IEEE Trans Power Electron 1998;13(2):253-60
- [6]. Panov, Y., Rajagopalan, J. and Lee, F. C. "Analysis and design of Nparalleled dc-dc converters with master-slave current sharing control,"in Proc. IEEE Appl. Power Electron. Conf., 1996, pp. 678-684.

- [7]. Batarseh, K. Siri, and Lee, H. "Investigation of the output droopcharacteristics of parallel-connnected dc-dc converters," in Proc. IEEEPower Electron. Spec. Conf., vol. 1, 1994, pp. 1342-1351.
- [8]. Garabandic, D. S. and Petrovic, T. B. "Modeling parallel operating PWMdc-dc power supplies," IEEE Trans. Ind. Electron., vol. 42, pp. 545-550,Oct. 1995
- [9]. Kohama, T., Ninomiya, T., Shoyama, M. and Ihara, F. "Dynamic analysisof parallel-module converter system with current balance controllers,"in Proc. IEEE Int. Telecomm. Energy Conf., 1994, pp. 190-195.
- [10]. Rajagopalan, J., Xing, K., Guo, Y. and Lee, F. C. "Modeling and dynamicanalysis of paralleled dc-dc converters with master/slave current sharingcontrol," in Proc. IEEE Appl. Power Electron. Conf.,1996, pp. 678-684
- [11]. Thottuvelil, V. J. and Verghese, G. C. "Analysis and control design of paralleled dc/dc converters with current sharing," IEEE Trans. PowerElectron., vol. 13, pp. 635-644, July 1998
- parallel connected converters: I," IEEE Trans. Aerosp. Electron. Syst., vol. 28,pp. 829-840, 1992
- [13]. Thottuvelil, V. J. and Verghese, G. C. "Stability analysis of paralleled dc-dc converters with active current sharing," in Proc. IEEE Power Electron.Spec. Conf., 1996, pp. 1080–1086.