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Implementation of Error Correction Technique Based On Decimal Matrix Code

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Abstract: Error detection and correction (EDAC) has become more important with the continued device scaling. In many computer systems, the contents of memory are protected by an errordetection and correction (EDAC) code. In order to maintain a good level of reliability, it is necessary to protect memory cells using protection codes various error detection and correction methods are being used. The report discusses in detail about multiple error correction, exactly to detect and correct 64 errors. The proposed technique utilizesdecimal matrix algorithms to detect errors, so that more errors were detected and corrected, but the main problem is that they would require higher delay overhead. Latterly, matrix codes (MCs) based on hamming codes have been proposed for storage protection.Moreover, the encoder-reuse technique (ERT) is advised to minimize the area overhead of extra circuits without interrupting the whole encoding and decoding operations.ERT uses DMC encoder itself to be part of the decipherer.The proposed paper was gone through and utilized effectively in an actual space experiment.

Keywords: Error correction codes (ECCs), Encoder Reuse Technique (ERT), and Matrix Code (MC)

I. INTRODUCTION

The primary idea for developing error detection and correction is to add some redundancy (i.e.,Some extra data) to a message, which recipients can use to check consistency of the delivered message, and to recover data determined to be spoiled.Error-correcting codes are frequently employed in lower-layer communication, as considerably as for reliable computer memory media such as CDs, DVDs, hard disks, and RAM.

AS CMOS technology scales down to the nanoscale and memories are combined with an increasing number of electronic systems, the soft error rate in storage cells is quickly increasing, especially when memories operate in space environments due to the ionizing effects of atmospheric neutron, alpha-particle, and cosmic rays.

Hamming Codes and Matrix Codes are largely applied to correct Single Error Upsets (SEU's) in storage due to their ability to correct single errors with reduced area and performance overhead.Though excellent for correction of single faults in a data word, they cannot correct double bit errors caused by single event upset.An elongation of the basic Single Error Correction – Double Error Detection Hamming Code has been aimed to organize a limited class of codes known as Hsiao Codes to improve the speed, price and reliability of the decoding logic.

One more year of the SEC-DED codes known as Single-error-correcting, Double-error-detecting Single-byte-error-detecting SEC-DED-SBD codes were proposed to discover any number of errors affecting a single byte. These codes are more suitable than the conventional SEC-DED codes for protecting the byte-organized memories.

Built-in current sensors (BICS) are proposed to assist with the single - error correction and double-error detection codes to provide protection against MCUs. However, this technique can only correct two errors in a word.

More recently, in 2-D matrix codes (MCs) are proposed to efficiently correct MCUs per word with a low decoding delay, in which one word is divided into multiple rows and multiple columns in logical. The bits per row are protected by Hamming code, while parity code is added in each column. For the MC based on Hamming, when two errors are detected by Hamming, the vertical syndrome bits are activated so that these two errors can be corrected. As a result, MC is capable of correcting only two errors in all cases. In an approach that combines decimal algorithm with Hamming code has been conceived to be applied at software level. It uses the addition of integer values to detect and correct soft errors. The results obtained have shown that this approach has a lower delay overhead over other codes.

The proposed DMC utilizes a decimal algorithm (decimal integer addition and decimal integer subtraction) to detect errors. The advantage of using decimal algorithm is that the error detection capability is maximized so that the reliability of memory is enhanced. Besides, the encoder-reuse technique (ERT) is proposed to minimize the area overhead of extra

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circuits (encoder and decoder) without disturbing the whole encoding and decoding processes, because ERT uses DMC

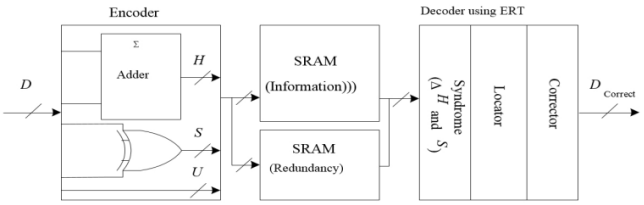


Fig 1. Schematic of fault-tolerant, memory protected with DMC.

This paper is divided into the following sections. The proposed DMC is introduced and its encoder and decoder circuits are presented in Section II. The simulation outputs are in section III. Finally, some conclusions of this paper are discussed and shared in Section IV.

II. PROPOSED DMC

In this section, DMC is proposed to assure reliability in the presence of MCUs with reduced performance overheads, and a 128-bit word is encoded and decoded as an example based on the proposed techniques.

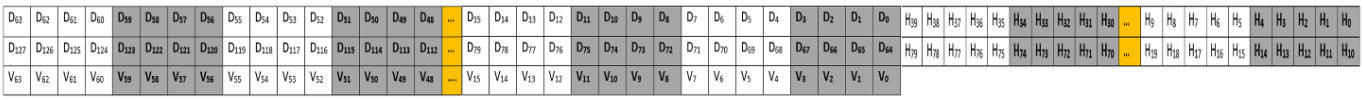
A. *Proposed Schematic of Fault-Tolerant Memory*

The proposed schematic of fault-tolerant, memory is depicted in Fig. First, during the encoding (write) process, information bits D is fed to the DMC encoder, and then the horizontal redundant bits H and vertical redundant bits V are obtained from the DMC encoder. When the encoding process is completed, the obtained DMC code word is stored in the memory. If MCUs occur in the memory, these errors can be corrected in the decoding process. Due to the advantage of decimal algorithm, the proposed DMC has the higher fault-tolerant capability with lower performance overheads. In the fault-tolerant, memory, the ERT technique is proposed to reduce the area overhead of extra circuits and will be introduced in the following sections.

B. *Proposed DMC Encoder*

In the proposed DMC, first, the divide-symbol and arrange-matrix ideas are performed, i.e., The N-bit word is divided into k symbols of m bits (N = k × m), and these symbols are arranged in a k1 × k2 2-D matrix (k = k1 × k2, where the values of k1 and k2 represent the numbers of rows and columns in the logical matrix respectively). Second, the horizontal redundant bits H are produced by performing decimal integer addition of selected symbols per row. Here, each symbol is regarded as a decimal integer. Third, the vertical redundant bits V are obtained by the binary operation among the bits per column. It should be noted that both divide-symbol and arrange-matrix is implemented in logical instead of in physical.

To explain the proposed DMC scheme, we take a 128-bit word as an example, as shown in Fig. 2. The cells from D_0 to D_{128} are information bits. This 128-bit word has been divided into 32 symbols of 4-bit. $k_1 = 2$ and $k_2 = 4$ have been chosen simultaneously. H_0–$H_{80}$is horizontal check bits; V_0 through V_{31} are vertical check bits. However, it should be mentioned that the maximum correction capability (i.e., the maximum size of MCUs can be corrected) and the number of redundant



bits is different when the different values of k and m are chosen. Therefore, k and m should be carefully adjusted to maximize the correction capability and minimize the number of redundant bits. For example, in this case, when k = 2×2 and m = 8, only 1-bit error can be corrected and the number of redundant bits is 80. When k = 4 × 4 and m = 2, 3-bit errors can be corrected and the number of redundant bits is reduced to 32. However, when k = 2 × 4 and m = 4, the maximum correction capability is up to 5 bits and the number of redundant bits 144. In this paper, in order to enhance the reliability of memory, the error correction capability is first considered, so k = 2 × 8 and m = 4 are utilized to construct DMC.

The horizontal redundant bits *H* can be obtained by a decimal Integer addition as follows:

$$H_4H_3H_2H_1H_0 = D_3D_2D_1D_0 + D_{11}D_{10}D_9D_8 \quad (1)$$

$$H_9H_8H_7H_6H_5 = D_7D_6D_5D_4 + D_{15}D_{14}D_{13}D_{12} \quad (2)$$

And similarly for the horizontal redundant bits $H_{14}H_{13}H_{12}H_{11}H_{10}$ and $H_{19}H_{18}H_{17}H_{16}H_{15}$, where "+"represents decimal integer addition.

For the vertical redundant bits *V*, we have

$$V_0 = D_0 \text{ xor } D_{64} \quad (3)$$

$$V_1 = D_1 \text{ xor } D_{65} \quad (4)$$

And similarly for the rest vertical redundant bits.

The encoding can be performed by decimal and binary addition operations from (1) to (4). The encoder that computes the redundant bits using multibit adders and XOR gates is shown in Fig. In this figure, $H_{79} - H_0$ are horizontal redundant bits, $V_{63} - V_0$ are vertical redundant bits, and the

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remaining bits $U_{127} - U_0$ are the information bits which are directly copied from D_{127} to D_0. The enable signal En will be explained in the next section.

C.*Proposed DMC Decoder*

To obtain a word being corrected, the decoding process is required. For example, first, the received redundant bits $H_4H_3H_2H_1H_0$' and V_0'-V_3' are generated by the received information bits D'. Second, the horizontal syndrome bits $\Delta H_4H_3H_2H_1H_0$ and the vertical syndrome bits $S_3 - S_0$ can be calculated as follows:

$$\Delta H_4H_3H_2H_1H_0 = H_4H_3H_2H_1H_0' - H_4H_3H_2H_1H_0 \quad (5)$$

$$S_0=V_0'\text{xor}V_0 \quad (6)$$

And similarly for the rest vertical syndrome bits, where "–" represents decimal integer subtraction. When $\Delta H_4H_3H_2H_1H_0$ and $S_3 - S_0$ are equal to zero, the stored codeword has original information bits in symbol 0 where no errors occur. When $\Delta H_4H_3H_2H_1H_0$ and $S_3 - S_0$ are nonzero, the induced errors (the number of errors is 4 in this case) are detected and located in symbol 0, and then these errors can be corrected by

$$D_0\text{correct} = D_0 \text{ xor } S_0 \quad (7)$$

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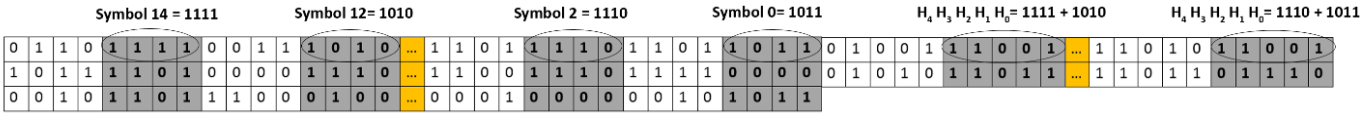

Fig.2 128-bit Logical Operation

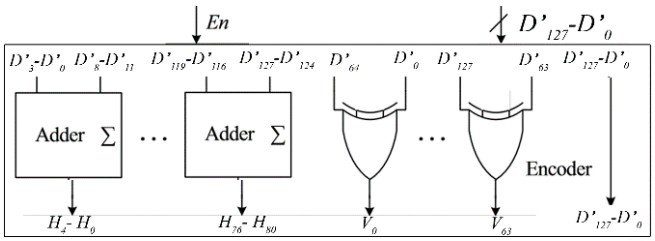

Fig.3. 128-bit DMC Encoder Structure

Extra circuit	*En*signal		Function
	Read signal	Write signal	
Encoder	0	1	Encoding
	1	0	Compute syndrome bits

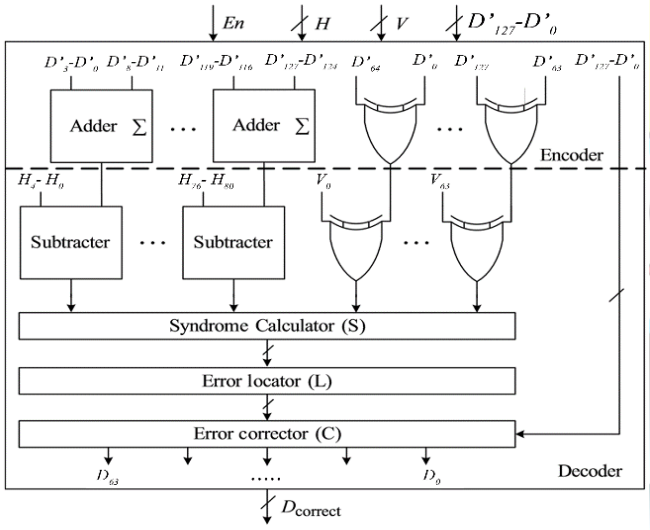

Fig.4. 128-bit DMC Decoder Structure

The proposed DMC decoder is depicted in Fig, which is made up of the following sub modules, and each executes a specific task in the decoding process: syndrome calculator, error locator, and error corrector.

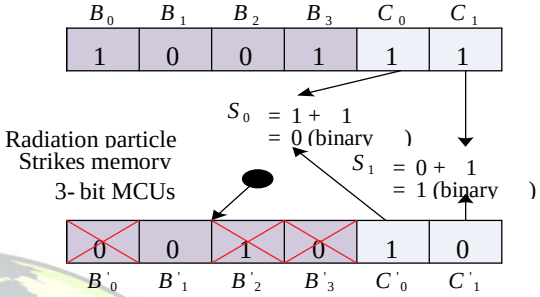

Fig 5. Limits of binary error detection in simple binary operations

In the proposed scheme, the circuit area of DMC is minimized by reusing its encoder. This is called the ERT. The ERT can reduce the area overhead of DMC without disturbing the whole encoding anddecoding processes. From Fig, it can be observed that the DMC encoder is also reused for obtaining the syndrome bits in DMC decoder. Therefore, the whole circuit area of DMC can be minimized as a result of using the existing circuits of the encoder. Besides, this figure also shows the proposed decoder with an enable signal En for deciding whether the encoder needs to be a part of the decoder. In other words, the En signal is used for distinguishing the encoder from the decoder, and it is under the control of the write and read signals in memory. Therefore, in the encoding (write) process,

The DMC encoder is only an encoder to execute the encoding operations. However, in the decoding (read) process, this encoder is employed for computing the syndrome bits in the decoder. These clearly show how the area overhead of extra circuits can be substantially reduced.

The decimal matrix code is proposed to provide enhanced memory reliability. This approach uses decimal algorithm, which increases the error detection capability. In the proposed work encoder is reused as a part of decoding circuit, thus reduces the area overhead compared to other techniques.

III. RESULTS

A. 128-bit Simulation Output

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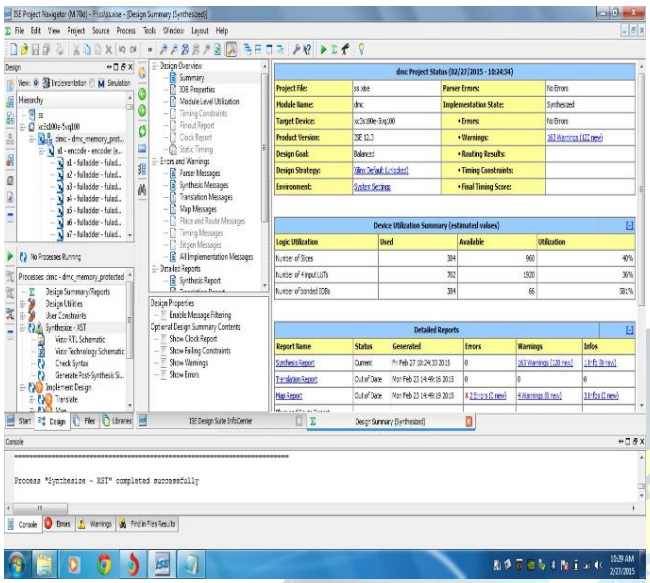
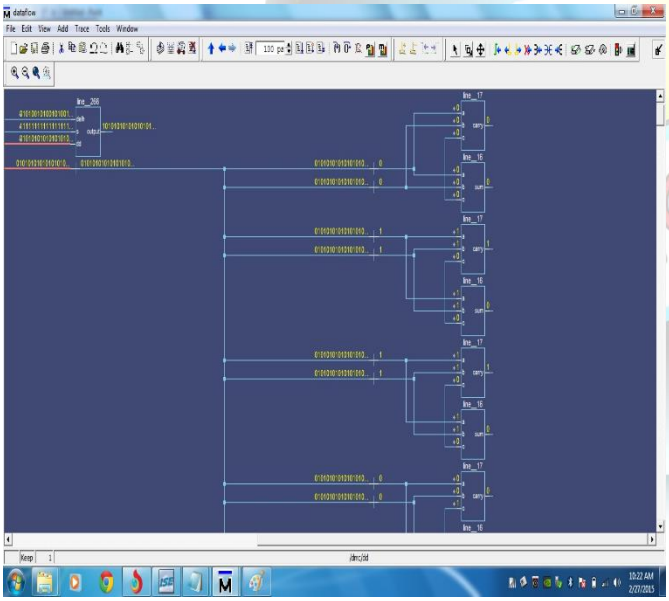
B. Area, Delay and Power Calculation



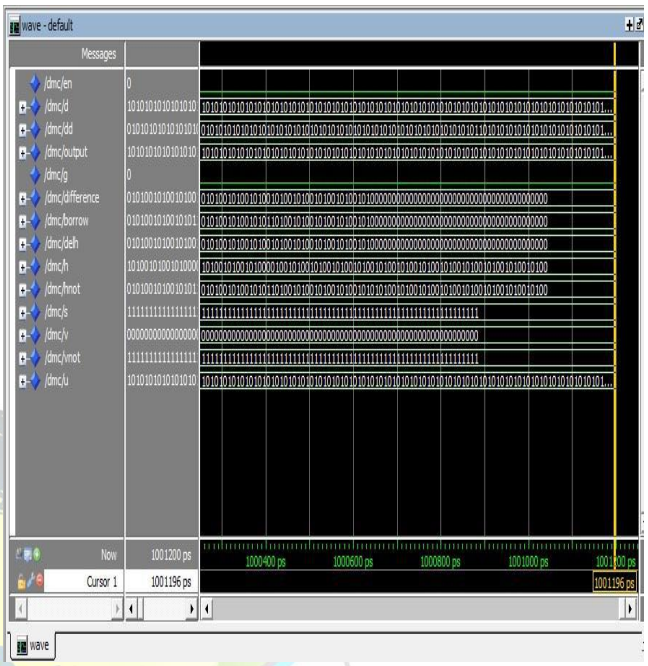
C. Data Flow Modelling



IV. CONCLUTION AND FUTURE WORK

Error correction codes are used to improve the memory protection and make the memory fault free. The various ECC are used to detect the occurrence of error and also correct the detected ones.

However the error detection capability and the overheads vary based on the codes used. The proposed



protection code DMC utilized decimal algorithm to detect errors, so that more errors were detected and corrected.

The only drawback of the proposed DMC is that more redundant bits are required to maintain higher reliability of memory.

FUTURE WORK

The future work will be conducted for the reduction of the redundant bits and the maintenance of the reliability of the proposed technique.

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BIOGRAPHY

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K. Sathyamoorthy, pursuing BE-ECE in SNS College of Engineering, Coimbatore. He Received the Diploma in Electronics and communication engineeringfrom the Department of Technical Education, Chennai. He Interested in Photoshop works and designing and published a paper titled "FPGA Implementation of Error Correction Technique Based On decimal Matrix Code" in International and National Conference.