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FPGA Simulation of Byte to Bit, Preamble Trailer and HEC Gen modules of Bluetooth Transmitter

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Abstract: This paper presents FPGA simulation of Byte to Bit, Preamble Trailer, HEC Gen, modules of Bluetooth Transmitter. Bluetooth is a universal short range radio link and is designed to provide low-cost and robust networking. Our Bluetooth transmitter is designed in Verilog -hardware description language (HDL) and is implemented in to FPGA. So, performed top level functional verification and debugging as well as detailed subsystem simulations of all the modules. The prototyping board equipped with Xilinx Spartan-3E FPGA device is used for hardware evaluation of system design. For simulation part, Xilinx ISE Design Suite 14.2 is used as the simulation tool. The proposed system has been validated for different sub-modules with simulation results.

Keywords: FPGA, Bluetooth, State transition diagram, Spartan3E, Transmitter

I. INTRODUCTION

Bluetooth was created by Ericson in 1994 as a wireless alternative for rs232 data cables. Bluetooth is the wireless communication technology managed by special interest group (sig) in 1998, to fulfil the demands of wireless personal area networking (WPAN). it offers wireless, short distance, point to point and point to multipoint data transfer operating at 2.4 GHz unlicensed industrial, scientific and medical (ism) band [1]. Bluetooth uses repeat skipping spread range development for all transmission. as it is well-known; this innovation limits impedance and transmission blunders and gives transmission security [2].

Bluetooth is a technology for data communication that uses short-range radio links to replace cables between computers and their connected units. Bluetooth utilizes 2.4 GHz industrial, scientific and medical (ism) radio band. Here, simulation of Bluetooth module is considered utilizing an embedded system FPGA. FPGA is a semiconductor device that is based around the cross section of a configurable logic blocks (CLBS) related by programmable interconnects. FPGAs can be reconfigured to the desired application. This property of FPGAs makes them different from application specific integrated circuits (ASICS), which are made for particular applications. Although there are one-time programmable (OTP) FPGAs, the predominant sorts are SRAM based which can be reconfigured even at run-time [2].

Bluetooth technology stands on the top as it is able to provide a communication between devices and users in a simple and efficient manner. There are many types of Bluetooth devices that are being used in our daily life. In these various types of Bluetooth devices, there are several types of Bluetooth modules that are designed to control various appliances. these modules are based on several specifications based on which they perform the operations that are related to it. One of its specifications is that, they work within a range of 45metres and will operate at 2.4 ghz frequency [3].

II. DESCRIPTION OF THE STATE TRANSITION DIAGRAM

The state transition diagram is shown in Fig1.The SMC (State Machine Controller) controls the overall operation of the transmitter. The transmitter being simulated here by using seven states-Idle, Preamble, Access Header, HEC, Payload and CRC. Initially, the transmitter is in idle state. It remains in the same state until the Rst=0 and Transmit Enable T×Ena=0.When Rst=1 and T×Ena=1, then it switches to preamble state. In preamble state, it checks for the condition of flag. If flag=0 and Preamble Over=1, then it switches to Access state and if flag=1 and Preamble Over=1, then it switches to Header state. But it remains in the Preamble state, if Preamble Over=0.In Access state it checks

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the packet type, If the packet type is 1 i.e., 0001, Access Over and T×Ena=1, then it switches to the Preamble state. If Access Over=0, then it remains in the same state. In Header state, if Header Over=0, then it remains in the same state and if Header Over=1, then it switches to HEC state and flag is assigned to 0.

In HEC state, it again checks the packet type. If it is 2 i.e. 0100, HEC Over and T×Ena=1, then it switches to the Preamble state. If HEC Over and T×Ena=0, then it switches to the Idle state. If the packet type is 4 i.e.0100 and HEC Over=1, then it switches to Payload state. In Payload state it remains in the same state if Payload Over=0.If Payload=1, then it switches to CRC state. In CRC state, it remains in the same state if CRC Over=0.If CRC Over=1 and T×Ena=1, then it switches to the Preamble state. If T×Ena=0, then it switches to the Idle state.

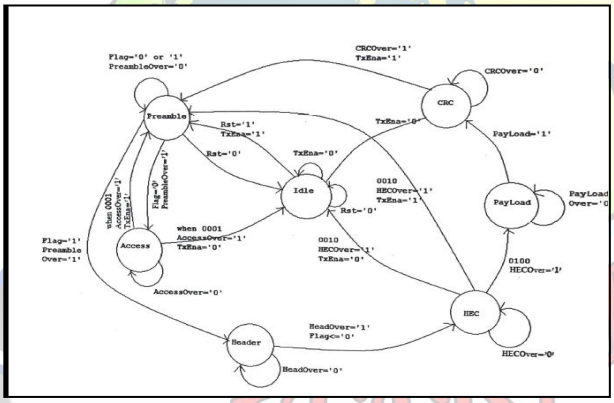

Fig. 1 State Diagram for the Bluetooth Transmitter

III. Implemented System Module

The simulation module shown in Fig 2 consist of various sub modules and it can be divided in to 4 different groups like in group 1- Access FIFO, Head Info, PayLd FIFO, Access Timer, Head Timer, PayLd Timer, in group 2- DataMux and state machine controller, in group 3- ByteToBit, Preamble Trailer, HEC Gen, CRC Gen and in group 4 only one module i.e. Serial Dat Mux. In our previous work, we have implemented FPGA Simulation of Access FIFO, PayLd FIFO and Head Info modules of Bluetooth Transmitter [4] and FPGA Simulation of Access Timer, Head Timer, Pay load timer and Data mux modules of Bluetooth Transmitter [5]. In this paper, we extend our work to simulation of some selected modules in group-3 i.e. Byte to Bit, Preamble Trailer, HEC Gen and their results are presented. So, remaining modules of group 1, 2, and 4 will not be discussed further in this paper.

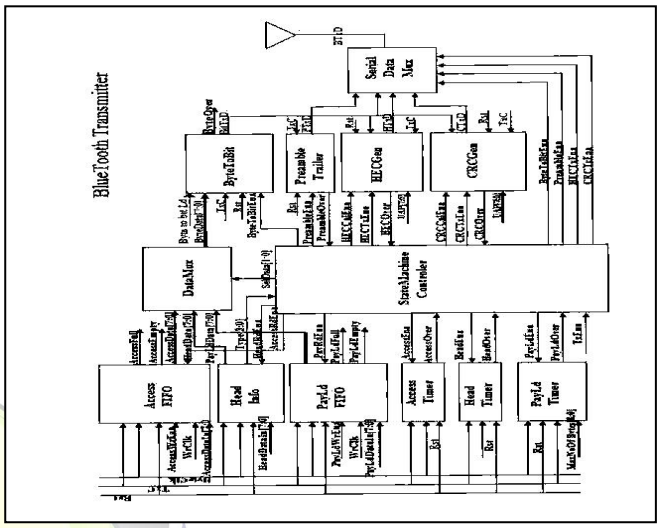

Fig. 2 Simulated Bluetooth transmitter module

IV. FPGA Simulation and Simulation Results

Spartan3E FPGA is used to verify the design. The Spartan-3E is logic optimized FPGA for applications where logic densities matter more than I/O count. It requires few interfaces and is suitable for embedded control applications. Sparatan-3E is the 3rd generation of FPGAs which offers a choice of five platforms, each delivering a unique cost-optimized balance of programmable logic. The Spartan-3E family is a superior alternative to mask programmed ASICs [6]. The prototyping board equipped with Xilinx xv200e target device, along with cs144 target package at a target speed of -6 was used in a FPGA device for hardware evaluation of system design. For simulation part, Xilinx ISE Design Suite 14.2 is used as the simulation tool.

A. Byte to Bit

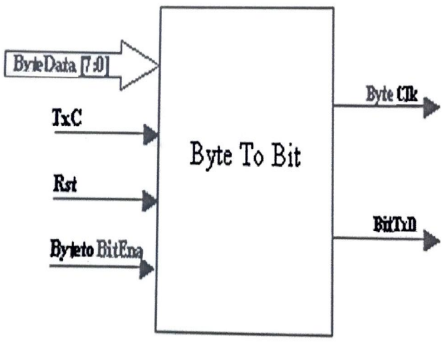

Fig. 3 Byte to Bit module

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A.1 Signal Description

TABLE I

S.No.	Port name	Mode	Description
1.	TxC	Input	Synchronizing clock
2.	Rst	Input	It initializes all internal registers
3.	ByteData[7:0]	Input	Bytes to be converted to bits
4.	Byte to BitEna	Input	Enables the Byte to bit conversion
5.	ByteClk	Output	Asserted high when conversion is completed
6.	BitT×D	Output	Byte converted to bits
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5.	ByteClk	Output	Asserted high when conversion is completed
6.	BitT×D	Output	Byte converted to bits

Description

This will convert the Byte form of the data in to Bit form of data. Byte to Bit module is shown in Fig.3 and simulated waveforms are shown in Fig.4.

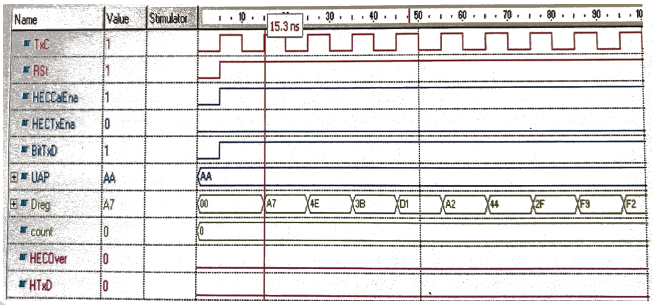

Fig.4 Simulation waveforms of HEC Gen module

B. Preamble Trailer

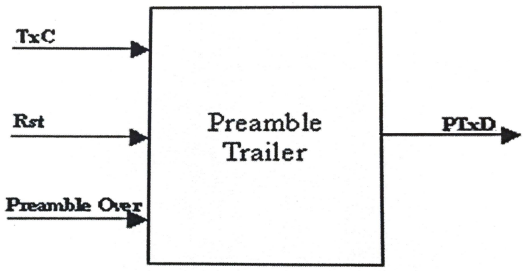

Fig 5 Preamble Trailer

B.1 SIGNAL DESCRIPTION

TABLE II

S. No	Port name	Mode	Description
1.	TxC	Input	Synchronizing clock
2.	Rst	Input	It initializes all internal registers
3.	PreambleOver	Input	Indicates the end of Preamble transmitted sequence
4.	PT×D	Output	Indicates the preamble is transmitted

Description:

The preamble is a fixed zero. One pattern of the 4 symbols used to for DC compensation. The sequence is either 1010 or 0101. Preamble Trailer module is shown in Fig.5 and simulated waveforms are shown in Fig.6.

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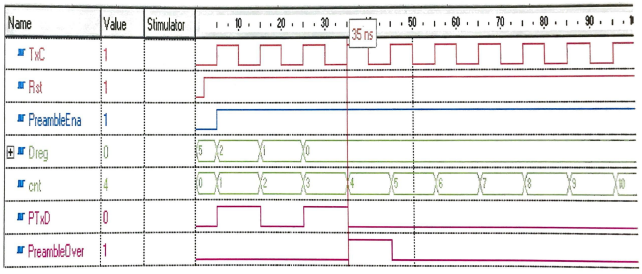

Fig. 6 Simulation waveforms of Preamble Trailer

C. HEC Gen

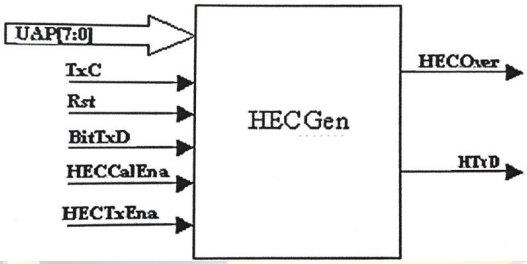

Fig. 7 HEC Gen module

C.1 SIGNAL DESCRIPTION

TABLE III

S .No.	Port name	Mode	Description
1.	TxC	Input	Synchronizing clock
2.	Rst	Input	It initializes all internal registers
3.	HECCalEna	Input	Signal which enables the HEC generator to calculate the HEC code
4.	HECT×Ena	Input	The signal when enabled compares the 8-bit received code with the generated code
5.	BitT×D	Input	Input bits for which the HEC code is generated
6.	UAP	Input[7:0]	It is upper address part provided by the device
7.	HT×D	Output	It is enabled when the header bits are correctly transmitted
8.	HECOver	Output	Indicates that the HEC check is complete

Description:

Every header has a Header Error Check to check the integrity of the packet. HEC Gen module is shown in Fig.7 and simulated waveforms are shown in Fig.8.

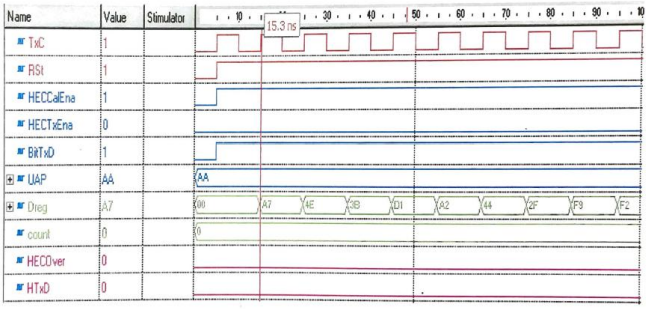

Fig.8 Simulation waveforms of HEC Gen module

IV. CONCLUSION

We have presented modelling and simulation of Bluetooth transmitter using VHDL-FPGA. Simulation of some selected Bluetooth transmitter modules is presented. Different modules of Bluetooth transmitter were simulated and their results are presented in the form of waveforms. The status of different signals used in each module was presented in the form of a table. Some of the critical parameters of simulation are mentioned under FPGA resource usage. State transition diagram presents the flow of control in the Bluetooth transmitter.

V. FGPA RESOURCE USAGE

Target Device: xv200e
Target package: cs144
Target speed: -6
Logic Distribution:
IOB Flip Flops: 8
Number of GCLKs--3 out of 4—75%
Number of GCLKIOBs--3 out of 4—75%
Total equivalent gate count for design: 10,422
Additional JTAG gate count for IOBs: 1,776
Peak memory usage: 69 MB

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Delay summary report:
The score for this design is: 294
The number of signals not completely
Routed for this design is: 0
The average connection delay for this design is: 1.784

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Dr. Arvind Mallikarjun Bhavikatti has a teaching experience of around 37 yrs. He is having 78 publications in various journals and conferences with 107 Citations to his credit. So far, he has produced 4 PhDs under VTU, Belagavi and one research scholar is actively pursuing PhD. He has worked as External examiner for PhD for other universities also. He has worked as member of BOS, BOE of ECE board for Gulbarga University, Gulbarga and VTU, Belgavi. Attended many workshops and conferences in various institutions. He has also worked as Chair/Co-chair of many conferences at his institute and other institutions. He has delivered talks at various workshops/FDPs. He is a fellow of IETE and life member of ISTE. At present he is working as a Professor in AI&ML department at SIT, Kalaburagi, Karnataka.

Smt. Mahadevi. Biradar has a teaching experience of around 37 years. She is having 40 publications in various journals and conferences. She is currently working as Associate Professor and HOD of Electrical and Electronics Engineering department at PDA College of Engineering, Kalaburagi, Karnataka. Her research area is Power electronics, Multilevel inverters, etc