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Comparative Harmonics Analysis of Three Phase Three Level NPC and A Novel T-type NPC Inverter

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Abstract: Multi-level Inverters (MLI) are commonly used in various industrial applications due to low total harmonic distortion in the output voltage. Among multilevel inverters, the three-level inverters are widely used due to its reliability and simplicity. Three level T-type NPC inverter can be used as an efficient inverter for low/medium voltage application for medium switching frequency range. We describe several, recently reported, new topologies and compare them with each other, in order to find out the optimal multilevel grid-connected inverter topology. Third harmonic reduction to three level three phase T-type NPC inverter and their performances are compared. The pulse generator methods are selected as the comparison and the THD of the proposed system is analyzed by simulating in MATLAB/SIMULINK platform under different levels. With the high potential in high power for industry, multilevel inverter will become most popular for so many applications.
Keywords: Multi-Level Inverters, Neutral Point Clamped Inverter, Total Harmonics Distortion.

I. INTRODUCTION

Multilevel inverters include an array of power semiconductors and dc voltage sources, the output of which generate voltage with stepped waveform [1] in comparison with a two-level voltage-source inverter (VSI). The multilevel voltage source inverter enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference [2].By increasing the number of levels in multilevel inverter output voltage have more steps in generating a staircase waveform, which has a reduced harmonic distortion. However a larger number of levels increase the number of devices that must be controlled and control complexity [3]. As a result, the most attractive applications of this technology are in medium to high voltage ranges. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources such as photovoltaic, wind and fuel cells which can be easily interfaced to a multilevel inverter system for a high power application. The advantages of multilevel inverters are their smaller output voltage step, which results in high voltage capability, lower harmonic components, lower switching losses, better electromagnetic compatibility and high power quality. Also it can operate at both fundamental switching frequency and high switching frequency PWM. The field applications include use in laminators, pumps, conveyors, compressors fans, blowers and mills. Subsequently, several multilevel inverter topologies have been developed. Three different topologies have been proposed for multilevel inverters namely Neutral point clamped (NPC) multilevel inverter, flying capacitor (FC) multilevel inverter and cascaded H-bridge (CHB) multilevel inverter[4],[5]. The NPC multilevel inverter also called diode clamped can be consider the first generation of multilevel inverter introduced by Nabae et al.[6], which was a three level inverter. The three-level case of the NPC multilevel inverter has been widely applied in different industries. Unlike the NPC type, the FC multilevel inverter offers some redundant switching states that can be used to regulate capacitors voltage. However, the control scheme becomes complicated. Moreover, the number of capacitors increases by increasing the number of voltage levels.

II. 3-LEVEL CONVENTIONAL NPC INVERTER

Neutral Point Clamped (NPC) or Diode-Clamped inverter is a well-known topology which is widely used in industrial applications [7]. Fig .1 shows the structure of a 3-level three-phase NPC. It needs one DC source as input as shown in Fig.1. Clamping diodes of this topology results in an additional zero voltage at the output. There are 4 switches in each leg of a 3-level NPC so, a total number of 24=16 switching states may be possible. By ignoring invalid switching states (the ones leading to a open-circuit or short-circuit in the output) and considering the fact that in phase R (R=a,b or c) the lower switches ($S3a$,$S4a$)are always in an contradictory state with respect to the upper switches ($S1a$,$S2a$) there will be only 3 effective switching states. Each one of these three states which are denoted as 0, 1 and 2 and their respective voltages in the output

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are given in Table I. State ‘’1”gives a zero voltage by using clamping diodes to connect the neutral point (O) to the output. In the similar manner state “2” (“0””) gives +vdc/2(-vdc/2) by applying voltage of capacitor C1 (reverse voltage of C2) to the output. As an illustration, Fig. 1 shows how switching state “2” generates a positive (+vdc/2) voltage at the phase output (vao). As stated earlier, the only change between 3-level NPC and the conventional 2-level full-bridge inverter is clamping diodes. For each leg of an-level NPC, there would be (n−1)(n−2)clamping diodes and there would be (n−1) DC-link capacitors. Since these capacitors divide the input voltage (vdc) among themselves, nominal voltage rating of each of them would be Vdc/ (n-1) as well as that of each switches. But in case of an n-level (n>3) NPC inverter, clamping diodes will have different voltage ratings because different reverse voltages might be given to them [8]. 3-level output waveform of this inverter gives high quality output but switching technique is another factor that has to be taken in to account.

The three level three phase neutral point clamped inverter is heart of the unified solar PV and battery storage system. The inverter structures consist of twelve switches and six unidirectional switches connected to the midpoint of the source. The capacitor used before the npc inverter split the neutral voltage to maintain half voltage either positive or negative. The neutral voltage is compensated by MPWM. ANPC inverter includes the DC power source to output DC voltage having a neutral point. An NPC convert DC voltage in to AC voltage in three phases PWM control.

When a mode is selected, consider to a first and a second PWM modes by comparing amplitude of voltage reference with a predefined value that is defined by a minimum pulse width, a first voltage reference means to add a predefined bias value at which a changes to positive/negative within a fixed period to voltage references in respective phases in a first PWM mode, a second voltage reference means to fix the voltage reference in one phase by a value with minimum pulse width when voltage reference in one phase is smaller than a described value that is defined by the minimum pulse width in a next PWM mode and correct voltage references of other two phases so as to make line voltage to a value corresponding to the voltage reference, and a modulation frequency varied over to lower PWM control modulation frequency in the first PWM mode and to suppress power loss caused by switching in the first PWM mode

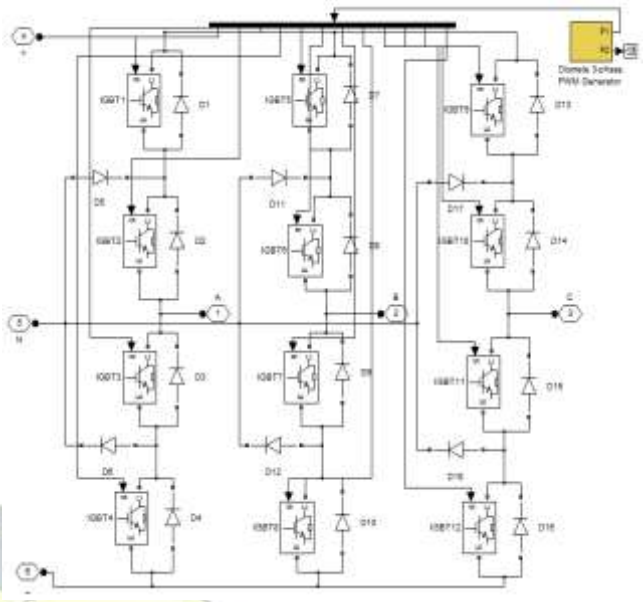

Fig.1 Three Level Neutral Clamped Inverter

A. Switching Strategy

A three-level inverter can assume a total of 27 switching states. The associated switching state 14 vectors are visualized in Fig.2.The notation, e.g. (+ 0 –), indicates that phase *a* is connected to the positive dc rail, phase *b* to the neutral point, and phase *c* to the negative dc rail. The switching state vectors can be associated to four groups:

1. The zero vectors V0+ = V0 (+ + +), V00 = V0 (0 0 0) and V0– =V0 (– – –) do not cause a current flow through the neutral point. Hence the neutral point potential is not affected.
2. Large vectors, such as (+ – –), connect the phase terminals either to the positive or the negative dc-rail. They do not cause a current flow through the neutral point which leaves the neutral point potential unaffected.
3. Medium vectors, such as (+ 0 –), connect one of the three phase terminals to the neutral point. The resulting neutral point current changes the neutral point potential.

Zero vectors: V0.V13.
Large vectors: VI, V3, V5, V7, V9, V11.
Medium vectors: V2, V4, V6, V8, V0, V12.

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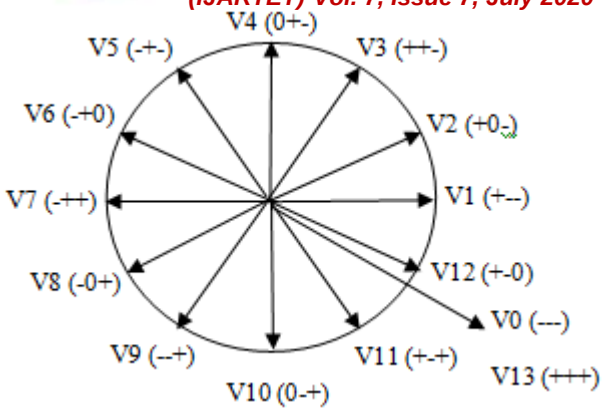

Fig.2 Switching State Vectors

III. Proposed Topology Of 3-Level T Type - Npc Inverter

Driven by the increasing environmental concerns, photovoltaic (PV) power generation systems are attracting the market and research interest. PV grid-connected inverters, acting as the interface between the grid and PV power system, have been studied widely. Although two-level inverter is commonly adopted, three-level topology is found to be more suitable for distributed PV generation systems. As one of the most typical three-level inverter, neutral-point-clamped (NPC) inverter, has been researched in many literatures, with the advantage of low device voltage stress , superior output voltage quality, low switching losses and low du/dt. To simplified the control algorithm and reduce the number of devices, topology of T-type three-level neutral-point-clamped converter (T-NPC) is derived, as shown in Fig.3. Compare to that in NPC, each bridge leg in T-NPC reduces two diodes as shown in Fig.2, so lower conduction losses can be achieved and the operation algorithm can be simplified, while the other advantages of NPC are kept. Considering the lower DC link voltage available in distributed PV generation systems, T-NPC grid-connected PV inverter is more exceptive in efficiency and cost comparing to NPC inverters. This paper attempts to give the power losses calculation method and design procedure of T-NPC PV inverter with high efficiency for power and space. To verify the effectiveness and reliability of T-NPC inverter, temperature rise experiment has been performed.

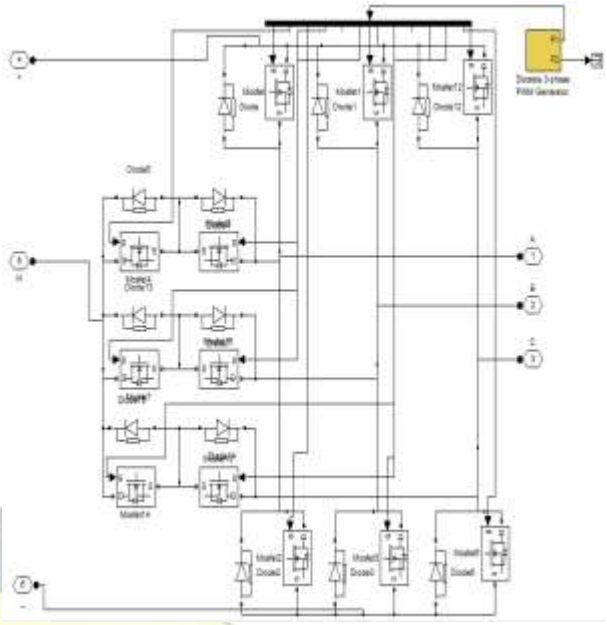

Fig.3 Three Level T-Type Neutral Clamped Inverter

A t-type multilevel converter is an attractive breed of high-performance power converters widely applied in industrial applications. This is because of the lower number of switching devices utilized in their circuit topologies and higher efficiency compared with the conventional I-type neutral-point-clamped converters [1]–[3].However, like other types of multilevel converters, T-type converters are not immune to electrical faults in their semiconductor devices. For instance, switch open-circuit or short-circuit faults could cause catastrophic system failures if no fault-tolerant solutions are provided. Particularly, the availability of fault-tolerant solutions becomes more important when such T-type inverters are applied in safety-critical applications, such as electric vehicles (EVs), uninterruptable power supplies (UPSs), wind and solar energy conversions, and the like. Although T-type converters have certain inherent fault-tolerant capabilities due to their unique topologies, as reported in [4], the output voltage and linear modulation range have to be significantly reduced during the fault-tolerant operation region. Such de rating is not preferred in certain applications (e.g., UPSs, EVs, etc.), where rated output voltages and output power are stringent requirements. Therefore, it would be of great significance to improve T-type converters' topology with enhanced fault-tolerant capability, to guarantee full output voltages during post fault operations. The existing solutions for the fault-tolerant operation of T-type converters are mainly achieved by paralleling multiple redundant inverter legs, such as the circuit topologies detailed in [5] and [6], which achieves full output voltages under inverter fault-tolerant conditions, but at much higher system cost with decreased inverter efficiency due to a large number of redundant semiconductor devices involved in the

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converter circuits. In fact, most of the redundant semiconductor devices in the existing fault-tolerant topology simply idle in the circuits without any contribution to system performance improvement under healthy conditions, resulting in decreased inverter efficiency due to the associated device conduction and/or switching losses.

The Three-phase of T type -NPC inverter is shown in Fig.2, in which T1~T4 are MOSFET switches, D1~D4 are FWDs, C1 and C2 are DC link capacitors. Assume that the direction of current flowing out from bridge leg is positive. Generally, the output terminal of the bridge leg can be connected to positive (P), neutral (O), or negative (N) side of DC link, and the output voltage can be set to three values, as shown in Table 1.

Table –I: Switching Table for T-Type NPC inverter

Operation mode	T1	T2	T3	T4	Output Voltage
P	ON	ON	OFF	OFF	+Vdc/2
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

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IV. SIMULATION RESULTS

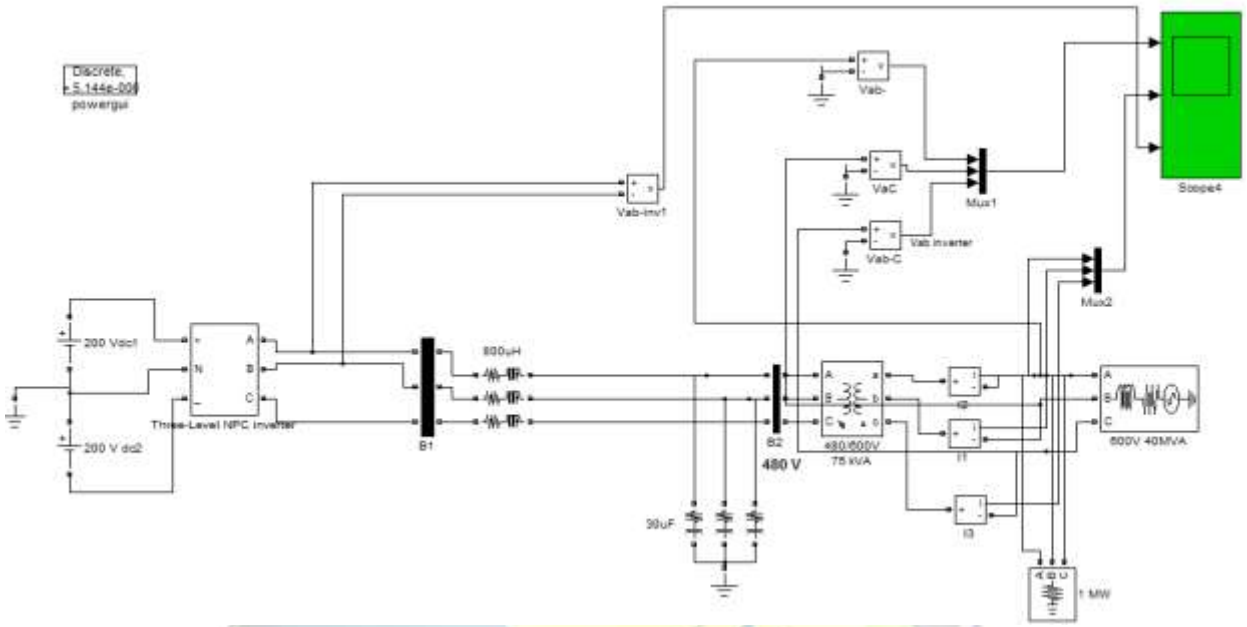

Fig. 4 Simulation model of 3-Level Conventional NPC inverter

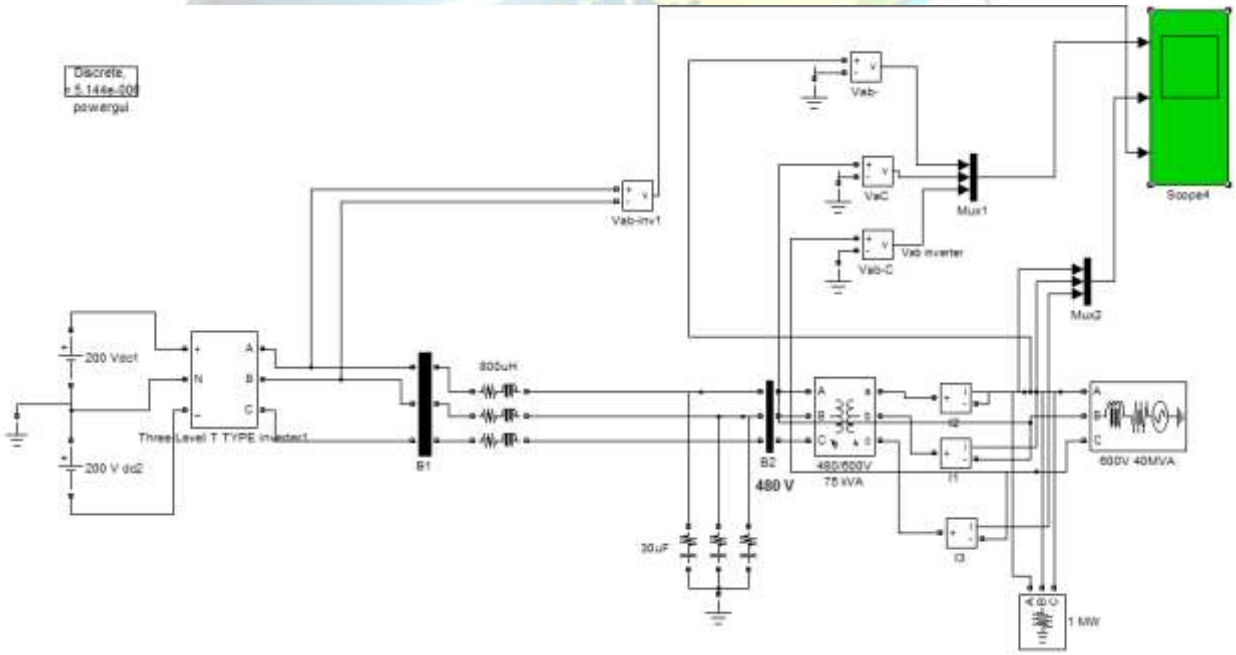

Fig. 5 Simulation model of 3-Level Proposed T-Type NPC inverter

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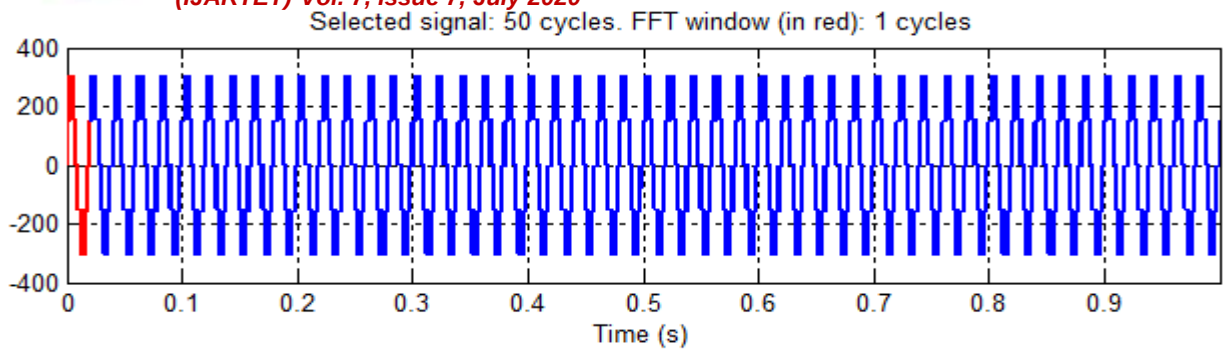

Fig. 6 Line voltage of 3-Level Conventional NPC inverter

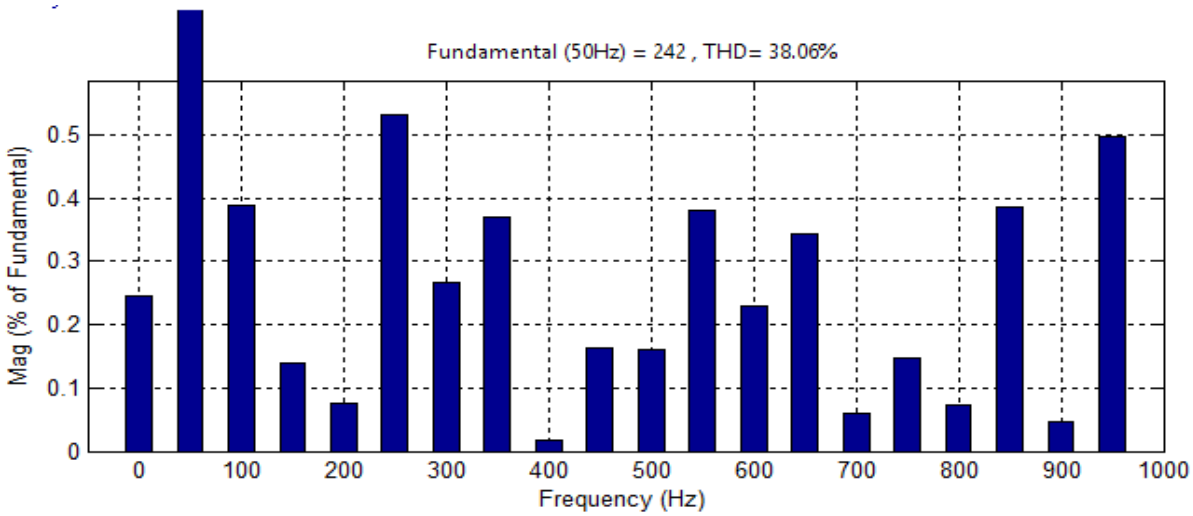

Fig. 7 THD of 3-Level Conventional NPC inverter

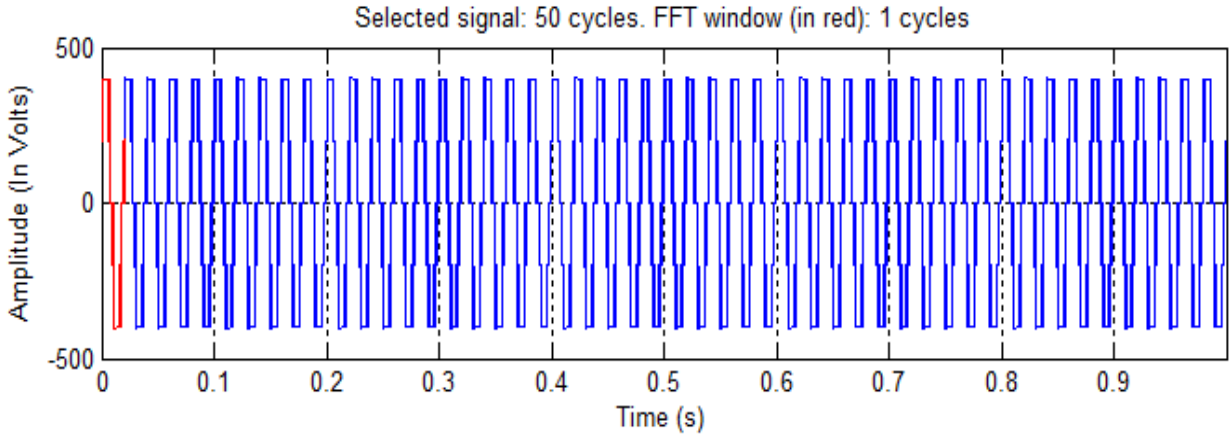

Fig. 8 Line voltage of of 3-Level Proposed T-Type NPC inverter

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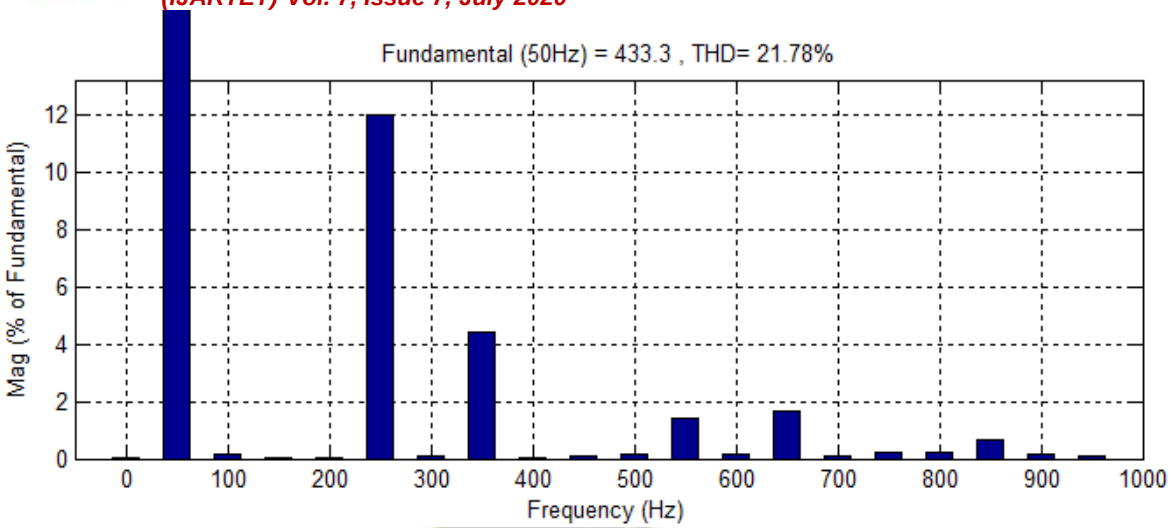

Fig. 9 THD of 3-Level Proposed T-Type NPC inverter

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V. CONCLUSION

A Three-phase T-type Three level inverter topology has been proposed in this paper. With a carrier-based modulation method, three output voltage levels can be achieved in the proposed topology. Compared with the existing topologies, both the number of components and voltage stresses across the components are reduced. A voltage self-balancing circuit is utilized to balance the three dc-link capacitor voltages. The simulation results have THD% and also Line voltage were verified the performance of the proposed inverter .Further study could be focused on the voltage-balance control for the three dc-link capacitor voltages.

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