ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 6, Issue 7, July 2019

PV based Hybrid Multilevel DVR with SVPWM for Power Quality Improvement

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Abstract: In this paper the power quality disturbances such as voltage sag, swell is mitigated by using a custom power electronic device, Dynamic Voltage Restorer (DVR) which is of seven level multilevel inverter composed of Capacitor Clamped and Cascaded H-bridge topology. The DC link capacitor of the Hybrid Multilevel Dynamic Voltage Restorer is supplied by the PV panel to compensate any voltage deviations that occur in a system caused by power quality issues .The Hybrid Multilevel configuration presented has many advantages over conventional multilevel inverter and the PWM pulses to the inverter are given by Space Vector Pulse Width Modulation (SVPWM) .Simulations are carried out in MATLAB/SIMULINK software in order to evaluate the performance of Photovoltaic fed DVR in mitigating the voltage disturbances .The Simulation results show that the proposed multicell inverter provides different levels of output voltages and high modularity and the study also shows that Space Vector Modulation is more efficient in reducing the Total Harmonic Distortions.

Keywords: DVR, Sag, Swell, Harmonics, Photovoltaic array, SVPWM, SPWM.

I. INTRODUCTION

Present days power quality issues are becoming major problems in over distribution system, in order to get constant load voltage power quality issues are to be mitigated. However, especially in the distribution systems, having more nonlinear loads which are significantly affecting the quality of the power supply. Because of these nonlinear loads, the purity of the supply waveform is disturbing. This ends up producing power quality issues [1]. Voltage sags (dips) are defined as one of the most frequently occurring power quality problems. The reduction in voltage magnitude between 10% to 90% compared to nominal voltage from half a cycle to a few seconds are termed as voltage sags. There are different ways to mitigate voltage dips in power quality systems. Among those, the dynamic voltage restorer (DVR) is the most effective device, based on the voltage source converter (VSC) principle [2]. Swell is opposite to that of a Sag, having an increase in AC Voltage for a voltage magnitude greater than 110% of the nominal voltage. Usually swells are caused by abrupt switching of heavy loads which leads to transients, interruptions and complete collapse of the system etc.

The definition of a harmonic is "a sinusoidal component of a periodic wave or\ quantity having a frequency that is an integral multiple of the fundamental frequency." i.e. a pure sine wave in terms a clean power waveform without any harmonics.

This paper is structured as follows: Section II describes briefly the operation of DVR. Section III presents the principle of operation of Hybrid Multilevel inverter. Section IV presents PV fed DVR model. Section V presents Space Vector Pulse Width Modulation (SVPWM). Section VI represents results of multilevel DVR and the output results and conclusion in Section VII.

II. OPERATION OF DVR

The DVR can mitigate the load voltages from the problems such as sag, swell, and harmonics that are produced in the supply voltages. Hence, it can protect the critical consumer loads from tripping and consequent losses. [9].

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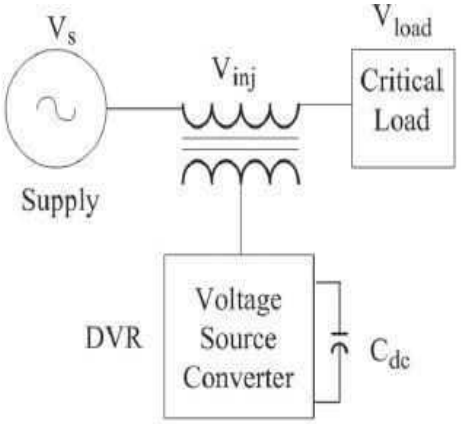

Fig.1.Configuration of DVR

The schematic of a DVR-connected system is shown in Fig. 1. The voltage Vinj is inserted such that the load voltage Vload is constant in magnitude and is in prescribed limits, although the supply voltage Vs is not constant in magnitude or distorted. During the voltage sag, the voltage is reduced and during swell it is increased.

During normal operations the DVR doesn't inject any voltage and remain ideal and when abnormal conditions occur the DVR comes into action. DVR injects the voltage through a booster transformer thus maintaining the load voltage in prescribed limits.[3].

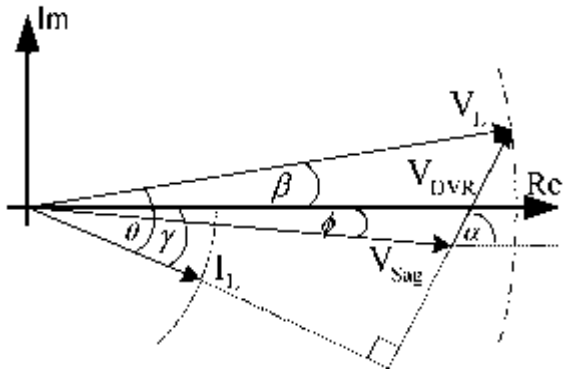

Fig.2. Voltage Sag compensation

The above fig.2. Shows the phasor diagram of compensated voltage which can be analysed in different ways depending on the angle of load voltage. In this the DVR continuously tracks the supply voltage (Vs) and injects the missing voltage.

II. Proposed Hybrid Multilevel Inverter

A multicell inverter has several advantages over a traditional two-level inverter that uses high switching frequency pulse width modulation (PWM). The proposed Hybrid Multilevel Inverter composes of Capacitor Clamped and Cascaded H-bridge. The three-level H-bridge inverter topology used in the Cascaded multilevel inverter presents some advantages over two level topologies. Beyond the obvious advantage is the number of output levels, this structure allows to double the peak to peak voltage from vdc to 2vdc, by applying to the load the voltages: +vdc, 0 and −vdc. In This topology would be even more powerful if the dc-link voltage is supplied by a PV which is a variable DC voltage and is adjusted according to load requirements.

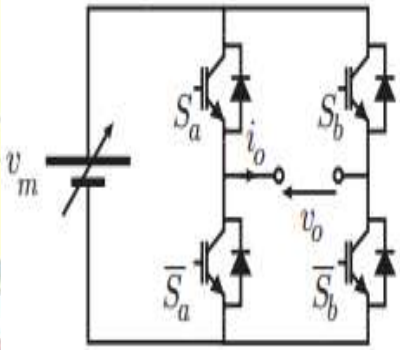

Fig.3.Multicell conceptual model

The multicell inverters have many attractive properties such as it is suitable for medium and high voltage applications and particularly transformer less preserving the output voltage levels. The switches of these multicell inverter are operated in complementary to each other the values for Vm are calculated by using following formula.[4].

$$Vm = \quad k/Vdc; \quad I \leq k<1$$

In the proposed multicell Inverter the capacitor clamped multilevel inverter gives four level output including zero and the output of this inverter acts as input the cascaded H-bridge hence the output is of seven level. The levels of output obtained in the MCML are V, 2V/3, V/3, 0, -V/3, 2V/3, -V for a DC supply of V volts.[10].

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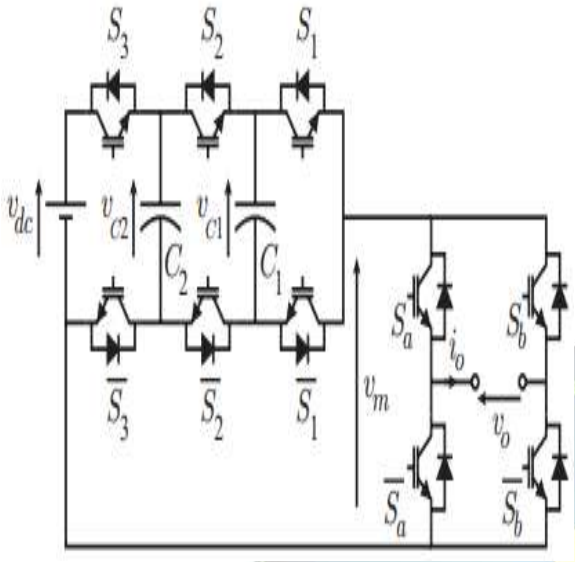

Fig.4. Proposed Hybrid Multilevel Inverter

With a proper modulation technique, the number of levels that this new topology can reach is:

$$L = n\,(2i+1) - 1$$

Where n is the number of cells connected in series and 'i' is the number of FC sub-cells on each cell.

IV. PV BASED DVR SYSTEM

To process electrical current through PV power electronic device DC-DC converters are used. In this proposed system the DC-DC converter is used. A Buck - Boost converter is used to generate the voltage to higher rate. A simplified model of PV cell is shown in the fig.5.A single diode model with a series connected resistance is used to generate the voltage based on the equivalent circuit with an ideal current source.

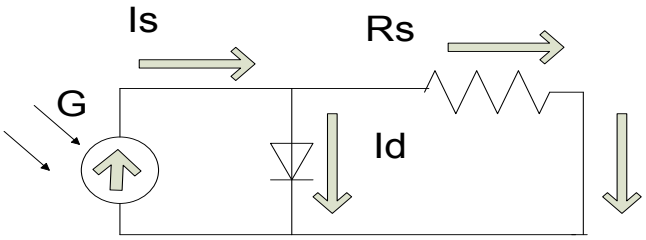

Fig.5.PV cell with single diode and series resistance

The V-I characteristics of solar cell with one diode and series resistance is given by:

$$I = Is - Io\left[e^{\frac{q(V+IRs)}{mkt}} - 1\right]$$

Where Io is the diode reverse bias saturation current, q is the electron charge, m is the diode ideality factor, k is the Boltzmann's constant, and T is the cell temperature. In this proposed work Maximum Power Point Tracking (MPPT) technique along with PI controller is used to track the voltage. Fractional open circuit voltage MPPT controller is used and the working of MPPT controller with PI controller is described in block diagram as shown in fig.5.

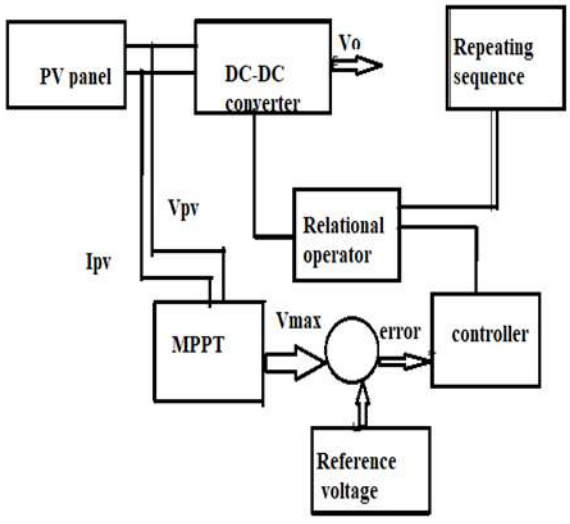

Fig.6.Block diagram of PV array with controller.

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The open circuit voltage and short circuit current are calculated using relevant formulas from the equivalent circuit. The calculated parameters are tracked by fractional open circuit MPPT controller. Compared to other MPPT techniques this proposed MPPT technique is efficient in terms of cost, absence of filter, time, memory etc. [5].

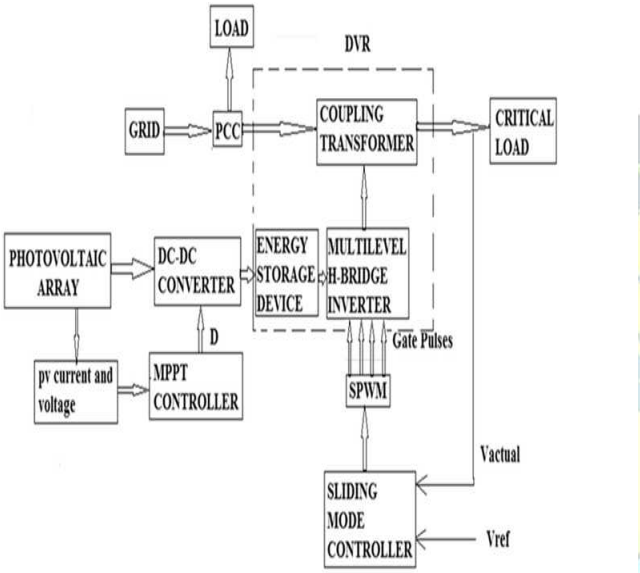

Fig.7.PV based DVR system

The MPPT tracked voltage is considered as actual voltage and the reference voltage is given to the PI controller. The PI controller takes necessary actions and generates an error signal which is given to the DC-DC converter through PWM generator and the relational operators, hence the duty ratio and switching frequency are noted and output is generated from converter which is fed to the Hybrid Multilevel inverter (DVR).[6].

V. PROPOSED CONTROL STRATEGIES

In this proposed work the PWM technique used is space vector modulation along with PI controller. By using PI controller, the reference signals are generated and that generated error signals gives reference sinusoidal signals that is used as reference and for SVPWM PWM pulses are given to the inverter.

Space Vector Modulation with PI controller:

The SVPWM technique is the most advanced digital PWM technique compared to the other PWM techniques because of its attractive and efficient characteristics. The SVPWM technique is very effective in reducing the Total Harmonic Distortions (THD). The three sinusoidal voltages are taken as reference from the voltage measurement of the source voltage block and given to the Phase Locked Loop (PLL) the PLL generates or stabilises the input signal in terms of magnitude and angle and the stabilized signal is given to the PI controller the actual signal and the reference signal is compared generated from the PI controller is given to unit function to generate an error signal and that produces a sinusoidal signal that is used as reference signal to SVPWM generation .[7].

The generated reference signals such as Va, Vb, Vc are given to coordinate transformation (abc reference frame to the stationary dq frame) and the three reference sinusoidal voltages which are at constant amplitude vector rotating at constant frequency .The reference signal generated through this transformation and is sampled with sample time (Ts).This PWM technique approximates the reference voltage (Vref) in eight switching state vectors (Vo to V7).

$$Va=Vm \sin(wt)$$
$$Vb=Vm \sin(wt-120)$$
$$Vc=Vm \sin(wt+120)$$

The SVPWM considers these three space vectors as a single vector.

$$Vs=3/2Vm[\sin(wt)-j\cos(wt)$$

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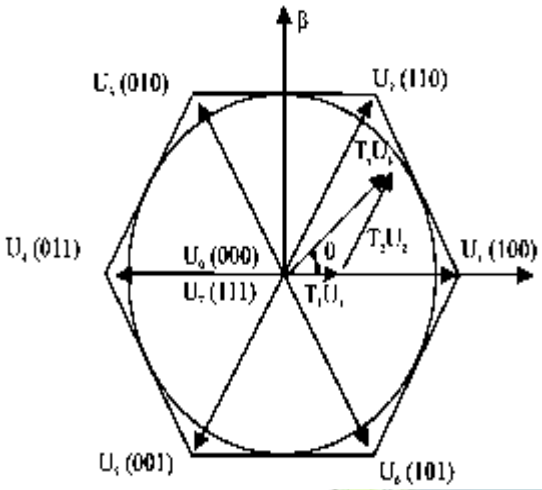

Fig.8.SVPWM switching state Vectors

There are eight possible switching vectors in which six are active state vectors and two are non-active state vectors. (0,0,0),(0,0,1),(0,1,1),(0,1,0),(1,1,0),(1,0,0,),(1,1,1), here (0,0,0) and (1,1,1) are non-active states and remaining are active states. In order to generate the SVPWM technique first we have to determine the Vd, Vq,(coordinate transformation), Vref and angle (alpha).Next we have to determine the time duration T1,T2,T0 through required function formulas and in the final step determine the switching times of each transistor[8] .

$$Vref=\sqrt{Vd^2 + Vq^2}$$

Reference voltage is sampled at regular interval 'Ts'.

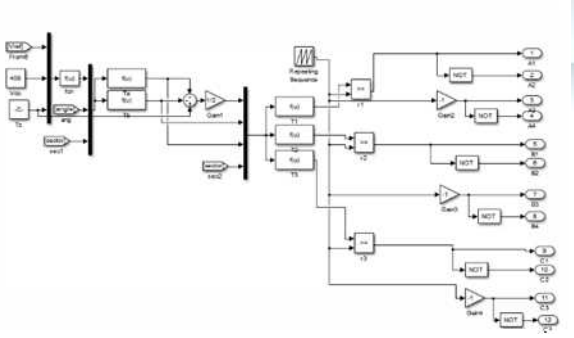

Fig.9.Simulation circuit of SVPWM generation

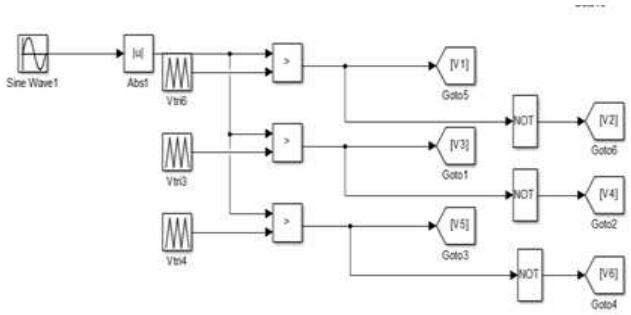

Fig.10.Simulation circuit of SVPWM generation for MLI

The phase disposition method is used in which all carrier wave has same phase and amplitude.

VI. Simulation Results

In this proposed Hybrid Multilevel DVR all types of symmetrical and non-symmetrical faults are simulated with a nominal voltage of 1 p.u.and PV output power of 3500W and ripple filter inductance of 10mH and capacitance of 20 uF. The injection transformer used is linear transformer of ratio 1:2 and the proportional values of Kp is chosen as 0.9 and given as reference to the PWM generation circuit.

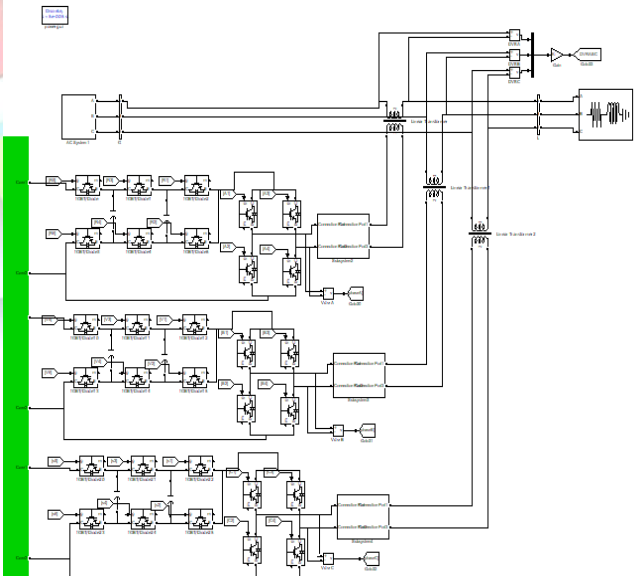

Fig.11.Simulation circuit of proposed DVR

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A. Solar Output Power:

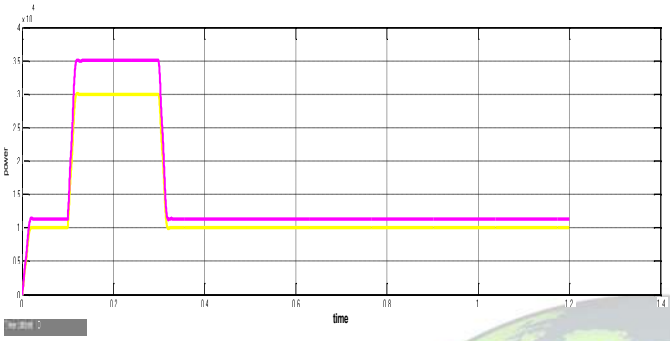

Fig.11. (a). Solar output Power

B. SVPWM output waveform

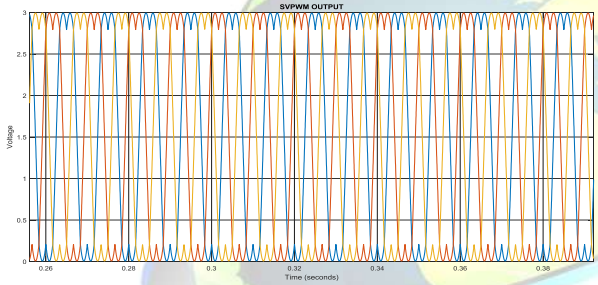

Fig.11. (b). SVPWM output

C.Sevel level Output of Hybrid MLI:

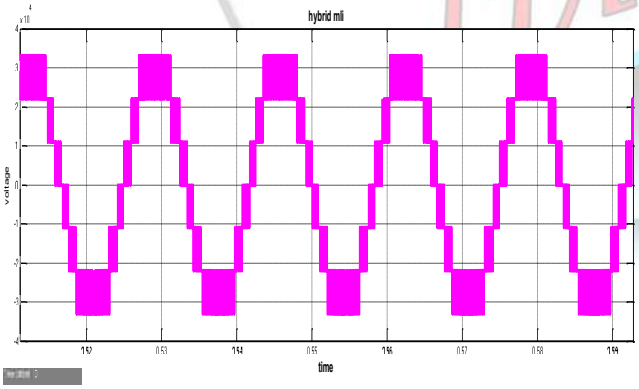

Fig.11. (c). Seven level output of phase-A

D.Sag and Swell in 3-phases:

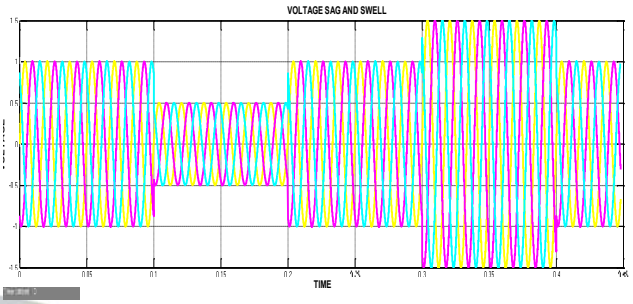

Fig.11. (d). ***Source voltage (Vs) with sag and swell.***

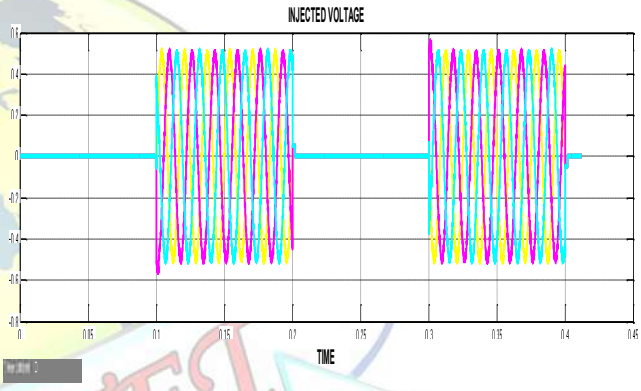

Fig.11. (e). ***Injected Voltage (Vc)***

From the above fig the sag is created for 3 phases for time 0.1 to 0.2. and swell for 0.3 to 0.4.

E. Swell in 2 -phases:

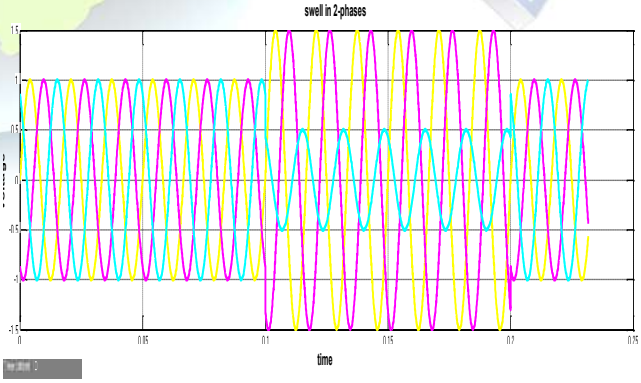

Fig.11. (f). ***Source Voltage (Vs)***

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Injected voltage:

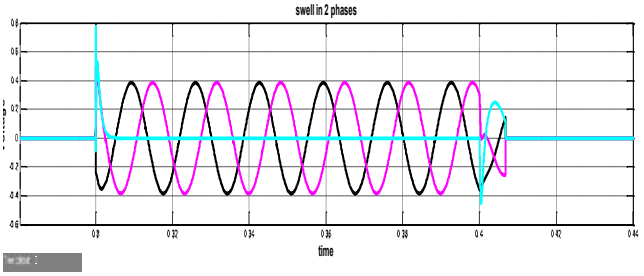

Fig.11. (g). Injected Voltage (Vc)

F. Swell in 1-phase:

Fig.11. (h). Source voltage (Vs).

From the above fig the swell is created for 1 phase for time 0.3 to 0.4.

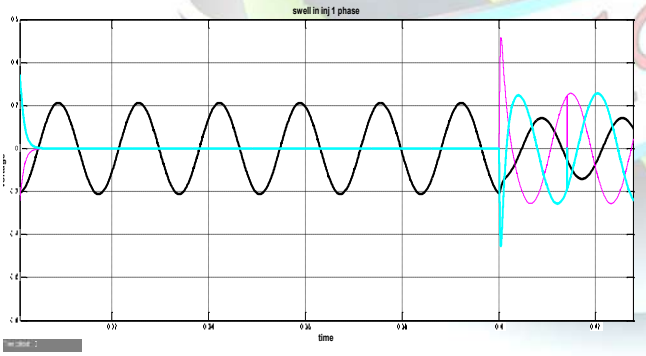

Fig.11. (i). Injected Voltage (Vc)

G. Interruption:

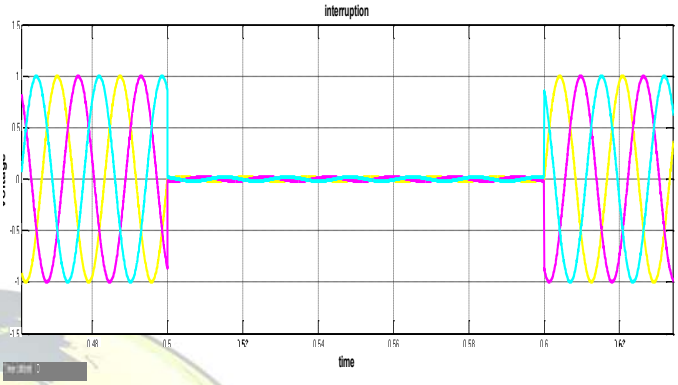

Fig.11. (j). System voltage (Vs) with interruption

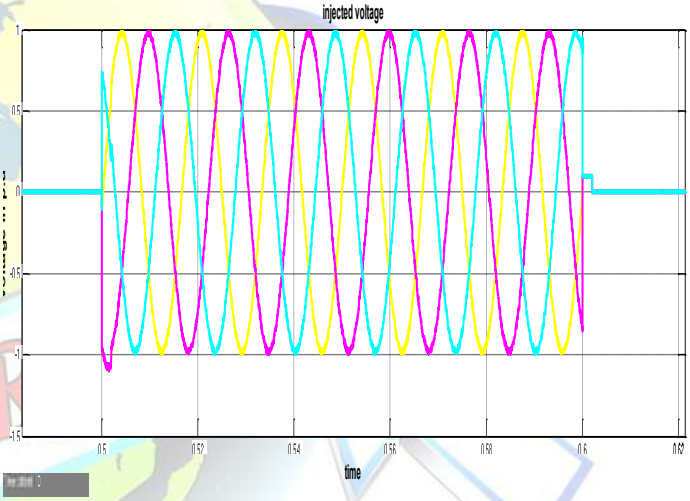

Fig.11. (k). Injected voltage (Vc)

From the above fig. the source voltage (Vs) are shown for interruption for time 0.5 to 0.6.

H.Voltage sag in 2-phases (LLG):

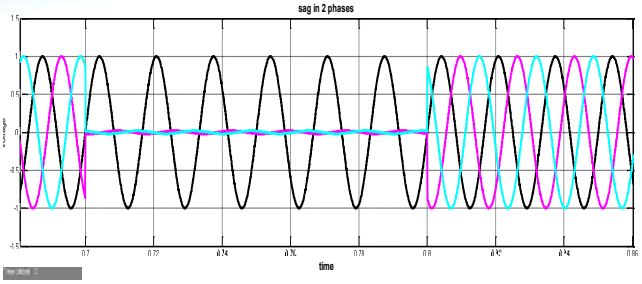

Fig.11. (l). Source voltage (Vs)

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From the above fig.the source voltage (Vs) with sag in 2 phases is shown and injected voltage (Vc) for time between 0.7 and 0.8.

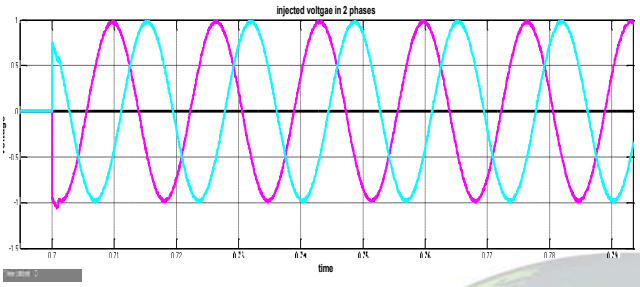

Fig.11.(m). Injected voltage (Vc)

I. Voltage sag in 1-phase (LG):

Fig.11. (n). Source voltage (Vs)

From the above fig. the source voltage (Vs) is shown for 1-phase and the injected voltage (Vc), Wavelet coefficients (Cd) for the time between 0.9 to 1.0 is represented

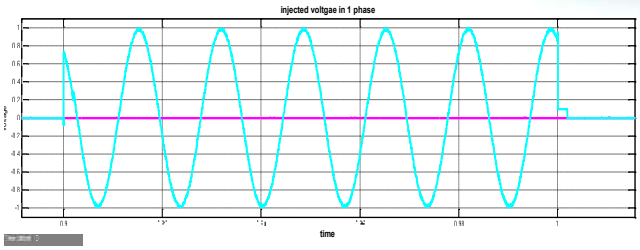

Fig.11. (o). Injected voltage (Vc)

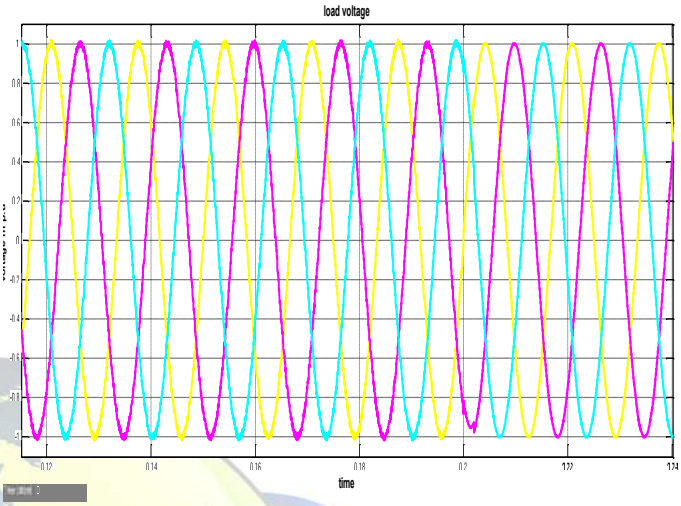

Fig.11. (p). Load Voltage (VL)

Table I: THD comparison table for SVPWM

Fault						
Sag			Swell			Outage
1-phase	2 -phase	3-phase	1-phase	2-phase	3-phase	1.41
0.51	0.58	1.33	0.78	0.81	1.39	

From the above tabular columns, it is clear that the THD % for SVPWM is less and is under IEEE standard region.

VII. CONCLUSION

The modular Multilevel inverter-based DVR is evaluated for mitigation of both balanced and unbalanced (sag and swell) types of faults. The performance of PV based multilevel DVR is evaluated for power quality improvement .The drawback of self-supported DVR is overcome by using PV based DVR .The THD content in the output voltage is less than 5% which is well within the acceptable limits of IEEE standards.

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