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Performance Evaluation of Low Power Mongrel Flip-Flop using Duo Sleepy Stack Inverter

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Abstract: In this paper inverter pairs are designed using leakage power reduction technique known as sleepy stack technique. The static CMOS inverter in conventional DDFF is replaced by sleepy stack inverters because as feature size scales down below 0.1u leakage power gets increased. The simulations were performed under 90 nm technology in Tanner Tool. The supply voltage is given as 1.8V throughout for the entire simulation analysis. The leakage power and total power for static CMOS inverter and sleepy stack inverter were compared. It is observed that sleepy stack inverter has reduced leakage power to 98% and the total power is reduced to 14.2%. The total power is reduced to approximately 18%, in proposed D, flip flops. The leakage power is reduced to 90.1%. As proposed flip-flop has improved performance in term of leakage power, total power and power delay at high speed, it can be widely used in high performance application.

Keywords: Flip flops; leakage power; low power; leakage reduction, tanner simulator tool.

I. INTRODUCTION

Since the Past Decade, consumption of power in VLSI chips has rapidly been raising. The Scientist Moore's Law drives VLSI technology to rapid increases in transistor densities and radio clock frequencies. Scaling in the last few years in past year in VLSI technology it is shown that a number of transistors in a single chip raise approx 40% annually. The Operation frequency of VLSI systems raises approx 30% per year.

While capacitance and input voltages scale decrease meanwhile, consuming the power of VLSI chips is raised continuously. In another way, a cooling system cannot improve as well as the power consumption raises. Therefore in the near future chips are expected to have circumstances of cooling system, and solution for this will be costlier and inefficient.

For high optimistic gainer VLSI chip-design, the choice of the back-end approach has a significant impact on the design in term of time and cost. Making every single gate from scratch is not necessarily the best technique. Instead, an adequate set of premeditated standard cells can be applied as building blocks to design most of the operative blocks. Semiconductor manufacturers offer definitive cell libraries, which are also promoted by CAD tools in automated design stream including the eventual physical auto-installation and routing [1,2].

However, the excerpts of the criterion cells as well as their attainment have some circumstances. Although the attainment circumstances, criterion cell libraries could be utilize for even in design of high performance VLSI chips. Generally, only a slight portion of the chips has performance-critical units, and the rest of the design could be maximally automated to trim the time without degrading the desired performance. Further, the concept of cell library can be drawn-out to support the full-custom part of the chip. Custom (in-house) cell libraries can be made and contained by the designers of the performance critical units. This results in a sharp decrease in the number of cells to be created and verified trimming the total chip layout time certainly [3,4].

Therefore, to design high performance chips, development of an efficient cell library is essential. A cell library contains a number of cells with different functionalities, where every cell might be have different size and driving capability. Two central categories of cells includes in cell library are flip-flops and latches. In any synchronous VLSI chip design these are extremely important circuit elements.

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They are not only responsible for accurate timing, functionality, and performance of the chips, but also their clocked devices that consume a significant portion of the total active power. In comparing with the power crash for different design in VLSI chips, latches and flip-flops are the major part of the power consumption in synchronous systems. The components have an impact on power consumption and speed of VLSI systems, are Latches and flip-flops. Thus, analysis on low-power and high performance latches and flip-flops is necessary. A universal flip-flop with the outstanding performance, low energy usage, and high robustness in resistance to noise would be a perfect component in cell libraries. However, improving the performance of flip-flops generally involves significant power and robustness trade-offs. Hence a set of several latches and flip-flops with best performances are necessary to bind the use of more power consumption and noise-sensitive components only for smaller part of the chips with critical performance units. These elements trimmed global and unnecessary use of power as well as robustness degradations, which would result in overall trim in noise margin requiring extra careful and time consuming design.

In contrast to different published results [1-7], a wide power-performance area for each of the eight flip-flops has been covered. For compact size, useful operating ranges of the flip-flops have been identified. The design-space exploration not only enables a true comparison, but also it beat potentially large overlaps in operating range of the flip-flops. This term provides an opportunity to trim the number of different circuit topologies in a flip-flop library.

II. EXISTING D FLIP FLOPS

Flip-flop (FF) being a storage element occupies a significant space in digital circuit design such as register, counter and finite state machine. In view of its huge applications, it is important to understand its operation in details obtaining a high level of insight into its various performance metrics such as speed, power dissipation, hold-time, set-up time and area. Thus, there is a significant research effort on Flip Flop which revealed various techniques for its performance improvement and optimization.

There can be various type of FF, each having advantage/disadvantage over one another. D-FF is among commonly used FFs because of its relatively simple operation. It can be either of static or dynamic type as shown in Fig. 2 and Fig .3. In static flip-flop output data is stored using latch whereas in dynamic flip-flop output is stored by using the node capacitance and thus it needs clock pulse at regular interval to preserve data at appropriate logic level. Static flip-flop generally utilizes more transistor than a dynamic flip-flop. Glitches and charge sharing are two drawbacks that happen in dynamic type D-FF, resulting in a different state of the circuit node voltage.

The FF can be either level or edge triggered, and thus can be classified as follows:

- Positive level triggered flip-flops
- Negative level triggered flip-flops
- Positive edge triggered flip-flops
- Negative edge triggered flip-flops
- Dual edge triggered flip-flop

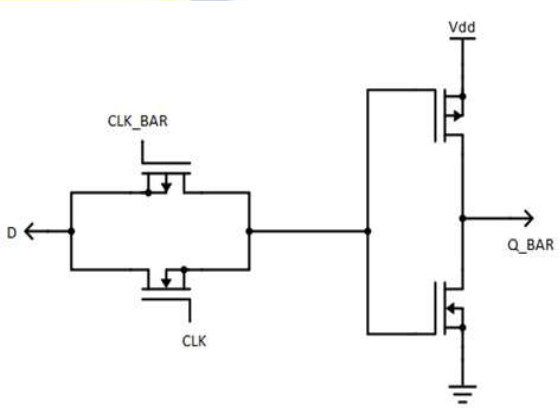

Fig. 1. Dynamic D flip flop

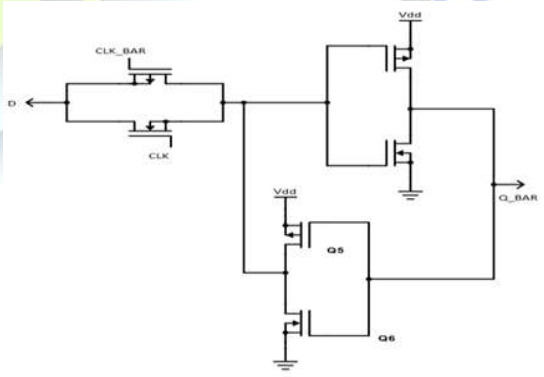

Fig. 2. Static D-flip flop

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A. Positive Level Triggered Flip-Flops

These all flip-flops are active when clock is at active high level, and don't respond to any transition in clock or when clock is at active low. Fig.3 and Fig.4 shown typical example of positive level triggered static and dynamic type D flip-flop respectively. It is clear that input data is transfer to output when clock is at logic high level.

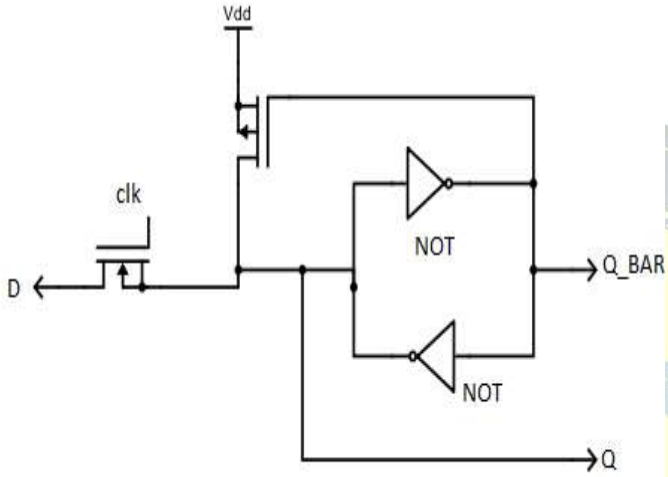

Fig. 3. Positive level static D-flip flop

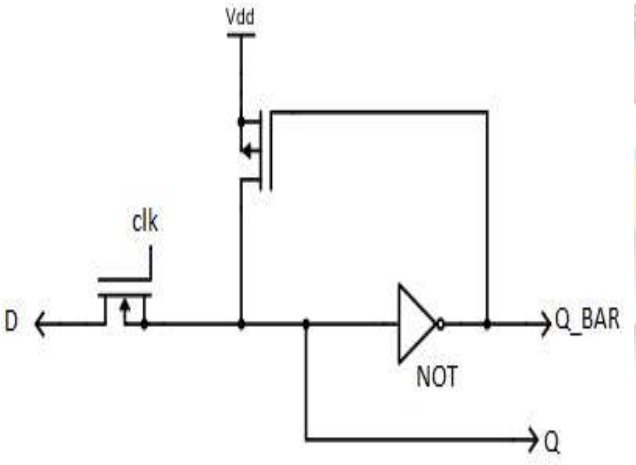

Fig. 4. Positive level dynamic D-flip flop

B. Negative Level Triggered Flip-Flops

As per name of negative level triggered flip-flops work only at active low of clock pulse. Circuit schematic of negative level triggered flip-flops by using transmission gate shown in Fig. 5 and 6. Transmission gate based flip-flops don't need voltage boost circuit techniques as in Fig. 3 and Fig. 4 which are based on pass transistor.

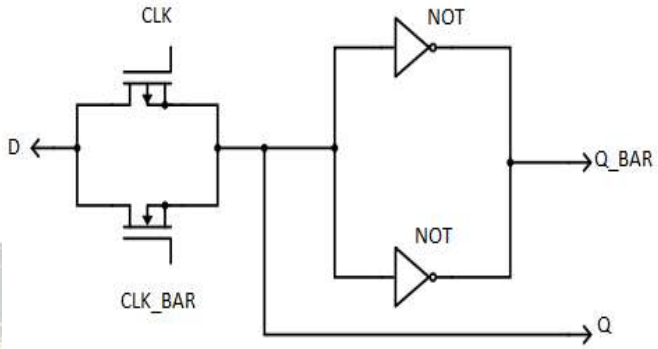

Fig. 5. Negative level triggered static D-flip-flop

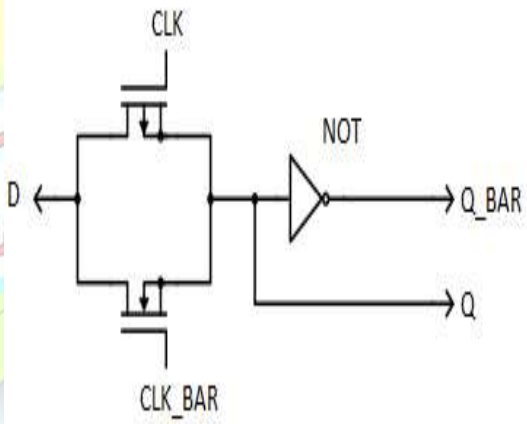

Fig. 6. Negative level triggered dynamic D-flip flop

C. Positive Edge Triggered Flip-Flops

When rising edge of clock is utilized to trigger the flop-flop, such flip-flops comes under the category of +ve edge triggered flip-flops. Schematic of +ve edge-triggered flip-flop shown in Fig. 5 and Fig. 6.

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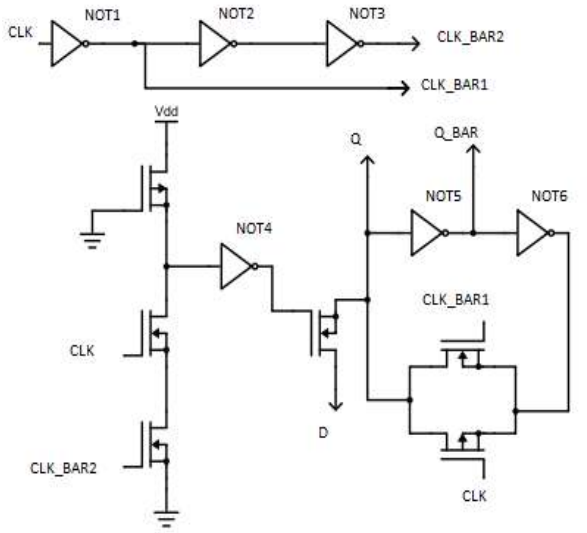

Fig. 7. Positive edge triggered static D-flip-flop

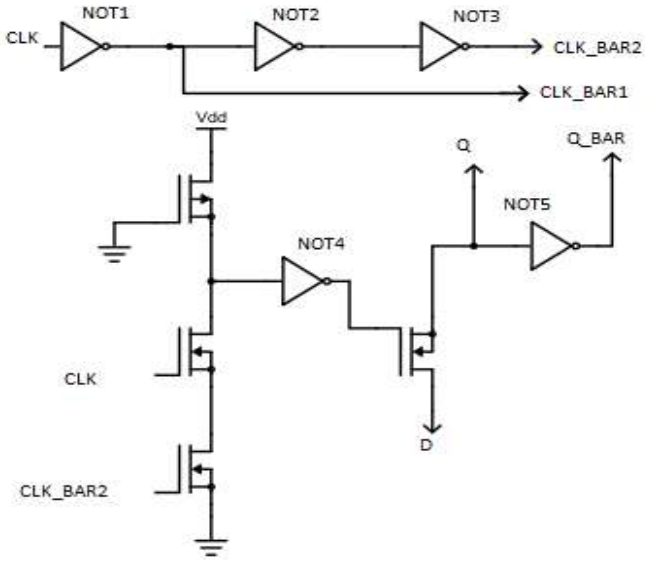

Fig. 8. Positive edge triggered dynamic D-flip-flop

III. PROPOSED FLIP-FLOP ARCHITECTURE

In the proposed flip flop architecture the inverter pairs are designed using leakage power reduction technique known as sleepy stack technique. The static CMOS inverter in conventional DDFF is replaced by sleepy stack inverters because as feature size scales down below 0.1u, leakage power gets improve. When a static CMOS inverter is used in low feature size technology, the supply voltage gets reduced which in turn reduces the threshold voltage. The transistors used were low threshold voltage. So there is greater risk of leakage current in this case. Short channel length and change in gate length also pave way for higher leakage. This sleepy stack technique is the combination of sleep transistor technique and forced stack technique. It uses high threshold voltage transistors and stack effect to reduce the leakage power.

The sleepy stack inverter is shown in the Fig 10. P1, P2, N1, N2 are high threshold voltage transistors. P3 and N3 are low threshold voltage transistors. P2 and N2 are sleep transistors. It operates on two modes.

A. *Active mode* - In active mode, S=0 and S_{bar}=1. The sleep transistors are switched ON throughout this mode. It has faster switching time. As sleep transistors are switched on throughout, it passes the logic values from source to drain and directly into the low V_{th} transistors regardless of the status of transistors which are parallel to sleep transistors.

B. *Sleep mode* - In sleep mode, S=1 and S_{bar}=0. The sleep transistors are switched OFF. Though they are switched OFF, the transistors parallel to sleep transistors helps in maintaining exact logic state of the design. Reduction in leakage power is achieved by two ways. Firstly high V_{th} transistors parallel to sleep transistors are used to block the leakage current. Secondly by stack effect created by P1, P3 and N1, N3 transistors. When two or more transistor which are stacked together are turned off simultaneously, there is greater reduction in leakage current. This effect is called as stack effect. Suppose when input =1, the stacked NMOS transistors N1, N3 are switched ON and stacked PMOS transistors P1, P3 are switched OFF. Thus the stacked PMOS do not allow any leakage current to pass through. Though there is large leakage power reduction, area is a trade-off.

The proposed flip flop is shown in Fig 9. When this sleepy stack inverter pair is used in the flip flop, the overall leakage power reduction of the flip flop can be achieved by operating the flip flop in sleep mode. The total power is also reduced which can be obtained by running the flip flop in active mode. This proposed flip flop also operates as like DDFF in evaluation and pre -charge phase. The latching of input takes place at evaluation phase and

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holding of the output takes place in pre-charge phase. The overlapping period (T_{ov}) of the flip flop is set as 61ps with supply voltage of 1.8V. Hold time of logic 0 ($T_{hold}0$) is observed to be 24ps. Hold time of logic 1 ($T_{hold}1$) is observed to be 35ps. The race around problem is overcome by the 1-1 overlap of CLK 1 and CLK 2.

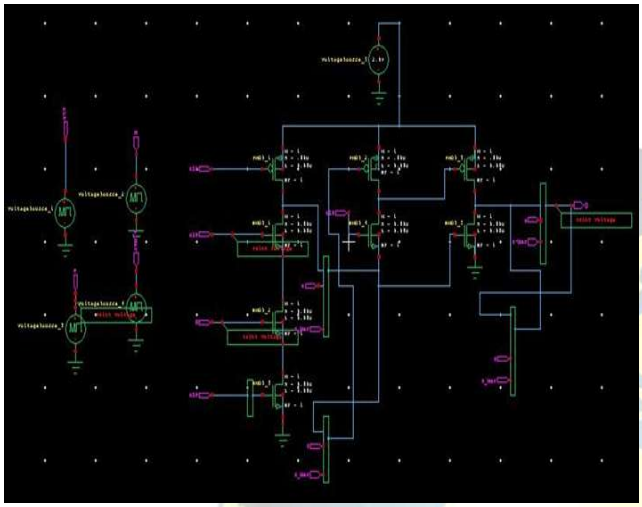

Fig. 9. Proposed D flip-flop.

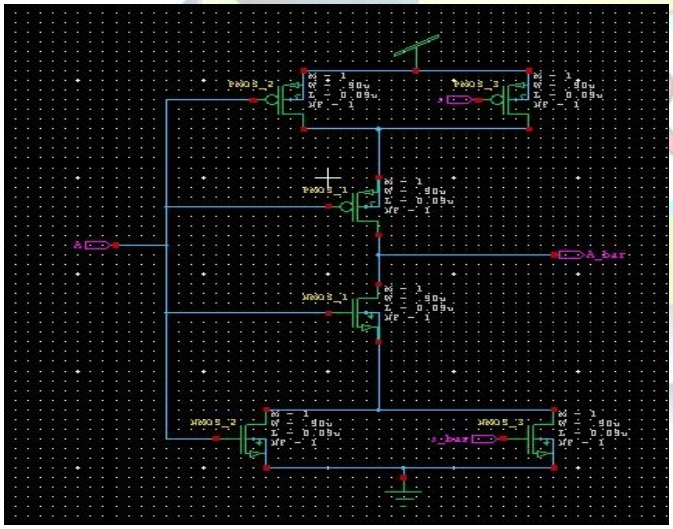

Fig. 10. Sleepy stack inverter

IV. SIMULATION AND RESULTS

The simulations were performed under 90 nm technology in Tanner Tool. The supply voltage is given as 1.8V throughout for the entire simulation analysis. The leakage power and total power for static CMOS inverter and sleepy stack inverter were compared. It is observed that sleepy stack inverter has reduced leakage power to 98% and the total power is reduced to 14.2% as given.

The flip flop is operated at 1GHz clock frequency. It has a negative set up time and positive hold time with respect to 1-1 overlap of CLK and CLK_{Bar}. The power, delay and PDP are calculated at 27% data activity for the conventional D flip flops and proposed D flip flop. The total power is reduced to approximately 18%, in proposed D flip flops. It is because of switching power dissipation. The delay is maintained in the proposed D flip flop as like conventional flip flop. The leakage power and total power is calculated for different data activities of conventional and proposed flip flop.

The total power of proposed flip flop is observed to be less for 27% and 0% data activities when compared with conventional flip flop. The power consumed at 100% data activity is same for both the conventional and proposed flip flops. The static leakage performance of flip flops for various input –output patterns were analyzed. When CLK=1, D=0, Q=0 the static leakage is minimum as given. This concludes that the run-time leakage power and total power depends on the input vectors also.

TABLE 1 PERFORMANCE OF INVERTER

Flip - Flops	Leakage power (nW)	Total Power (µW)	Delay (ns)	PDP (fJ)
Conventional D Flip Flop	52.596	63.25	4.6205	292.25
Proposed Sleepy Stack	4.9852	49.17	3.7438	238.73

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TABLE 2 PERFORMANCE OF PROPOSED D FLIP-FLOP

Inverter Type	Leakage power (pW)	Total power(nW)
CMOS	3897.6	403
Sleepy Stack	3.2497	358.1

TABLE 3 COMPARISON WITH EXISTING LITERATURE

Comparison	Leakage power (nW)	Total power (µW)	Delay (ns)	PDP (fJ)
H. Evangelene et al [1]	5.7438	50.44	4.6175	232.91
Proposed	4.9852	49.17	3.7438	238.73

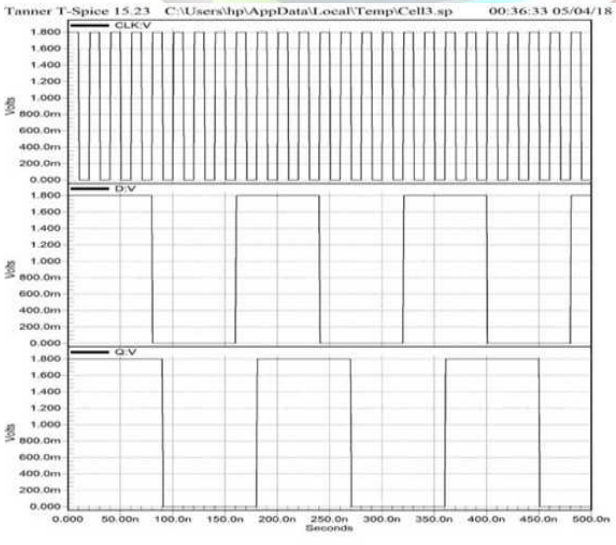

Fig. 11. Output waveform of proposed method

V. CONCLUSION

In this paper, the inverter pairs are designed using leakage power reduction technique known as sleepy stack technique. The static CMOS inverter in conventional DDFF is replaced by sleepy stack inverters. The leakage power and total power for static CMOS inverter and sleepy stack inverter were compared. It is observed that sleepy stack inverter has reduced leakage power to 98% and the total power is reduced to 14.2% as given. Performance of proposed flip-flop has improved in terms of leakage power is 4.98 nW, total power is 49.17 µW and power delay is 3.74 ns at high speed.

Power can be further reduced by using adiabatic logic which utilizes low input as a supply voltage instead of supply. Dynamic families can also be integrated at ease with different flip flops in order to improve the speed of device.

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