Low Power Consumption in CMOS VLSI Design using Modern Trends

S.Sriramsurya

M.E, VLSI-Design, P. A.College of engineering and Technology, Pollachi, India

Abstract: The big revolution of wireless communication, to demanding the mobile (portable)devices designer to design a low power consumption device. Power loss is one of the main parameter of integrated circuits, particularly for portable communication devices. There has been consistent research and development to improve the power consumption and performance of the device in various level of abstraction starting from mask layout - circuit, Gate and Register level - to system level. There are many approaches presentto design low power consumption devices, including hardware and software are identified to design the VLSI Circuit with minimum power consumption and optimization between the power and performance. This paper analyzes the main source of low power consumption CMOS circuit & their impact.

KEY WORDS Static dissipation, Dynamic dissipation, Power-Delay, Portable Devices.

INTRODUCTION

Methods The CMOS power indulgences are static and dynamic. When there is no transition in logic. Dynamic power dissipation occurs when the transition logic is from high to low or low to high. Main source of power indulgence in chip is due to dynamic power indulgence. The dynamic power is dissipated in the form of charging, discharging of capacitance. With advent in semiconductor technology especially in the last few years there has been drastic revolution in the field of information and technology. Tens of million of transistor are fabricated in a single chip. At the same time the complexity in designing, testing and fabricating the chip has also increased. The major worry for the designer now is to optimize the power consumption without degrading the performance. Dynamic power dissipation is addition of P-switching & S-short-circuit.

$$Pswitching = a \ f \ Ceff \ .Vdd^2$$
$$Sshort\text{-}circuit = Isc \ .Vdd.f.$$

We introduce the CMOS inverter and observe the various parameters and their impact in power dissipation.
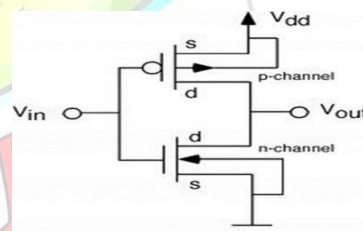

Figure.1. CMOS Inverter

Observation of key parameters and their impact on power and delay for CMOS inverter are purposed below based on simulation.

Clock frequency and its impact on power dissipation The fundamental dynamic power dissipation is P= αCV2F shows that the power dissipation depends on load capacitance clock frequency and supply voltage. An experimental setup fig (2) to show a linear relation between clock frequency and the power consumption is carried out. We verify this here by simulating the inverter over a frequency range (0.5 GHz, 1GHz, and 1.5 GHz). A capacitor of 10fF is used as a load.

The observation is shown in the figure 3.as the clock frequency increases so does the power consumption. This shows the linear dependency of clock frequency and the power consumption. To have a better performance of device it is necessary to increase the clock frequency especially for high speed device but in the mean time optimization is sought for low power consumption.
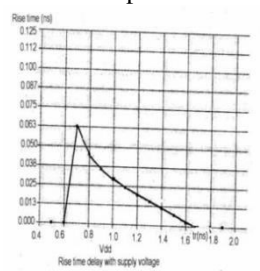

Figure.2. Clock Vs Power consumption

Load capacitance and its impact on power dissipation To obtain the effect of output capacitance and delay of cmos inverter a layout is drawn based on .12 micron cmos technology with a inverter connected with single inverter and with four inverters as shown in figure 4.
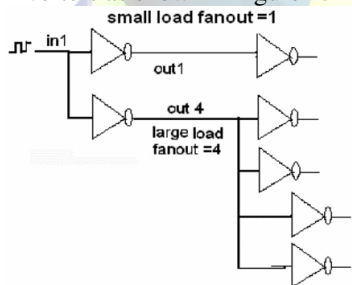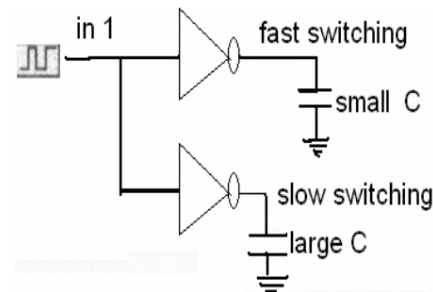

Figure.3. Inverter Connected with another Inverter of Fanout 1 and Fanout 4

The inverter with small load capacitance (fanout=1) has fast switching and with large output capacitance (fanout=4) has slow switching characteristics. This observation is made true by simulating the inverter with different load capacitance and deriving the rise and fall time. The average of rise and fall time gives the switching time.
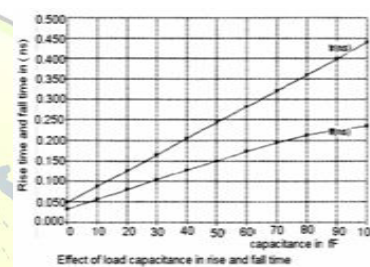

Figure,4,FanIn/OutSwitching

Figure.5.Graphical representation of fan In and Fan OUT

The figure 6 shows that as the load capacitance is increased rise and fall time also increase. Supply voltage and its impact on power dissipation: The equation $P=\_CV2F$ suggest that there is a quadrature effect of supply voltage in power dissipation as it is proportional to square of the supply voltage. A first order approximation shows that the power consumption is proportional to Vdd2 .The experiment is conducted by using the supply voltage from 0.5v to 2V with supply voltage increment step as 0.1V.the graph plotted below shows that the square law is valid 0.8v to 1.5v .there is a very rise in power consumption after 1.5v due to the avalanche effect in n channel MOS device. It is necessary to figure out the optimization between the supply voltage and the performance of the device. For this delay dependency in supply voltage is shown in figure 8.
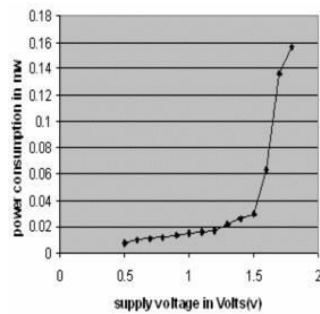
Figure.6. Increase in Power Consumption with Vdd

The delay significantly increases as the supply voltage is scaled from 1.6 v .eventually after 0.7v the delay is such a high the simulator does not evaluate and device does not work.
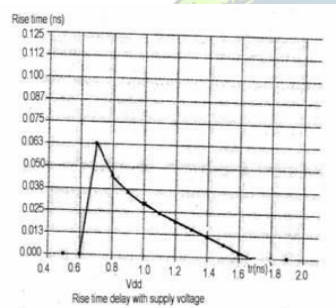

Figure.7. Rise time delay with supply voltages

CONCLUSION

The paper has revisited the major dynamic power dissipation components and studied the impact on cmos inverter hence it gives a better idea to optimize the power and performance of the design. The result and plots were obtained by simulation.

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