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FPGA DATA ACQUISITION SYSTEM IN ETHERNET COMMUNICATION LINKS

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ABSTRACT

FPGA technology combines theflexibility in implementing the interface to the detectors, high data throughput and access to external memory. The FPGA-based data acquisition system of the COMPASS experiment offers a complete event building in the FPGA firmware that consists of data readouts multiplexer modules and a switch module. The system thus includes front-end cores, the FPGA-based event builder core and L1 trigger generation cores. The front-end interface is represented by a TDC core and an interface to the external ADC. The front-end modules perform digitization of the incoming detector signal. The data concentrator modules collect data from the front-ends, combine them into an event and send the events to the FPGA Data Acquisition system. The trigger generator is used in parallel to the data concentrator. It collects data from the front-ends and uses the information to generate a trigger signal. The detectors send data over S links. The links with the low data rate are multiplexed in the S-Link multiplexer before the event builder. The event building is done in two stages, S-Links which are the multiplexer modules and multiplexed data streams are then sent to a switch module where the final events are built in FPGA firmware and distributed to readout PCs over S-Links. The multiplexer and the switch modules are connected to the COMPASS trigger and timing system which plays an important role in the error recovery of the datachain.

I.INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as small- scale integration (SSI), improvements in techniqueled to devices withhundreds of logic gates, known asmedium-scale integration (MSI).

Data acquisition is the sampling of continuous real world information to generate data that can be manipulated by a computer. Acquired data can be displayed, analyzed, and stored on a computer. A PC can be used to provide data acquisition of real world information such as voltage, current, temperature, pressure, or sound. The components of data acquisition systems include appropriate sensors, filters, signal conditioning, data acquisition devices, and application software. Ultimately data analysis can only be as good as the input data, so acquisition is responsible for providing high-quality data.
The components of data acquisition systems include:

- Sensors, to convert physical parameters to electricalsignals.
- Signal conditioning circuitry, to convert sensor signals into a form that can be converted to digital values.
- Analog-to-digital converters, to convert conditioned sensor signals to digitalvalues.

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II. EXISTINGSYSTEM

The system has been built for COMPASS (Common Muon and Proton Apparatus for Structure and Spectroscopy) in hardware equipment based processed, and a fixed target experiment at CERN's SPS. These modules are similar in functionality, however, specific to the attached type of front-end electronics. All front-end cards are readout via one of these two modules. The readout modules retransmit the trigger to the frontends and store the event identifier information in the buffer until the corresponding data arrive from the front-ends. The readout modules combine the data from all attached front-ends in one block and send this block together with the event identifier to the readout buffers (ROB) via Slink interface. The ROBs buffer the data arriving during the 3 second spill and send them via Gigabit Ethernet and a high speed network switch to the event builders which combine all data to a complete eventblock.

III. PROPOSEDSYSTEM

The new FPGA-based data acquisition system of the COMPASS experiment offers a complete event building in the FPGA firmware in contrast to the old system which used a server farm and switched 1 Gb/s Ethernet network. In our proposed system, the framework supports Xilinx FPGA and provides a collection of IP cores written in VHDL which use the common interconnect interface. The IP core library offers functionality required for the development of the full DAQ chain. The library consists of TDC channels, an interface to a multi-channel 80 MS/s 10-bit ADC, data transmission and synchronization protocol between FPGAs, event builder and slow control. The functionality is distributed among FPGA modules built in the AMC form factor: front-end and data concentrator as shown in Figure1.

A. BlockDiagram

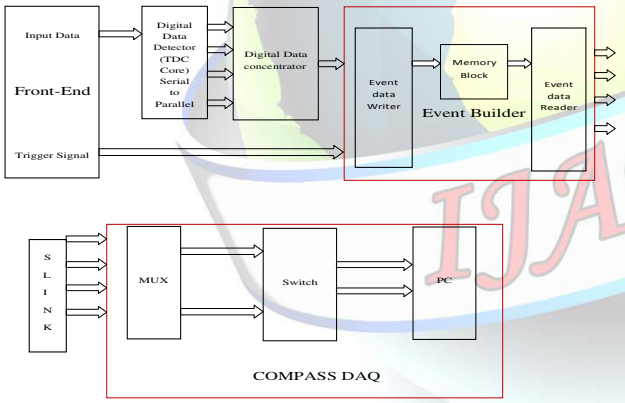

Figure 1 Block Diagram FPGA-Based Data Acquisition System

B. Block DiagramDescription

FRONT END
TDC Core

The front-end interface is represented by a TDC core and an interface to the external ADC. The front- end modules are connected to the detector and can perform digitization of the incoming signal or simply receive digitized data. The difference in the signal propagation time to the TDC core is compensated by calibrating the delay in the Readout Module. Data acquisition systems in high energy physics show similar architecture. Many systems use FPGA technology which combines the flexibility in implementing the interface to the detectors, high data throughput and access to external memory. These are necessaryfeatures

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which make FPGAs a perfect tool in designing data acquisition systems.

ADC

In electronics, an analog-to-digital converter (ADC, A/D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal. An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. Typically the digital output is a two's complement binary number that is proportional to the input, but there are other possibilities. There are several ADC architectures. Due to the complexity and the need for precisely matched components, all but the most specialized ADCs are implemented as integrated circuits(ICs).

Data Concentrator

In telecommunication, the term concentrator has the following meanings: In data transmission, a functional unit that permits a common path to handle more data sources than there is channels currently available within the path. A concentrator usually provides communication capability between many low-speed, usually asynchronous channels and one or more high-speed, usually synchronous channels.

Trigger Generator

Since the digitized data has a timestamp, it can be processed to generate trigger signals. The data processing is done using logical AND, OR and VETO cores. The cores work with the delayed time reference and generate a decision with a fixed latency. The delayed time reference is a counter which runs with the same frequency as the front-end clock, but is delayed to account for the data propagation time to the counter. The cores have 2 data inputs, an input for a configurable coincidence time window and an output. The cores can be chained in several stages if more than two inputs are used. The trigger generator is used in parallel to the data concentrator. It collects data from the front-ends and uses the information to generate a trigger signal.

Memory Write/Read Operation

The event building algorithm has been successfully used in the DAQ of the COMPASS experiment. The algorithm which is shown in the below Figure 2 is designed around external memory. The access to the memory is managed by the core by Xilinx. The memory is divided into banks by the number of the outgoing links. The banks are sub-divided into slots which have a size of the largest possible event and are reserved for single events. The first step upon receiving data from the front-ends is a consistency check of the data format. The frames with errors in the data format are discarded and replaced with dummy frames. Theirpurpose is to preserve the event structure. The data are then passed to the data writer cores. The first data writer

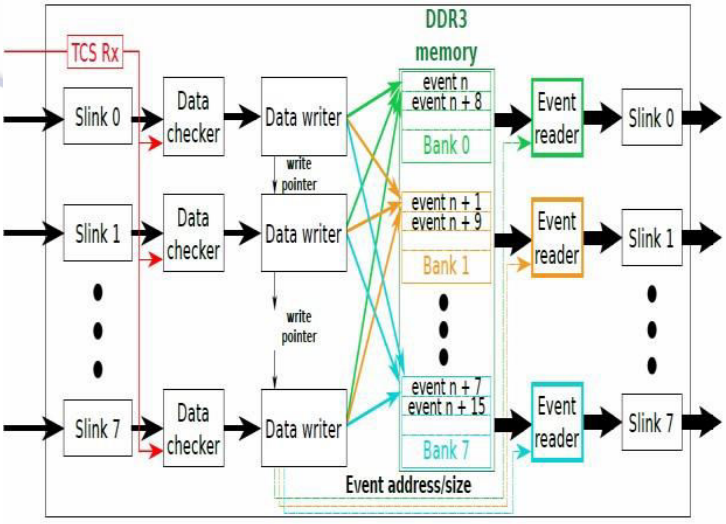

Figure 2 Memory Write/Read Operation determines the next bank and writes the event into the new slot. After completing the event it sends the memory pointer to the next writer and becomes ready to accept the new event. When the last writer writes the event to the memory, the pointer to the event together with the event size is transmitted to the corresponding memory reader. The reader core then reads the full event from

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the memory and sends it to the outgoing link.

IV. RESULTS ANDDISCUSSION

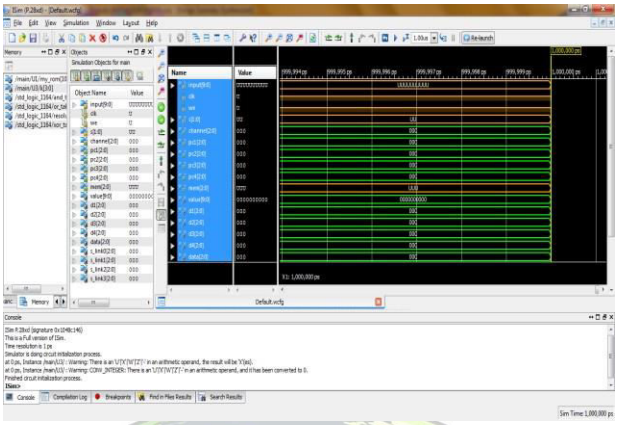

Figure 3 ADC in undefined Input values

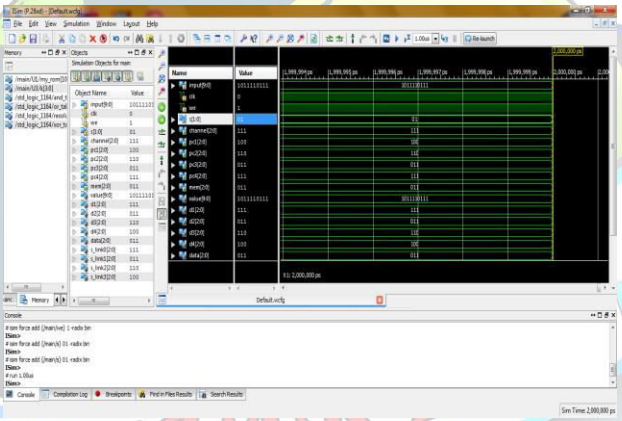

Figure 4 ADC after defined Input values

SYNTHESIS RESULT OF THE SYSTEM

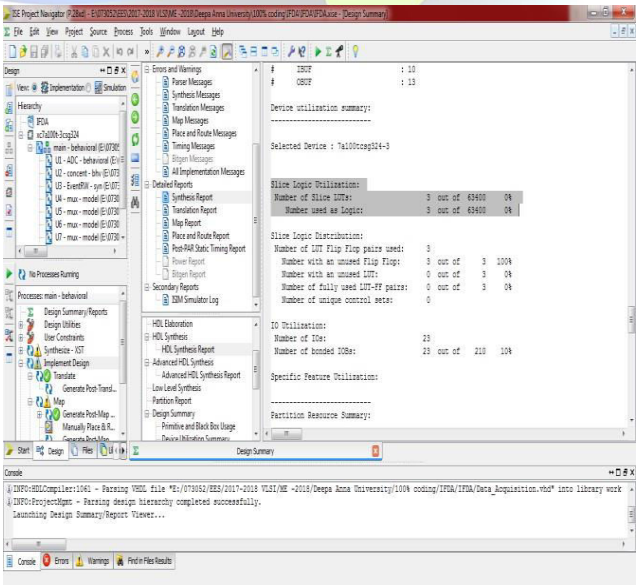

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Figure 5 Area Analysis

The Area analysis of the system is shown in above Figure 5. This analysis mainly concentrated on the total number of slice registers in the entire system. The number of slice registers are used to obtain the output. Hence, the available numbers of slice registers are 63,400 and the used numbers of slice registers are 3.

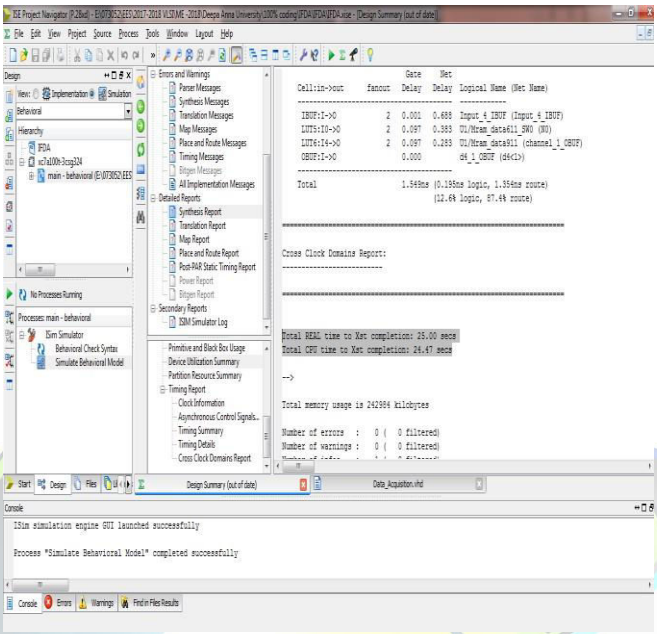

Figure 6 Speed Analysis

The Speed analysis of the system is shown in the above Figure 6. This analysis mainly depends on the total CPU time. Hence, the total CPU time used to generate the output is 24.47 secs.

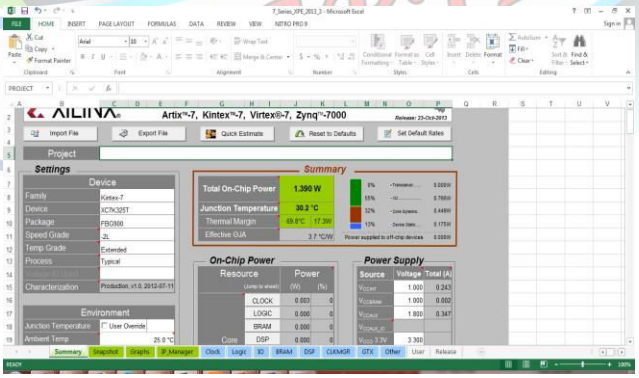

Figure 7 Power Analysis

The Power analysis of the system is shown in above Figure 7. This analysis mainly concentrated on the number IOs in the entire system to obtain the output. In the entire system, the available numbers of IOsare240andtheIOsusedtoobtaintheoutputare
234. The total available power in the system is 1.390W and hence the utilization of power is 1.137 mW.

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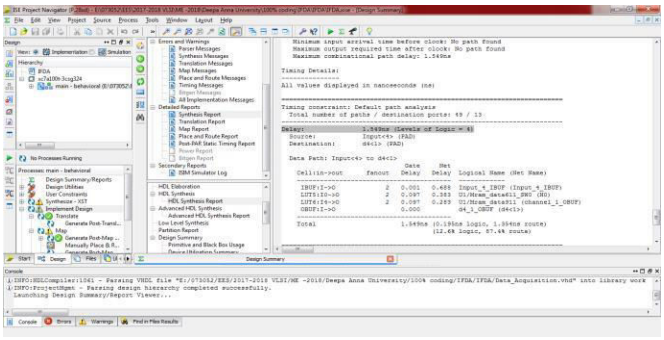

Figure 8 Delay Analysis

The Delay analysis of the system is shown in above Figure 8. The Main concentration of delay analysis is based on the time taken to obtain the output from the time of applying input. Hence, the delay time is 1.549ns.

Table 1 Performance Analysis Comparison table

	AREA (No'S)	SPEED (sec)	POWER CONSUMPTION (mW)	DELAY (ns)
Proposed System	3	25	1.390	1.549ns
Existing System	30	32	4.73	Proto - type based

V. CONCLUSION

The FPGA-based 10-bit data acquisition system of the COMPASS experiment offers a complete event building in the FPGA firmware that consists of data readouts multiplexer modules and a switch module processed using simulation Xilinx software. The multiplexer and the switch modules are connected to the COMPASS trigger and timing system. In the process ADC converted in TDC level. The timing and trigger distribution link used during the beam test recovers the clock phase of the data source are checked. We had compared existing system hardware equipment's and simulation LUT, Speed and Delay with optimized in our proposed work.

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