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COMPLEMENTARY METAL OXIDE SEMICONDUCTOR BASED CURRENT MODE THRESHOLD LOGIC GATE DESIGNS

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ABSTRACT

This process presents a new implementation of current mode threshold functions for improved gate delay and switching energy. An analytical method is also proposed in order to identify quickly the sensor size that minimizes the gate delay. Simulation results on different gates implemented using the optimum sensor size indicates that the proposed current mode implementation method outperforms consistently the existing implementations in delay as well as switching energy. Logical processing in TLGs is more sophisticated than the traditional Boolean gates, and TLGs can implement complex logic functions. A basic TLG consists of N-inputs, a weight value for each input, and a threshold weight. The sum of the input weights is compared with the threshold weight. This process fully implemented in 25nm CMOS technology for future chip integration process.

I.INTRODUCTION

Complementary Metal Oxide Semiconductor abbreviated as CMOS, is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. In 1963, while working for Fairchild Semiconductor, Frank Wan lass patented CMOS (US patent 3,356,858).CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS).

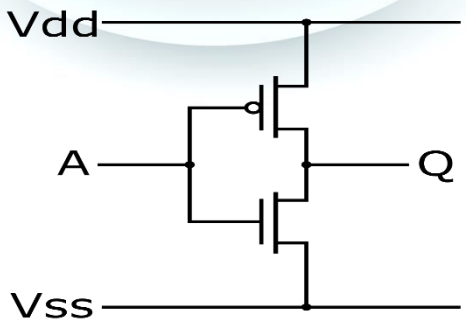

Figure 1 CMOS Inverter

he words "complementary-symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

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PMOS and NMOS

PMOS and NMOS interface CMOS inverter. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or N-type metal-oxide-semiconductor logic (NMOS) logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in Very-large-scale integration (VLSI) chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-κ dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.

Technical Details of CMOS Design

"CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes. As of 2010, CPUs with the best performance per watt each year have been CMOS static logic since 1976. CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistor (MOSFETs) to implement logic gates and other digital circuits. Although CMOS logic can be implemented with discrete devices for demonstrations, commercial CMOS products are integrated circuits composed of up to billions of transistors of both types, on a rectangular piece of silicon of between 10 and 400 mm. CMOS always uses all enhancement-mode MOSFETs (in other words, a zero gate-to-source voltage turns the transistor off).

II. EXISTING SYSTEM

Dynamic Resistive Threshold-Logic (DRTL) design based on non-volatile resistive memory DRTL employs resistive memory elements to implement the weights and the thresholds, while a compact dynamic CMOS latch is used for the comparison operation. The resulting DRTL gate acts as a low-power, configureurable dynamic logic unit and can be used to build fully pipelined, high-performance programmable computing blocks. Multiple stages in such a DRTL design can be connected using energy-efficient low swing programmable interconnect networks based on resistive switches. Owing to memory-based compact logic and interconnect design and high speed dynamic-pipelined operation, DRTL can achieve more than two orders of magnitude improvement in energy-delay product as compared to look-up table based CMOS FPGA.

Dynamic Resistive Threshold Logic (DRTL) employs resistive memory elements to implement the weights and the thresholds, while a compact dynamic CMOS latch is used for the comparison operation. This TLG becomes very difficult to analyze when there is many consideration errors (because more number of inputs). An analytical method is also proposed in order to identify quickly the sensor size that minimizes the gate delay. Simulation results on different gates implemented using the optimum sensor size indicates that the proposed current mode implementation method outperforms consistently the existing implementations in delay as well as switching energy

III. PROPOSED SYSTEM

In proposed system, the threshold logic can be performing based on the weight of the input and threshold weight. In this process we are proposed the low power and high switching energy Current Mode Threshold Logic Gate (CMTLG) and Differential Current Mode Threshold Logic (DCMTL).

A basic TLG consists of N-inputs, a weight value for each input, and a threshold weight. The sum of the input weights is compared with the threshold weight. This process considers implementations of threshold logic functions using current mode. This is a popular CMOS-based approach.

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A. Block Diagram

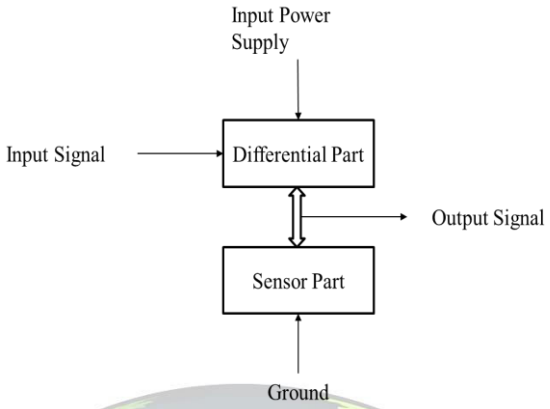

Figure 2 Block Diagram of TLG

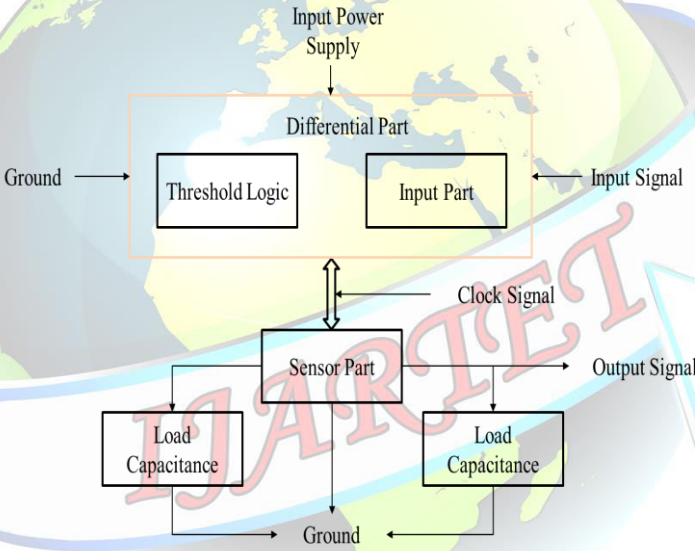

Figure 3 Flow Diagram of TLG

The inputs part has PMOS transistors that implement the positive input weights. The threshold part has PMOS transistors that implement the threshold weight and the negative input weights. Typically, a weight of value x is implemented by connecting x minimum size PMOS transistors in parallel. (Alternatively, it can be implemented by a single PMOS transistor whose width is x times the minimum size.)In both the parts, all the PMOS transistors are connected in parallel. The total current flowing through the threshold part is denoted by IT. The total current passing through the inputs part is denoted by IA. For each applied input pattern, PMOS active (ON) transistors correspond to input weights for inputs that are assigned a logic value 1.

The new implementation, which we call the dual clock current mode logic (DCCML), which results in both speed and switching energy [power-delay product (PDP)] improvements over the approaches. They consist of two parts: the differential part and the sensor part. All the PMOS transistors in the sensor part have the same size S, which we call the sensor size. The sensor size impacts the performance of all the three current mode implementations for any threshold logic function. It is a very time-consuming task to obtain the optimum sensor size through iterative SPICE simulations, one simulation for a different sensor size. A new TLG implementation is proposed. It is called DCCML. As the name indicates, two clocks are used to achieve low power consumption and high speed. As in previous approaches, the DCCML is divided into two basic blocks: the differential block and the sensor block.

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The differential block is further divided into four blocks: the positive threshold, the negative inputs, the negative threshold, and the positive inputs. All the transistors in the differential block are equal-sized PMOS transistors and are connected in parallel, as shown in Figure 3 The sensor block consists of six PMOS transistorsP1 · · · P6 and three NMOS transistors N1 , N2, and N3. The gates of transistors P1 and N1 are connected to Clk1 and the gates of transistors P2, P5, and P6 are connected to Clk2. Transistor N1 acts as an equalizing transistor and it equalizes the voltage at nodes OP and OPB. Transistors P5 and P6 isolate the differential block from the sensor block. The transistors in the positive threshold and negative threshold are always active. Transistors in the positive and negative inputs blocks are active depending upon the input pattern applied.

B. BEHAVIOR OF Threshold Logic Gate (TLG)

- Logical processing in TLGs is more sophisticated than the traditional Boolean gates, and TLGs can implement complex logic functions
- In a TLG, weights are the principal elements that define the functionality of a gate.
- A basic TLG consists of N-inputs, a weight value for each input, and a threshold weight.
- The sum of the input weights is compared with the threshold weight.
- The number of transistors in the sensor part is constant and does not depend on the implemented function.
- The number of transistors in the differential part depends on the sum of input weights and the threshold weight.
- The sensor size impacts the performance of all the three current mode implementations for any threshold logic function.

It is a very time-consuming task to obtain the optimum sensor size through iterative SPICE simulations, one simulation for a different sensor size.

C. Current Mode Threshold Logic Gate (CMTLG)

This section presents CMTLG. The block diagram of the CMTLG is shown in Figure 4. It consists of the differential part and the sensor part. The differential part is subdivided into two parts: the threshold part and the (positive) inputs part. The inputs part has PMOS transistors that implement the positive input weights. The threshold part has PMOS transistors that implement the threshold weight and the negative input weights.

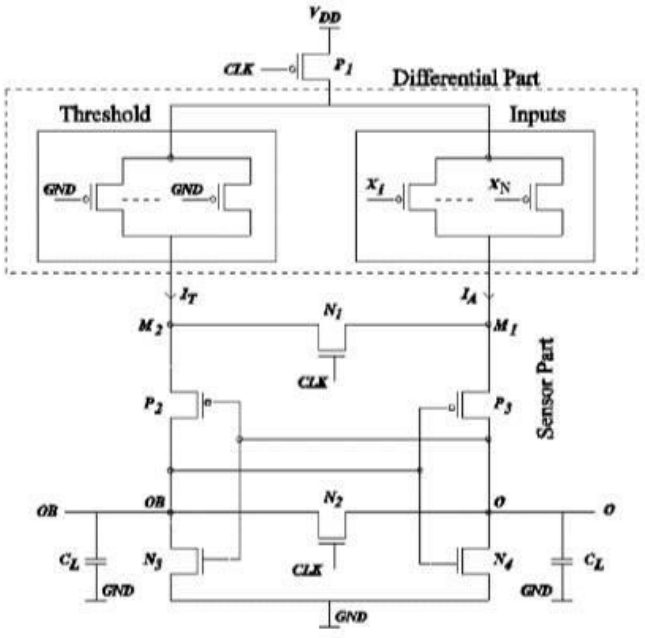

Figure 4 Current Mode TLG circuit

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Typically, a weight of value *x* is implemented by connecting *x* minimum size PMOS transistors in parallel. (Alternatively, it can be implemented by a single PMOS transistor whose width is *x* times the minimum size.) In both the parts, all the PMOS transistors are connected in parallel.

Low-power dissipation is achieved by limiting the voltage swing on the interconnects and the internal nodes of the CMTL gates. High-performance is achieved by the use of transistor configure rations that sense a small difference in cur- rent and set the differential outputs to the correct values. The realization of NAND, NOR, AND, OR logic gates and other logic functions using the CMTL gates is presented. We also present several implementations of CMTL gates and describe the relative advantages and limitations of these implementations.

The a general circuit diagram of the CMTL gates. The low-swing inputs are fed to a PMOS based CMTL gate. The CMTL gate senses the low input swings, performs the logic computations and creates full-swing output voltages. The output nodes of the CMTL gate with full-swing are used as inputs to the NMOS based interconnect driver. In the next section, we describe the current-mode threshold logic gates and present several implementations of threshold logic gates. The simulation results for the realization of different logic functions using CMTL gate, we describe the limitations and other reliability issues. A threshold gate is a super-set of logic gates such as AND, NAND, OR, NOR. It can be used to realize more complicated functions such as majority function in a single logic gate. A detailed description of threshold logic can be found.

D. Differential Current Mode Threshold Logic Gate (DCML)

The bias generation process has the PMOS and NMOS transistor feedback from input voltage reference value and sensing voltage of the class AB stage. The voltage get from the reference voltage as the sensing of the output of the LDO. The bias generation output voltage to regulated cascade amplifier branches. The dashed capacitors at node A and node B, Cp, are the parasitic capacitances at the drain terminals of M1 and M2.

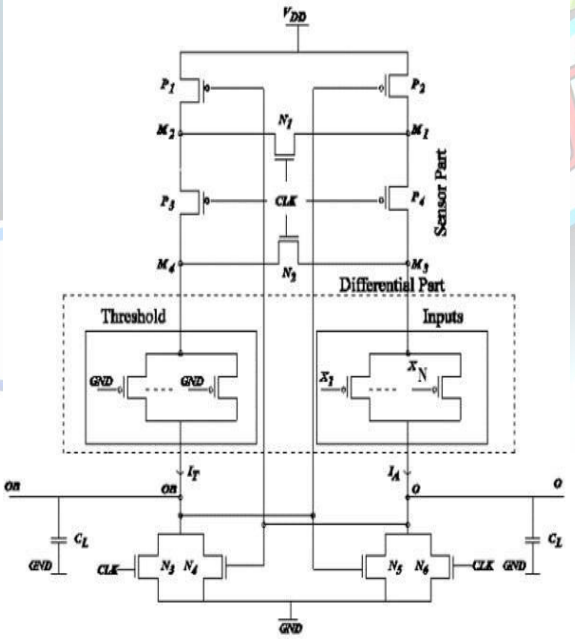

Figure 5 DCML circuit

Multi-stage topologies are usually adopted with carefully designed compensation schemes to ensure circuit stability. The significance of active area junction capacitance for circuits containing small size transistor was shown. The imperfection of analytical delay calculation models was revealed. The only way to correctly predict the delay in circuit containing small size transistors is electrical simulation with the use of full transistor equivalent circuit. All parasitic must be taken into account. Due to small bandwidth and big driver resistance of CMOS circuit's on-chip interconnections can be modeled as RC distributed lines.Another effect of low driver impedance is that the relaxation time, the time required for a signal to reach the steady state voltage of the coupling noise voltage on the quiet line, increases.

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IV. RESULTS AND DISCUSSION

In this section, describe results of about the proposed Current mode and Differential mode of TLG.

SIMULATED RESULT OF CURRENT MODE AND DIFFERENTIAL MODE TLG

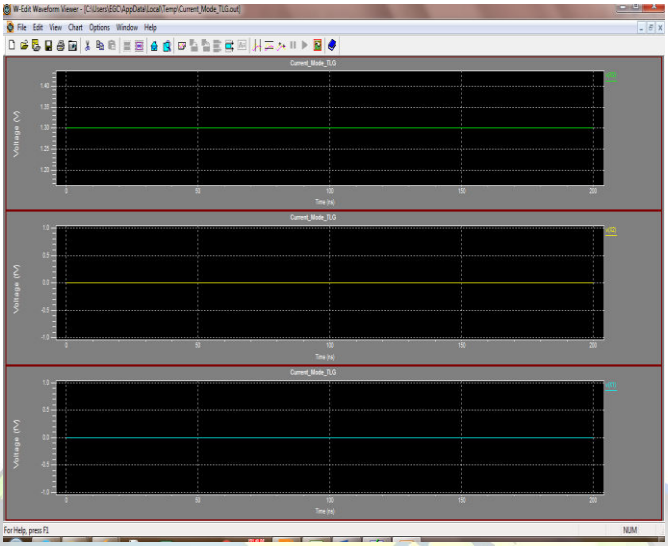

Figure 6 Input of Current Mode and Differential Mode TLG

The input for the current mode TLG and differential mode TLG is shown in the Figure 6. In which $v(x_1)$, $v(x_2)$, $v(x_3)$ are the input weights and v_{DD} is the drain voltage which is setted as 1.3V in this case v (clk) is the clock pulse given to the circuit v(out) is the output voltage that we obtain after stimulating the designed circuit.

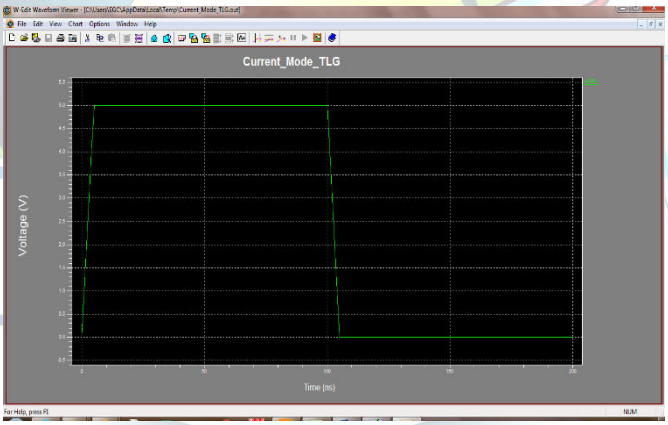

Figure 7 Clock Input

The clock input is shown in Figure 7 which operates the transistor according the clock pulse inputted to the circuit. This also denotes the ON and OFF state of the transistor this produces the output accordingly.

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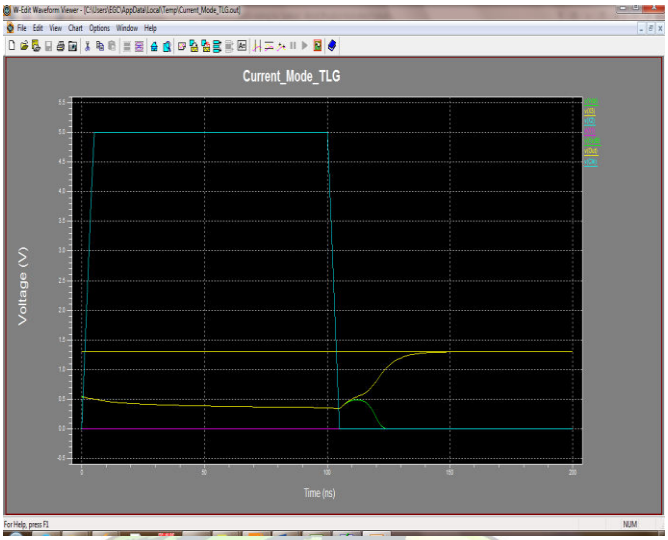

Figure 8 Current Mode TLG

The operation of the CMTLG is divided into two phases: the equalization phase and the evaluation phase. These phases are explained with the help of Figure 8 When the applied clock to the CMTLG is high, and then the circuit is in the equalization phase. When cl k is low, then the circuit is in the evaluation phase. In the equalization phase, transistors N_1 and N_2 are ON, nodes M_1 and M_2 have the same voltage because of transistor N_1, and nodes O and $O\ B$ have the same voltage because of transistor N_2. In the evaluation phase, transistors N_1 and N_2 are OFF, and if the threshold current is less than the active current, then the voltage at node O rises faster than that at node $O\ B$. If during the evaluation phase the threshold current exceeds the active current, then the voltage at node $O\ B$ rises faster than that at node O.

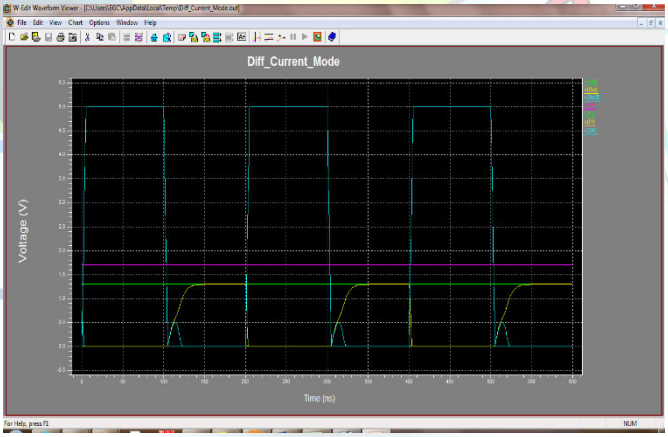

Figure 9 Differential Current Mode TLG

The differential current mode logic (DCML) approach. It is shown in Figure 9. It is also divided into the differential part and the sensor part. The currents through the threshold part and the inputs part are also denoted by I_T and I respectively. The sensor part consists of four PMOS transistors, labeled P_1–P_4, and six NMOS transistors, labeled N_1–N_6. The load capacitance CL is applied to both the output nodes O and OB.

SYNTHESIS RESULT OF DEVICE UTILIZATION

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Figure 10 Device Utilization Current Mode

The above Figure 10 depicts the device utilization in current mode, in this device and the node counts are shown. These details will be helpful for us to view the technology implemented in CMOS.

Figure 11 Device Utilization Differential Mode

The above Figure 11 depicts the device utilization in differential mode, in this device and the node counts are shown. These details will be helpful for us to view the technology implemented in CMOS.

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Figure 12 Program Speed in Current Mode

The above Figure 12 depicts the program speed in current mode; in this non graphical data of the operating time of the simulation are shown. These details will be helpful for us to view the total speed of the program in current mode

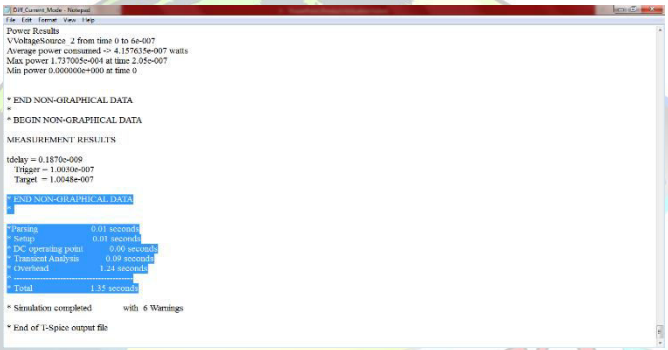

Figure 13 Program Speed in Differential Mode

The above Figure 13 depicts the program speed in differential mode; in this non graphical data of the operating time of the simulation are shown. These details will be helpful for us to view the total speed of the program in differential mode

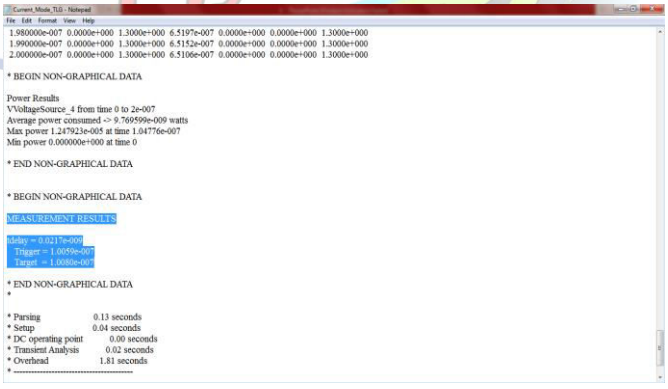

Figure 14 Power and Delay in Current Mode

The above Figure 14 depicts the power and delay in current mode; in this power results are shown. Where we can obtain the details of average power consumed and the delay after the simulation process.

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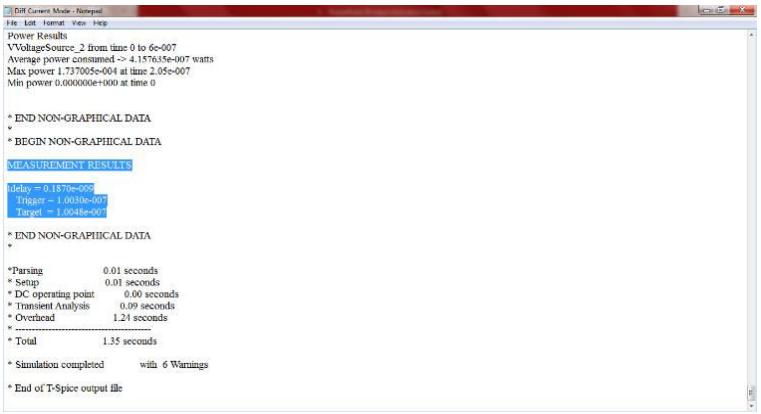

Figure 15 Power and Delay in Differential Mode

The above Figure 15 depicts the power and delay in differential mode; in this power results are shown. Where we can obtain the details of average power consumed and the delay after the simulation process.

Table 1 Performance Analysis Comparison table

METHODS	(N,T)	POWER CONSUMPTION (µW)	DELAY (ps)
Existing Method	8,5	10.124e-6	297
Proposed Method	8,5	9.764e-6	217

V.CONCLUSION

An analytical method has been proposed to identify quickly the transistor size in the sensor component of a current mode implementation that ensures very low gate delay (very close to the minimum), independent of the current mode method used to implement the threshold logic function. A new current mode implementation method was also proposed that outperforms existing implementations both in gate delay as well as energy.

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