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FPGA Implementation and Testing of I^2C Bus Protocol for Interfacing EEPROM

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***Abstract*-During early 1980's, Philips Semiconductors invented a serial bus interface, Inter-Integrated Circuit, commonly called as I^2C, to enable faster devices to communicate efficiently with slower devices without any data loss [1]. Two active wires Serial Data line (SDA) and Serial Clock Line (SCL) are used for this serial communication. In this paper, I^2C master bus was designed in Verilog using the concept of Finite state machine (FSM).The design is simulated and synthesized using Xilinx 14.2 ISE. The hardware implementation of the I^2C master is done using Spartan 6 FPGA. Here, EEPROM AT24C512 is used as a slave for writing operation. The LGLite ATE controller is used to read the stored data from the EEPROM and the I^2C protocol is verified using the Logic Analyzer.**

***Keywords*—Serial Data Line (SDA), Serial Clock Line (SCL), EEPROM, Spartan 6 FPGA, Finite State Machine, LGLite ATE Controller, Logic Analyzer.**

I. INTRODUCTION

Development of technology is determined based on efficient communication either between device to device or within the same device. Serial Communication is widely used everywhere because it is very cheap and best way for transferring data while parallel communication requires more data lines and synchronizations, which are very difficult to achieve. In order to achieve efficient serial communication, there are some protocols such as SPI, I^2C, DC-BUS, UNI/O and 1-Wire. They use multiplexing of the data channel and forwarding of messages to service multiple devices [2]. In order to overcome this problem,Philips Semiconductors introduced I^2C protocol, which requires only two lines for establishing communication with two or more chips and can control a network of device chips with just a two general purpose I/O pins [3], whereas other bus protocols require more pins and signals to connect devices.

A. Inter-Integrated Circuit (I^2C)

I^2C is a simple protocol for serial communication which consists of two lines Serial Data Line (SDA) and Serial Clock Line (SCL). This I^2C bus is simple to interface, has easier operation, which more and more engineers designers [4]. The advantage of I^2C is detection of error during recessive bits are transmitted [5]. The I^2C bus functions at three different speeds, minimum of under 100Kbps, maximum of at 3.4Mbps but usually at 400Kbps. This protocol is applicable for volume control in intelligent speakers, RTC and NVRAM chip access, reading hardware monitors, Data acquisition from diagnostic sensors and so on.

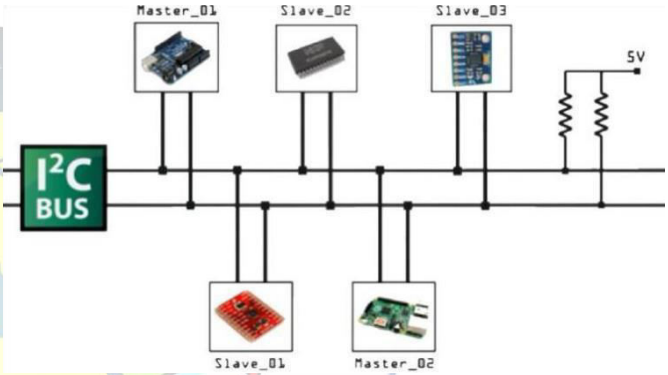

Fig. 1 Basic I^2C bus protocol application diagram

The I^2C can have both master and slave devices and that is illustrated in Fig 1. The master device generates clock and initiates the serial communication using start condition. Master sends the address of the slave to communicate with it. The slave device listens to the master and replies with an acknowledgement to indicate its presence. Once the acknowledgement is received, the master starts to send the data to the slave. The slave acknowledges the master on successfully receiving the data. Further, the master ends the serial communication using the stop condition. For, both start and stop conditions SCL has to be high and SDA changes from high to low means it is considered as start and the low to high transition of SDA is considered as stop.

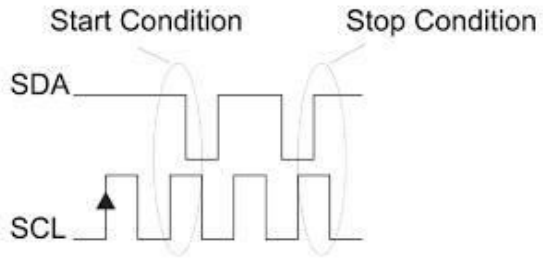

Fig. 2 Start and Stop conditions of I^2C bus protocol

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B. FPGA Spartan 6

Spartan 6 LX45 FPGA with 100 mbps Ethernet, 128 MB DDR2 memory, 4.3" LED backlit LCD touch screen, 2 MB SRAM makes an ideal platform for FPGA learning station. The Anvyl Board of Spartan 6 is shown in Fig 3.

Fig. 3 Spartan 6 LX45 FPGA – Anvyl Board

Additional to that, it consists of breadboard with 10 digital IO's, Keypad with 16 labeled keys (0-F), GPIO:14 LED's,8 Slide switches,8 DIP switches and four push buttons and seven 12-pin PMOD connectors with 56 IO's. Each 12 PMOD ports provide two 3.3 Vcc signals (pins 6 and 12), two Ground signals (pins 5 and 11) and eight logic signals as shown in Fig 4. Vcc and Ground pins can deliver upto 1 A of current.

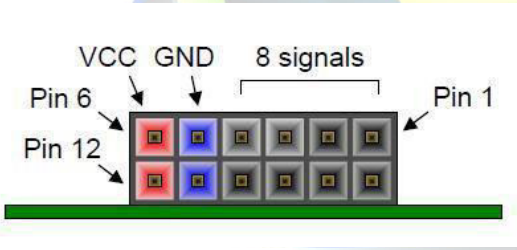

Fig. 4 Pmod ports – front view as loaded on PCB.

C. LG Lite Automatic Test Equipment (ATE)

LG Lite 32 channels are new generation three in one product which consists of pattern generator, logic analyzer and frequency counter. It is designed as PC hosted instrument and an ideal tool for learning fundamentals of Digital In-Circuit testing and test program development. The combination of Load board and Controller makes to perform the testing of Device under Test the set up is illustrated in Figure 5.

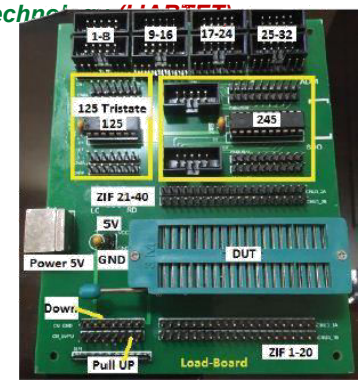

Fig. 5 LG Lite ATE Loadboard

D. EEPROM (AT24C512)

EEPROM AT24C512 provides 524,288 bits of erasable and programmable memory organized as 65,536 words of 8 bit each. This device is optimized and used in many industrial and commercial applications where low power is essential to operate it. It follows bidirectional data transfer protocol. The pin diagram is displayed in figure 6 which consist of 8 pin.

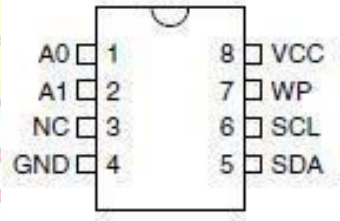

Fig. 6 AT24C512 pin diagram

First 512K EEPROM requires 8-bit device address to enable the chip for write or read operation. The eighth bit of the device address represents the selection bit for read or writes. For read it is set as high and for write it is set as low. Once the acknowledgement is received, the chip needs first word address followed by reception of acknowledgement. Then second word address is needed which ends with last acknowledgement. Only after this, the data can be written on EEPROM which throws the acknowledgement and ends with stop condition which is shown in Fig 7.

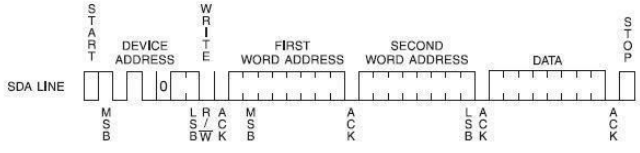

Fig. 7 AT24C512 byte write timing diagram

To read the data written in the chip the corresponding address have to be written with last bit as high, once the acknowledgement is received, the data is read from the

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EEPROM with negative acknowledgement and that is shown in Figure 8.

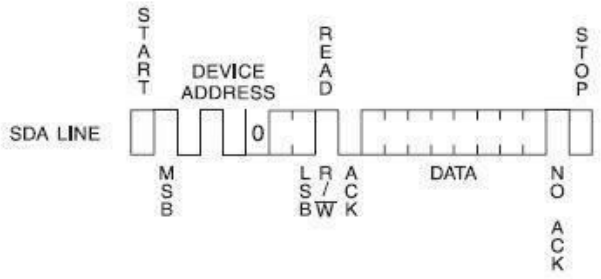

Fig. 8 AT24C512 current address read timing diagram

II. LITERATURE REVIEW

According to the reference paper [2], the authors have implemented the I^2C master in Spartan 3A and the slave used was the DS1307 real time clock module. Further, in the reference paper titled "Prototyping of Dual Master I^2C Bus Controller", the I^2C dual master bus was implemented in Spartan 3A FPGA and the EEPROM and DS1307 real time clock were used as a slave. According to the proposed work of the author mentioned in the reference [5], the master I^2C is implemented in Spartan FPGA 3A and data is written on it. The author of paper mentioned under reference [7], has implemented I^2C bus controller in Virtex 4. According to the reference paper [4] the I^2C bus was implemented in FPGA – SOPC using VHDL language. But, in our proposed work the master I^2C is implemented in Spartan FPGA 6 and the data is written and read operation is performed by LG Lite Automatic Test Equipment.

III. PROPOSED WORK

Our proposed method is categorized into three parts that is implementation, writing and testing. First part is Design and Implementation of Master I^2C Bus protocol using Verilog in Spartan 6 FPGA. Second part is writing the data from Spartan 6 to EEPROM (AT24C512). Then the third part is checking of the written data by reading it using LG Lite Automatic Test Equipment. Our overall proposed is represented diagrammatically in Fig 9.

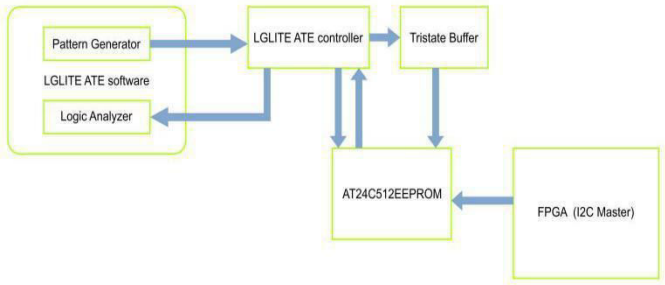

Fig. 9 Overall Block Diagram of Implementation and Testing of AT24C512

The Finite State machine for write operation of EEPROM based on AT24C512 is designed and verified in Xillinx Software using Verilog language. Since EEPROM works efficiently in 400 KHz, the 1MHz clock generated internally in Spartan 6 is divided into 400 KHz in the Verilog program. Serial Clock Line (SCL) and Serial Data Line (SDA) are generated based on the divided clock. The whole design is simulated in Xillinx Software. After that the synthesis process is performed to generate the RTL design schematic which determines the pin configuration for newly designed chip. The ports are assigned for the input and output pins as per the RTL schematic before it is being implemented in Spartan 6. Once the ports are assigned the design is implemented in the Spartan 6 and output, SCL and SDA are verified using Digital Storage Oscilloscope (DSO). The Device under Test EEPROM is placed on the ZIF socket of Loadboard for testing. The EEPROM is provided with corresponding power supply from Loadboard using flying leads. The SCL and SDA from Spartan 6 is fed as input to EEPROM for writing the data. This is how the data is written on EEPROM and in order to test and verify the vector program for read operation is developed in LGC software. In LGC software channel 1 to 8 is assigned for Pattern Generator and channel 9 to 32 is assigned for Logic analyzer. Pattern Generation is used for localization of data by writing device address. Logic Analyzer is used for displaying the output data in the form of waveform. So the bidirectional pin SDA is connected to the corresponding channel by using tristate buffer. Now by running the vector file of read operation, the data which is written by Spartan 6 in EEPROM is read back and viewed in the Logic Analyzer of LGC Software.

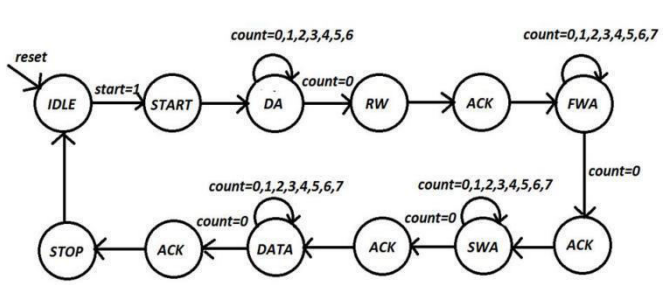

Fig. 10 Finite State Machine for write operation in EEPROM

Figure 10 depicts about Finite State Machine for write operation in EEPROM. When the reset is high, SDA and SCL lines remains in the idle state. When the reset is zero, it enters into start condition and sends the device address of seven bits followed by read/write bit. The slave acknowledges the master to indicate its presence. Then the master sends the first word address of 8 bit to the slave and continues sending the 8 bit second word address, on receiving the acknowledgement. The slave acknowledges the master once the address specified is located. The master sends the 8 bit data on the SDA line. Once the data is written on the

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slave, it acknowledges the master and enters into stop condition and finally reaches the idle state.

IV. RESULT ANALYSIS

A. *Simulation and Synthesis Result*

The Finite State Machine designed using Verilog is verified in the ISE simulator. The SDA and SCL lines are checked for the correct transition based on the address and data inputs. The simulation of Master I^{2}C bus protocol is displayed in figure 11.

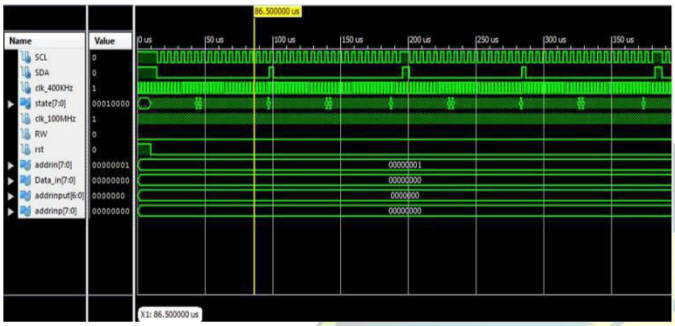

Fig. 10 Master I^{2}C bus protocol simulation result

During synthesis process RTL schematic is generated and newly designed pin configuration is displayed in figure 11.

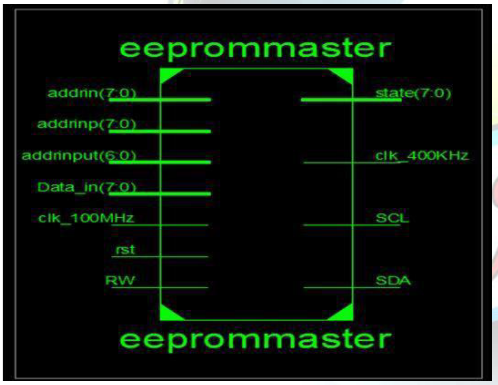

Fig. 11 RTL schematic for Master I^{2}C Bus protocol

B. *Spartan 6 Implementation Result*

The ports in Spartan 6 are configured using PlanAhead Software. The address and data inputs are assigned to the corresponding ports as shown in figure 11.

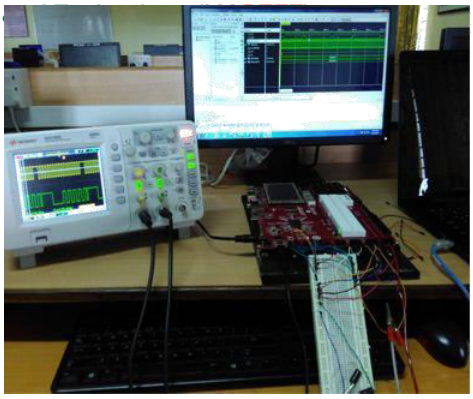

Fig. 11 Master I^{2}C bus protocol implementation set up diagram

The bit file of Verilog program is implemented using iMPACT software. Once the program is successfully implemented,the SCL and SDA lines are captured for verification in Digital Storage Oscilloscope (DSO) as shown in figure 12.

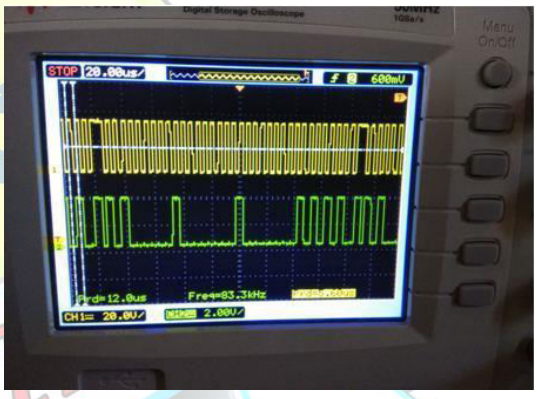

Fig. 12 Master I^{2}C bus protocol DSO verification result

C. *LG Lite ATE Testing Result*

From the Spartan 6 the data is written on EEPROM which is in Loadboard of LG Lite ATE. The overall set up diagram is displayed in figure 13.

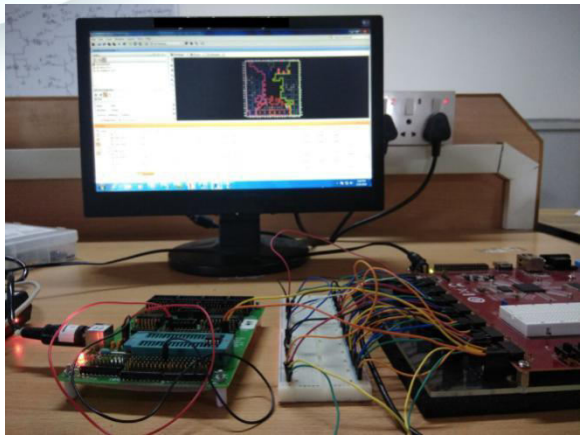

Fig. 13 Data writing to EEPROM from Spartan 6 set up diagram

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The written data in EEPROM is read by LG Lite ATE by LGC software and overall set up is in figure 14.

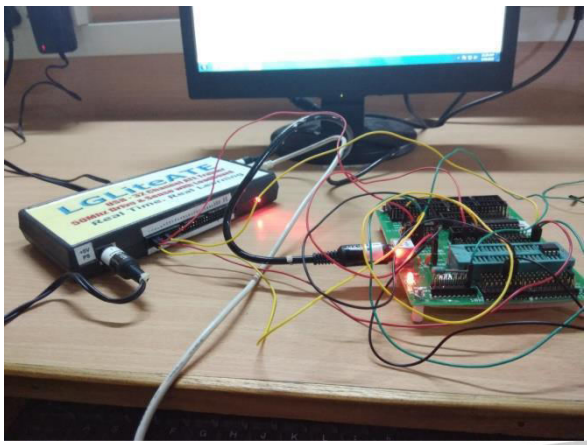

Fig. 14 Data reading from EEPROM by LG Lite ATE set up diagram

The data read from EEPROM by LG Lite ATE is viewed in Logic Analyzer as waveform which is shown in figure 15.

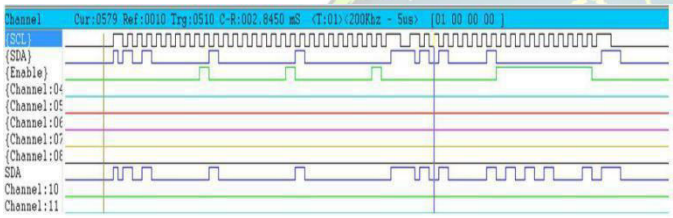

Fig. 15 Displayed data as waveform from Logic Analyzer in LGC Software

V. CONCLUSION

The I^2C master is designed in Verilog HDL based on finite state machine concept. It is then simulated, synthesized and implemented in Spartan 6 FPGA. The slave EEPROM is written with data sent in the SDA line by the I^2C master. Finally the LG Lite ATE controller used to read back the stored data from EEPROM and thus I^2C bus protocol is tested successfully. In our project byte write only is implemented and in future it can be extended to page write also and multi master and multi slave can also be implemented and tested using Automatic Test Equipment (ATE).

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