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Design of High Efficient 4*4 Multiplier using Booth Multiplier Architecture with High Efficient Sleep Transistor Logic in 45nm Technology

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***Abstract*—In this paper, we proposing a new technique for high speed 4*4 multiplier using booth multiplier based on Sleep Transistor Logic with 45nm technology In conventional multiplier area and power requirement is more. To reduce power in multiplier sleep transistor logic is implemented in the circuit to reduce power requirement. Sleep transistor logic is used to eliminate the 80% power dissipation of the circuit during the standby mode and active mode. Partial products of the conventional multiplier is reduced by using booth architecture. An 4 bit x 4 bit multiplier has also been implemented using the design of only using basic combinational circuits and its performance has been analyzed and compared with the similar multiplier available in literature. The proposed method achieves the high speed low power design for the multiplier. Simulated results indicate the superior performance of the proposed technique over conventional CMOS multiplier. Detailed comparison of simulated results for the conventional and present method of implementation is presented. Implementation and analysis is based on 45nm in Tanner EDA tool**

***IndexTerms*—4*4 multiplier,2T Mux,Hybrid adder,Booth architecture.**

I. INTRODUCTION

The assembly of full electronic circuits on a single chip significantly increase performance and reliability as compared the discrete components. Gordon Moore stated that various advancements in integrated circuit (IC) technology in 1965 and the market dynamics was the key reason for the growth semiconductor technology. Since 1970‟s integration density (no. of components) increased by every two or three years, caused increase in speed and technology. Reduction in size (technology scaling) in the key factors on integration density of the circuit.

Multiplication in VLSI systems and DSP architectures beholds itself as the most prominent parameter for determining the speed and designing of multipliers.

As technology has scaled down in nm regime, power dissipation and delay has becomes the major issue of discussion. Scaling down of technology leads to lower the power supply and threshold voltages caused significant growth in leakage power. This forced scientists to adapt new methodology to meet new power constraints

Booth Multiplier additionally reduces partial product to n/2.Booth Multiplier algorithm provides better result as compare to other multiplication algorithm. Wallace multiplication algorithm provide result but slow process in terms of latency or time complexity. Another disadvantage of Wallace

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multiplication algorithm is very irregular design structure so process slow.

Hybrid full adders and half adders are used to add the partial products from the multiplier to reduce delay and power. Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different idea called Sleep Transistor logic.

II. THEORY AND IMPLEMENTATION OF 4*4 MULTIPLIER

A combinational multiplier is a superior model Show casing how simple logic functions (gates, half adders and full adders) can be combined to build a much more complex function. Consider the following example (fig. 1) for binary multiplication of two positive 4-bit integer values. Here, each bit in the multiplier is multiplied with the multiplicand. Each of the four products is aligned (shifted left) according to the position of the bit in the multiplier that is being multiplied with the multiplicand

Here, each bit in the multiplier is multiplied with the multiplicand. Each of the four products is aligned (shifted left) according to the position of the bit in the multiplier that is being multiplied with the multiplicand. The four resulting products are added to form the final result. Therefore for an N×N multiplier, the result is 2N bits wide. With binary numbers, forming the products is much easy. If the multiplier bit is a 1, then the corresponding product is simply an appropriately shifted copy of the multiplicand. If the multiplier bit is a zero, then the product is zero. 1-bit binary multiplication is thus just an AND operation.

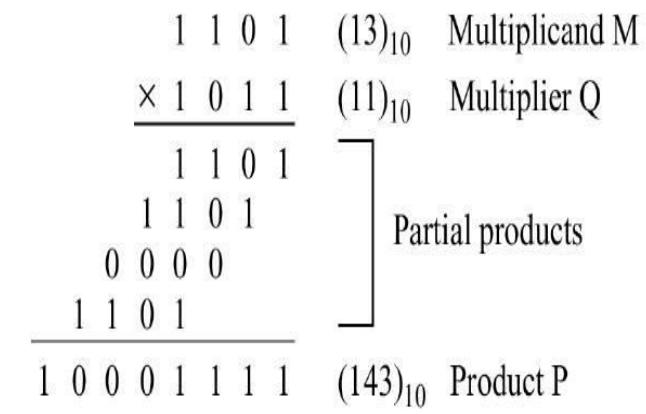

Fig.1. Binary multiplication example (4x4)

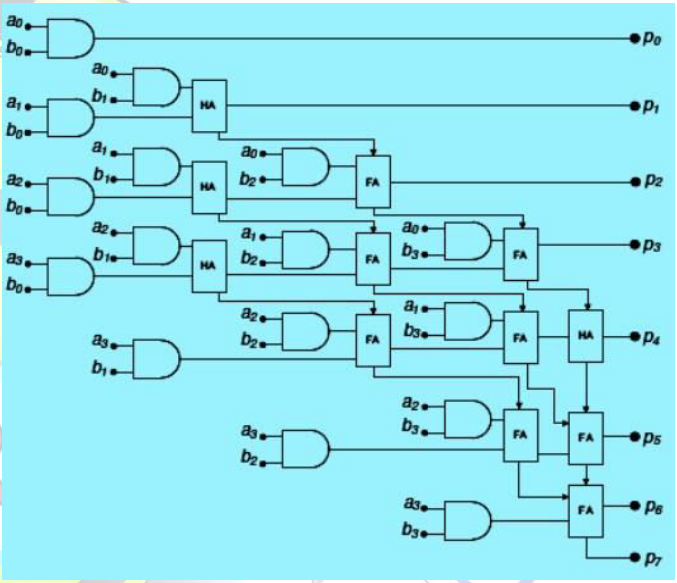

Fig. 2. 4x4 multiplier using AND gate, Half adder and full adder

To design a low power 4x4 multiplier the approach is to design the circuits with minimum nos. of transistors. Here the basic building blocks (half adder, full adder & AND gate) of\ the 4x4 multiplier shown in fig. 2 are constructed with minimum no of transistors

III. IMPLEMENTATION OF 16T HYBRID FULL ADDER

A) CONVENTIONAL FULL ADDER

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The conventional CMOS 28 transistor Full adder, as shown in above Figure 3, is considered as one of the Base case throughout this paper. The circuit is having inputs are a, b, c_{in} and the sum, c_{out} are the outputs of the one bit conventional 28 transistor full adder of 65nm technology

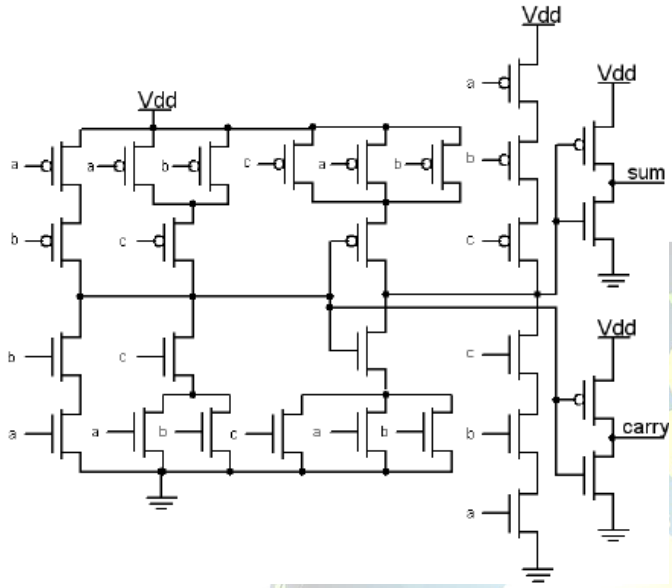

Fig.3 Schematic of Conventional 28T Full adder

B) **HYBRID FULL ADDER**:

Inhybrid adder some of the transistors in the existing are removed and others are interconnected and the overall power and area also reduced.fig4 shows the proposed hybrid full adder using logic gates

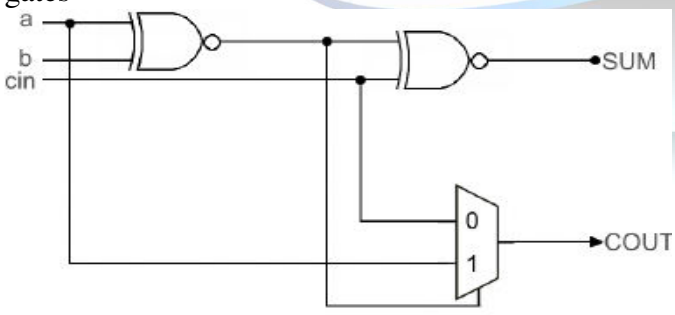

Fig.4.8-T FA based on MUX & XOR gates

The first component required to design a full adder with 8 transistors is XOR gate. Conventional XOR gate can be fabricated using Transmission Gate (TG) logic which needs more than 3 transistors. But here is the design of a XOR gatewith 3 transistors as shown in fig.5 below. The second component required to design a full adder with 2 XOR gate to implement the sum out & another two input MUX to implement the carry out. The basic structure of the 2:1 MUX using pass gate transistor logic and implement sleepy stack technique is shown in fig. 8. In this configuration we have connected PMOS and NMOS along with a SEL line, as in MUX.

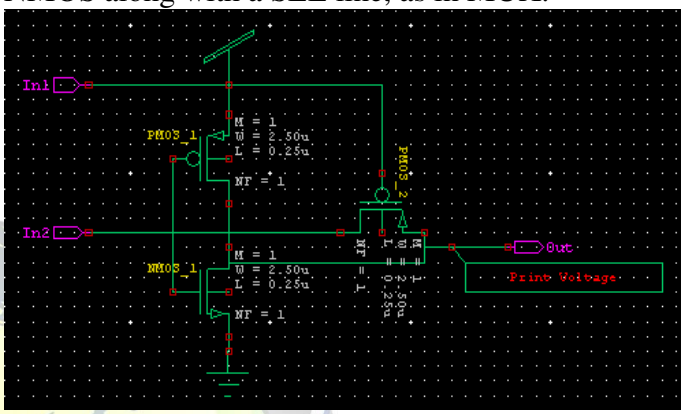

Fig. 5. Basic view of 3T XOR gate

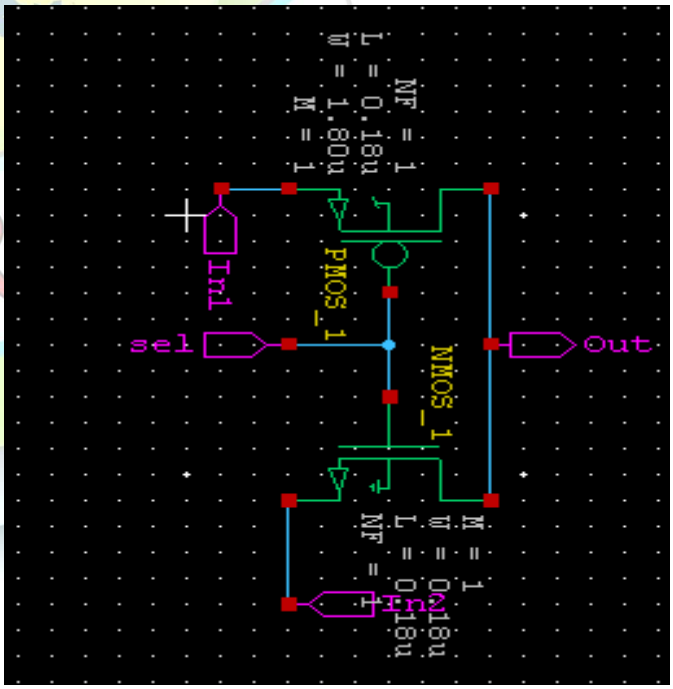

Fig.6. Basic view of 2T MUX

C. **5-T Half Adder (HA)**

As already we have designed 3-T XOR and 2-T AND gate,now one half adder can be easily designed with five nos. oftransistors.

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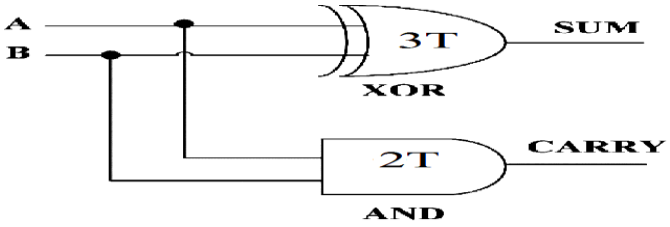

Fig. 7. 5-T HA based 3T XOR & 2T AND

IV. SLEEP TRANSISTOR TECHNIQUE

According to Moore's law, no. of transistors increases by every two year so there is a need to reduce the size of transistor (nanometer regime) as the size reduces power supply and threshold voltage should also be reduced. By lowering the value of threshold there is an exponential increase in leakage power. Due to this power dissipation there is a great effect on battery life of portable devices also leads to overheating, degradation in performance and functionality .In nanometer regime 40% power is dissipated only due to leakage currents. In the modern high performance integrated circuits, more than 40% of the active mode power is dissipated due to the leakage current. With the increased no. of transistor many leakage current comes under picture like sub-threshold conduction current, gate direct tunneling current, punch-through current. Many techniques have been proposed to reduce these leakages.The most important technique is Sleep Transistor technique.

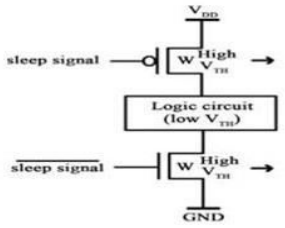

Fig.8.Sleep transistor logic

These High V_{th} is powered by sleep signal. The main logic circuit is made of Low V_{th} transistors. When the circuit is on active mode,the circuit with low V_{th} transistors is on through this high V_{th} transistors, and when the circuit is in inactive mode both high V_{th} are OFF making thecircuit disconnected to V_{dd} and Gnd. This causes reduction in leakage current when circuit is in standby mode

V. SIMULATION AND RESULT ANALYSIS

For testing the proposed multiplier we provide the input combinations as bit parameter.All the combinations are introduced during the time period between 10ns to 20ns.

Thus for the outputs we also concentrate over that particular time period only. We run the simulation over both conventional & proposed two differentmultipliers architecture. The transient responses of all the circuits are shown below in fig.11 & fig.12 respectively. After running the simulation the power consumption and delay of the circuits are tested and compared

TABLE 2: COMPARISN BETWEEN CONVENTIONAL & PROPOSED MULTIPLIER

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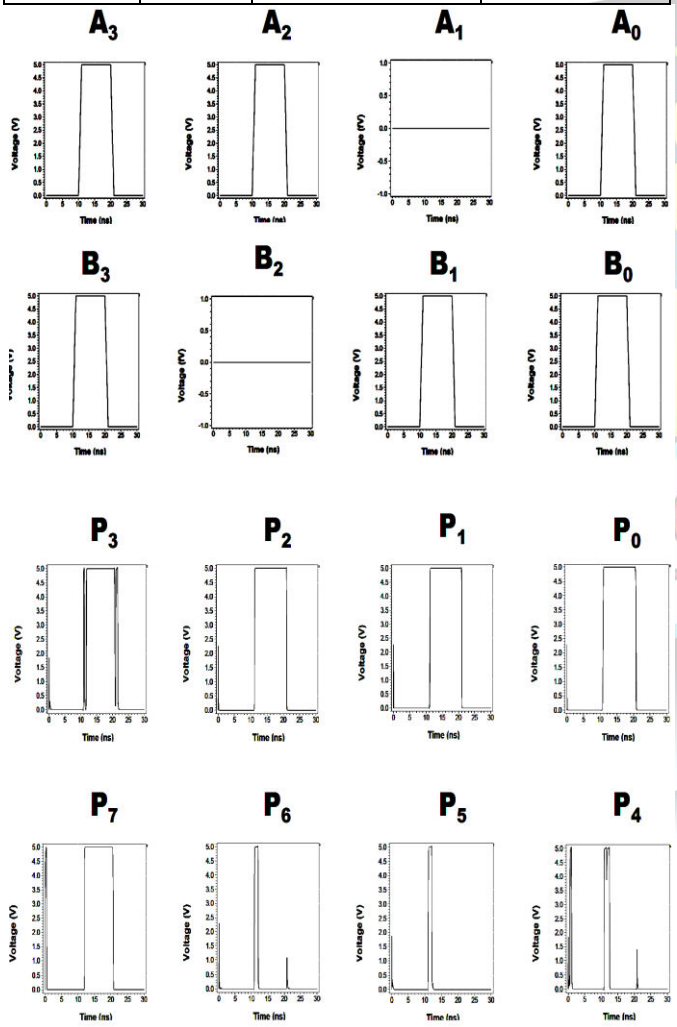
		CONVENTIONAL 4x4MULTIPLIER	PROPOSED 4x4 MULTIPLIER
Power Analysis	Avg. Power	18.15mw	14.32mw
	Max Power	.2267146	.24716
	Min Power	.6970	.49741
Transient Delay Analysis	Rise time delay	1.3875ns	1.100
	Fall time delay:	1.2ns	0.9ns



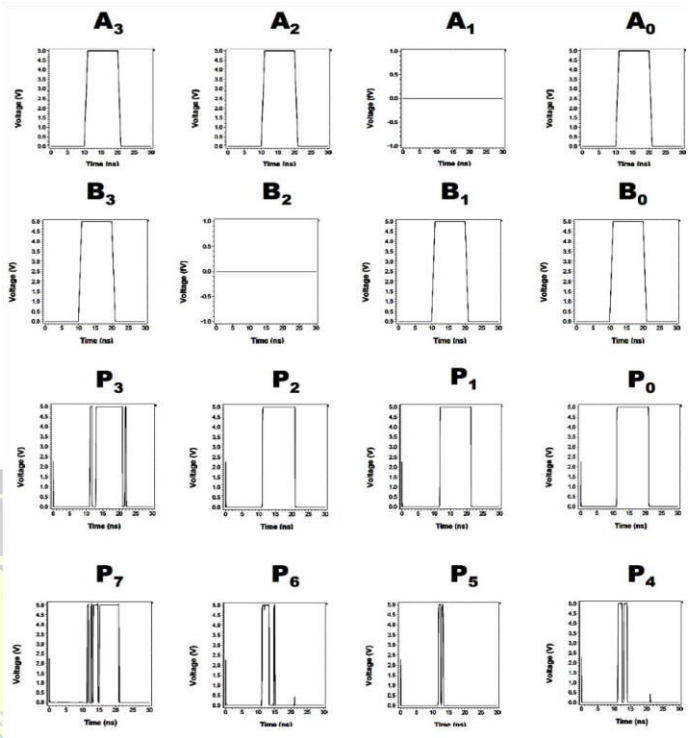


Fig. 10. Transient response of Proposed 4x4 Multiplier Ai: one multiplicand input (4 bits), Bi: one multiplier input (4 bits), Pi: partial product

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Fig. 9 Transient response of conventional 4x4 Multiplier Ai: one multiplicand input (4 bits), Bi: one multiplier input (4 bits), Pi: partial product

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