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ULTRA-EFFICIENT FUZZY MIN/MAX CIRCUITS BASED ON MOSFET WITH DT-SLEEP LOGIC

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***Abstract* -- Fuzzy logic has been successfully deployed in many real world automatic control systems including subway systems, autofocus cameras, washing machines, automobile transmissions, air-conditioners, industrial robots, aerospace, and autonomous robot navigation. In this paper we presents an efficient analog minimum and maximum circuits using DT-sleep (Dual Threshold - Sleep) logic. The proposed system which is used to eliminate the power dissipation such as leakage power dissipation and dynamic power dissipation of the circuit is developed by using the 45nm technology. The simulations conducted by using TANNER software that demonstrate the proposed fuzzy logic blocks considerably improve the performance parameters and function much more robustly even in the presence of process variations as compared to their MOSFET-based counterparts.**

Index terms—Fuzzy logic, Min/Max circuits, Metal Oxide semiconductor Field Effect Transistor (MOSFET).

I. INTRODUCTION

The logic expressions are not always totally true or false in the fuzzy logic, in contrast with the traditional binary logic in which they are either true or false. This concept makes the fuzzy logic more appropriate for the Applications of real life problems. Fuzzy space or explicitly fuzzy set is a very convenient method for representing some forms of uncertainty. In the mid-1960s, Zadeh proposed the idea of 'fuzzy sets' to account for numerous concepts used in human reasoning which are vague and imprecise. Since then, fuzzy sets, logics, and systems theories have been widely developed and have become involved even in human life applications such as autonomous mobile robots, automatic control applications, autofocus cameras, image analysis, diagnosis systems, artificial vision systems and traffic control systems.

Fuzzy systems are usually implemented using three main parts. The first part is "**fuzzifier**", which converts the crisp numbers into fuzzy numbers which varies between 0 and 1. The second part is "**fuzzy inference engine**" that uses the fuzzy set theory to map fuzzy inputs to fuzzy outputs and the last part is "**defuzzifier**" which converts fuzzy numbers into crisp numbers. It is preferred to design a system fully implemented by fuzzy components. To achieve this goal, efficient basic fuzzy operators should be first implemented.

Fuzzy controllers employ the same input and output variables as their conventional counterparts. The difference between both approaches is that, in most of the practically used conventional controllers, the output is obtained as a linear combination of inputs, while in the fuzzy approach, the control heuristic is defined by a set of rules that employ linguistic variables represented by fuzzy sets.

The fuzzy min/max functions are usually implemented based on source-coupled and comparator-based techniques. The source-coupled technique is simpler than the comparator-based technique, but it usually has lower precision, and by increasing the number of inputs, it consumes more power. Also, non-full-swing outputs and higher sensitivity to process variations are the other challenges of this technique.

Fuzzy logic provides a mathematical framework to deal with the uncertainty and the imprecision typical of the human reasoning system. One of its main characteristics is the capability to describe the behavior of a complex system in a linguistic way by means of IF–THEN rules similar to those employed in natural language. The facility of fuzzy logic controllers (FLCs) to capture the knowledge of human experts and translate it into robust control strategies without the need of a mathematical model of the system under control has led to a significant increase in the number of control applications using fuzzy inference techniques in the last 25 years].

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II. LITERATURE SURVEY

1. L. Benini, A. Bogliolo, and G. De Micheli. "A survey on design techniques for system-level dynamic power management," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8, no. 3, pp. 299–316, Jun. 2000.

Method: Dynamic power management is a design methodology for dynamically reconfiguring systems to provide the requested services and performance levels with a minimum number of active components or a minimum load on such components.

Inference: Even though DPM has been successfully employed in many real-life systems, much work is required for achieving a deep understanding on how to design systems that can be optimally power managed.

Demerit: The wake-up time recovery time, which is typically higher than in the case of clock gating because the component's operation must be reinitialized.

2. C. Chunhong, K. Changjun, and S. Majid "Activity-sensitive clock tree construction for low power," InProc. Int. Symp. Low Power Electron. Design, 2002, pp. 279–282.
Method: This paper presents an activity-senitive clock tree contruct in technique for low power design of VLSI clock networks. So We introduce the term of node difference based on module activity information,and show its relationship with the power consumption.
Inference: By using modules activity information,the clock tree construction algorithm and local ungating technique have been introduced for power savings.
Demerit: This requires more attention espcially at some levels close to the leaf nodes,where the weights of control sign as are relatively high.

III. METHODOLOGY

FUZZY LOGIC:

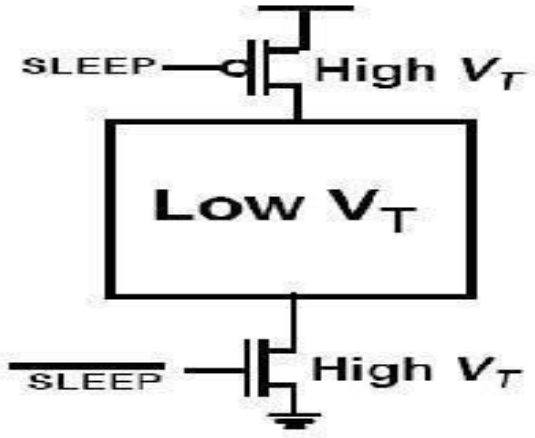
A form of algebra employing a range of values from "true" to "false" that is used in decision-making with imprecise data.

DT-SLEEP TRANSISTOR LOGIC:

In the DT-sleep transistor logic during the active mode only the header switch is conduct and allow the supply to the circuit during the standby mode the header switch is not conducted doesn't allow the power supply to the circuit which is used to eliminate the leakage power dissipation of the circuit

During the standby mode the footer switch is conducted and eliminate the negative feedback of the circuit

A circuit technique is proposed in this paper for simultaneously reducing the subthreshold and gate oxide leakage power consumption in domino logic circuits. Only P- channel sleep transistors and a dual threshold voltage CMOS technology are utilized to place an idle domino logic circuit into a low leakage state.



CMOS DUALITY :

An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistors and NMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground.

To accomplish this, the set of all paths to the voltage source must be the complement of the set of all paths to ground. This can be easily accomplished by defining one in terms of the NOT of the other. Due to the De Morgan's laws based logic, the PMOS transistors in parallel have corresponding NMOS transistors in series while the PMOS transistors in series have corresponding NMOS transistors in parallel.

CMOS LOGIC:

More complex logic functions such as those involving AND and OR gates require manipulating the paths between gates to represent the logic. When a path consists of two transistors in series, then both transistors must have low resistance to the corresponding supply voltage, modeling an AND.

When a path consists of two transistors in parallel, then either one or both of the transistors must have low resistance to connect the supply voltage to the output, modeling an OR. Shown on the below circuit diagram of a NAND gate in CMOS logic. If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and Vss (ground), bringing the output low.

CMOS POWER: SWITCHING AND LEAKAGE :

CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). On a typical ASIC in a modern 90 nanometer process, switching the output might take 120 picoseconds, and happen once every ten nanoseconds. NMOS logic dissipates power whenever the output is low ("static power"), because there is a current path from Vdd to Vssthrough the load resistor and the n-type network.

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Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS Devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the Chip has risen tremendously.

1. STATIC DISSIPATION

1.a. Sub threshold condition when the Transistors are OFF. Both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current (called sub threshold current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (Vdd might have been 5 V, and Vth for both NMOS and PMOS might have been 700 mV). A special type of the CMOS transistor with near zero threshold voltage is the native transistor.

1.b. Tunnelling Current through Gate Oxide SiO2 is a very good insulator, but at very small thickness levels electrons can tunnel across the very thin insulation; the probability drops off exponentially with oxide thickness. Tunnelling current becomes very important for transistors below 130nm technology with gate oxides of 20Å or thinner.

1.c. Leakage Current through reverse biased diodes There are small reverse leakage currents which is formed due to formation of reverse biased between diffusion regions and wells (for e.g., p-type diffusion vs. Nwell) , Wells and Substrate (for e.g., n-Well vs. P-Substrate).

1.d. Contention current in ratioed circuit.

2. DYNAMIC DISSIPATION

2.a. Charging and Discharging of load capacitances CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS Logic , current flows from VDD to the load Capacitance to charge it. and then flows from the Charged Load Capacitance to GND during discharge. Therefore in one complete charge/discharge cycle, a total of Q=CLVDD is thus transferred from VDD to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device: P = CV2f.

Since most gates do not operate/switch at every clock cycle they are often accompanied by a factor α, called the activity factor. Now, the dynamic power dissipation may be re-written as P = αCV2f.

A "Clock" in a system has an activity factor α = 1, since it rises and falls every cycle. Most data has an activity factor of 0.5. If correct Load Capacitance is estimated on a node together with its activity factor, then dynamic power dissipation at that node can be calculated effectively.

2.b. Short Circuit Power Dissipation Since there is a finite Rise/fall time for both pMOS and nMOS, during transition, say, from OFF to ON, both the transistors will be ONN for a small period of time in which Current will find a path directly from VDD to GND. Hence, creating a short circuit current. Short circuit power dissipation increases with rise and fall time of the transistors.

An additional form of power consumption became significant in the 1990s as wires on chip became narrower and the long wires became more resistive. CMOS gates at the end of those resistive wires see slow input transitions. During the middle of these transitions, both the NMOS and PMOS networks are partially conductive, and current flows directly from Vdd to Vss.

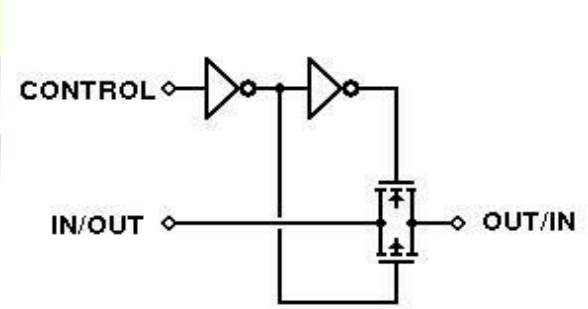
The power thus used is called crowbar power. Careful design which avoids weakly driven long skinny wires has ameliorated this effect, and crowbar power is nearly always substantially smaller than switching power.

To speed up designs, manufacturers have switched to constructions that have lower voltage thresholds;[citation needed] but because of this a modern NMOS transistor with a Vth of 200 mV has a significant subthreshold leakage current. Designs (e.g. desktop processors) which include vast numbers of circuits which are not actively switching still consume power because of this leakage current.

Leakage power is a significant portion of the total power consumed by such designs. Further technology advances that use even thinner gate dielectrics have an additional leakage component because of current tunneling through the extremely thin gate dielectric. Leakage power reduction using new material and system design is critical to sustaining scaling of CMOS.

TRANSMISSION GATE

One type of gate, shown to the FIG, is unique to CMOS technology. This is the bilateral switch, ortransmission gate. It makes full use of the fact that the individual FETs in a CMOS IC are constructed to be symmetrical. That is, the drain and source connections to any individual transistor can be interchanged without affecting the performance of either the transistor itself or the circuit as a whole.



When the N- and P-type FETs are connected as shown here and their gates are driven from complementary control signals, both transistors will be turned on or off together, rather than alternately. If they are both off, the signal path is essentially an open circuit — there is no connection between input and output. If they are both on, there is a very low-resistance connection between input and output, and a signal will be passed through.

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What is truly interesting about this structure is that the signal being controlled in this manner does not have to be a digital signal. As long as the signal voltage does not exceed the power supply voltages, even an analog signal can be controlled by this type of gate.

EXISTING SYSTEM:

In an existing system they design the Fuzzy minimum and maximum circuit separately it cause the it consume more area. The power is dissipate in both active mode and standby mode

Drawback of existing:

In an existing system we used the adiabatic technology .In an adiabatic logic it consume power in both active mode and standby mode.

If the circuit consume the 100% power supply it consume only the 40% remaing 60% is power dissipation the power dissipation is occur due to various reason such as

- Leakage power dissipation
- Dynamic power dissipation
- Short circuit power dissipation

Leakage power dissipation:

The leakage power dissipation is occur due to the leakage of the circuit for an example .If positive voltage is flow in the pmos circuit at that stage the pmos is non conductive due to leakage the power is dissipate.

Dynamic power dissipation:

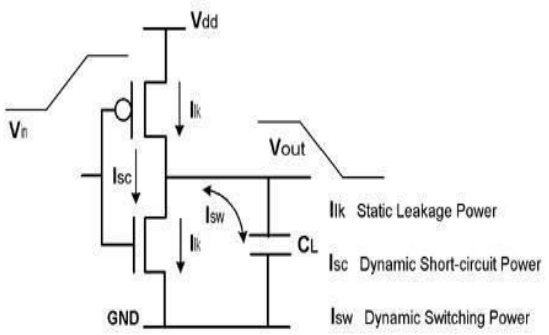
The power is dissipate with in the circuit is called as the dynamic power dissipation it cause reduce in the performance of the circuit .dueto dynamic power dissipation the circuit is will be damaged and make the circuit as the high power consumption circuit.

POWER RESULTS

vdd gnd from time 1e-008 to 1e-006
Average power consumed -> **4.689100e-004 watts**
Max power -> 8.216735e-004 at time 6.71471e-007
Min power -> 1.312049e-009 at time 7.87431e-007

MEASUREMENT RESULTS

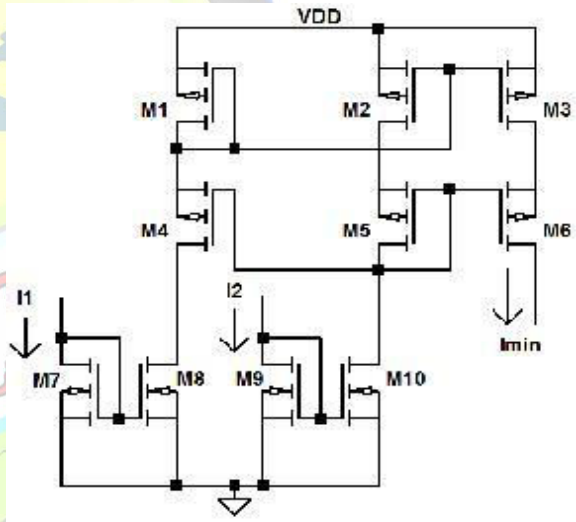
TRAN_Measure_Delay_1 = -2.3821e-
008 * END NON-GRAPHICAL DATA
* Parsing 0.08 seconds
* Setup 0.33 seconds
* DC operating point 0.00 seconds
* Transient Analysis 0.10 seconds
* Overhead 1.50 seconds
* ----------
* Total 2.01 seconds
* Simulation completed
* End of T-Spice output file.



IV. PROPOSED DESIGN

In a proposed system we design the minimum and maximum fuzzy circuit is available in the same circuit. The DT-Sleep logic is applied in the fuzzy minimum and maximum circuit the proposed system which is used to eliminate the power dissipation such as leakage power dissipation and dynamic power dissipation.

CIRCUIT DIAGRAM :



BENEFITS:

The fuzzy minimum and maximum circuit is available on the same circuit.
Leakage power dissipation is less.
Dynamic power dissipation is less.
Circuit efficiency is improved.

APPLICATION:

- wearable device
- Digital signal processing
- Digital image processing

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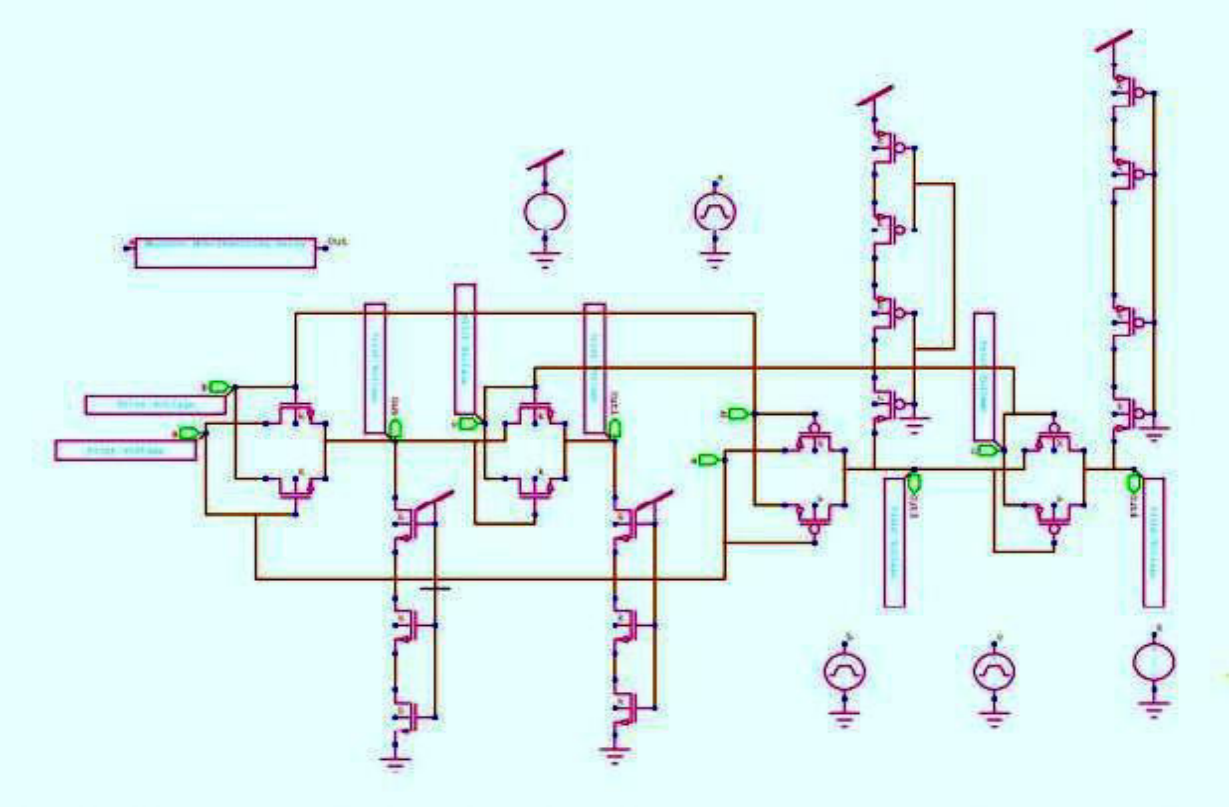
FULL MODULE -MIN AND MAX CIRCUIT ON THE SAME CIRCUIT:



V. CONCLUSION

Ultra-efficient deigns of the fundamental fuzzy logic circuits for nanotechnology have been presented in this paper. Determinable threshold voltage is a unique characteristic of MOSFET, which makes it a very suitable option for designing fuzzy systems. The proposed circuits have been design with a very low number of transistors, which leads to hardware efficiency, low power consumption and high performance operation. Full swing operation, accuracy, small error and the capability of being used in larger circuits are the other great advantages of our proposed designs. The simulation results indicate that these circuits function with high performance and robustness, even in the presence of major process variations.

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