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DESIGN OF AREA EFFICIENT LOW POWER RFID CODE GENERATOR USING 45NM CMOS LOGIC

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***Abstract*—This paper describes the design of the Radio frequency identification tag code generator using control clocked input and sleep logic which consumes low power. The low power design makes the RFID function easier to implement in flexible transponder. The RFID transponder chip generates 16- bit code and programming in ROM (Read-Only Memory). We design the RFID code generator which consist of counter, decoder, clock generator circuit and read only memory circuit with power gating logic which is used to improve the performance of the circuit and reduce the leakage and dynamic power dissipation of the circuit in 45nm technology.**

Keywords—clock generation,distribution networks,Radio frequency identification(RFID),logic circuit

I. INTRODUCTION

The Internet of Everything (*IOE*), also called ambient intelligence, is the subject of intense worldwide research with the goal of interconnecting a large number of "things": intelligent sensors, tags, mobile phones-the list is virtually endless. RFID tags with sensing capabilities are key enablers in Internet of everything(IOE).As the power constraints for RF-harvesting devices are strict,the sensor tags have to work with ultra low power and simple architecture. Our goal is to design low power RFID tag by reducing its size by using 45nm cmos logic in place of 65nm. Currently, flexible electronics research is popular and many application domains in Internet of Things (lOT) industry booming, such as wearable device, smart label, monitoring patch, and product tracking. The RFID technology is the important communicate interface in body-terminal network area of the lOT. The RFID system was embedded sensors such as temperature, motion and pressure which sense "Things" information and connected to internet. New trends in lOT made RFID cheaper, smarter and smaller. But the challenges facing chip are: power consumption, flexibility, ultimate thinness, security, and interoperability. Process in thin-film was diff erent from process in silicon-semiconductor, the essential benefit of

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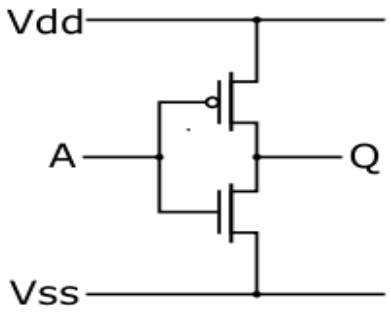
flexible electronics are inexpensive flexible substrates. Thin-film-transistor technology is considered to be the ideal choice for implementing flexible electronics, due to its compatibility with low-cost processes and low-temperature on flexible substrates. **RFID (Radio Frequency Identification** is known for Automatic identification technology which uses radio-frequency electromagnetic fields to identify objects carrying tags when they come close to a reader.Data (identification number for instance) included in the electronic chip of the RFID label can be collected by the reader. This reader can also change the content of the label's memory.However, RFID cannot be reduced to one technology. RFID uses several radio frequencies and many types of tag exist with different communication methods and power supply sources.

II. TECHNOLOGY SCALE DOWN

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated for many types of communication. Frank Wanlass patented CMOS in 1967 CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors(MOSFETs) for logic functions.



CMOS inverter (NOT logic gate)

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip. It was primarily this reason why CMOS won the race in the eighties and became the most used technology to be implemented in VLSI chips.
The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45nanometer node and beyond.

A. CMOS INVERSION

CMOS circuits are constructed in such a way that all P-typemetal-oxide-semiconductor (PMOS) transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistancebetween its source and drain

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contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every n-MOSFET with a p-MOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the n-MOSFET to conduct and the p-MOSFET not to conduct, while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time, both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

B. CMOS DUALITY

An important characteristic of a CMOS circuit is the duality that exists between its PMOS transistors and NMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground. To accomplish this, the set of all paths to the voltage source must be the complement of the set of all paths to ground. This can be easily accomplished by defining one in terms of the NOT of the other.Due to the De Morgan's laws-based logic, the PMOS transistors in parallel have corresponding NMOS transistors in series while the PMOS transistors in series have corresponding NMOS transistors in parallel.

MAJOR PROBLEMS IN THE CIRCUIT:

Power dissipation considerations have become important not only for reliability point of view, but they have assumed greater importance by the advent of portable battery devices such as cell phones, laptops, PDAs etc. The major effects of power dissipation is when power is dissipated, it invariably leads to rise in temperature of the chip.This rise in temperature affects the device both when the device is off and when the device is on. When the device is off, it leads to increase in the number of intrinsic carriers, $n_i$by the following relation:

$$n_i \propto e^{-\frac{EG}{KT}}$$

From this relation it can be seen that temperature increases, it leads to increase in the number of intrinsic carriers in the semiconductors. The majority carriers, contributed by the impurity atoms, are less affected by increase in temperature. Hence the device becomes more intrinsic. As temperature increases, leakage current, which directly depends on minority carrier concentration, increases which leads to further increase in temperature. Ultimately, the device might break down, if the increase in temperature is not taken care of by time to time removal of the dissipated heat.

A ON device won't be affected much by minority carrier increase, but will be affected by VT and μ which decrease with increase in temperature and lead to change in ID. Hence the device performance might not meet the required specifications. Also, power dissipation is more critical in battery powered applications as the greater power dissipated, the battery life will be.

COMPONENTS OF POWER DISSIPATION:

Unlike bipolar technologies, here a majority of power dissipation is static, the bulk of power dissipation in properly designed CMOS circuits is the dynamic charging and discharging of capacitances. Thus, a majority of the low power design methodology is dedicated to reducing this predominant factor of power dissipation. There are three main sources of power dissipation:

- Static power dissipation (PS)
- Dynamic power dissipation (DS)
- Short circuit power dissipation (PSC)

Thus total power dissipation,P_D is given by

$$P_D=P_S+P_D+P_{SC}$$

Two majors power dissipations are:

DYNAMIC POWER DISSIPATION:

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During switching, either from '0' to '1' or, alternatively, from '1' to '0', both n and p transistors are on for a short period of time. This results in a short current pulse from V_{DD} toV_{SS} . Current is also required to charge and discharge the output capacitive load. This latter term is usually the dominant term. The current pulse V_{DD} to V_{SS}results in a 'short-circuit' dissipation that is dependent on the input rise/fall time, the load capacitance and the gate design.

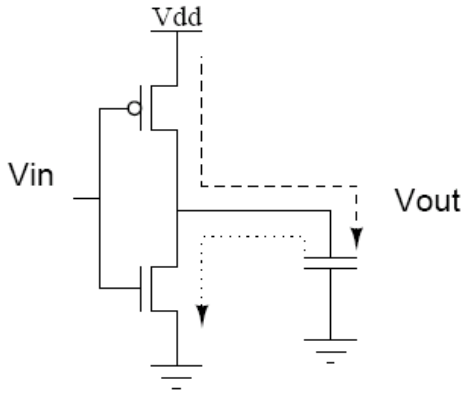


Fig: Power dissipation due to charging or discharging of capacitor

The dynamic dissipation can be modeled by assuming that the rise and fall time of the step input is much less than the repetition period.The average dynamic power P_D, dissipated during switching for a square-wave input, Vin, having a repetition frequency of $f_p=\frac{1}{tp}$, is given by

$$P_D=\frac{1}{tp}\int_0^{tp/2} i_n(t)\, V_{out}\, dt$$

$$+\frac{1}{tp}\int_{tp/2}^{tp} i_p(t)(V_{DD}-V_{out})\, dt$$

where

i_n= n-device transient current

i_p = p-device transient current

Thus for a repetitive step input the average power that is dissipated is proportional to the energy required to charge and discharge the circuit capacitance. The important factor to be noted here is that power to be proportional to switching frequency but independent of device parameters. The power dissipation also depends on the switching activity, denoted by, α. The equation can then can be written as,

$$P_D = C_L V_{DD}^2 f_p$$

SHORT-CIRCUIT POWER DISSIPATION:

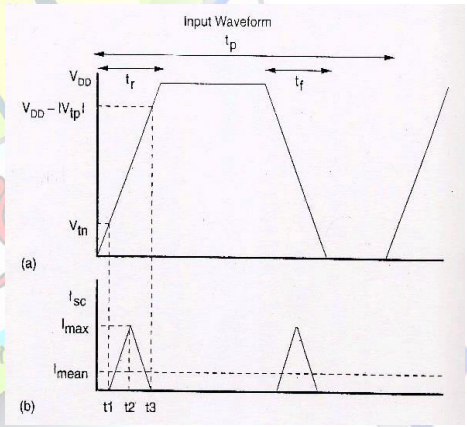
The short circuit power dissipation is given by,

$P_D = I_{mean} * V_{DD}$

For the input waveform shown in figure, which depicts the short-circuit in an unloaded inverter,

$$P_{SC}=\frac{\beta}{2}(V_{DD}-2V_t)^3 t_{rf} / t_p)$$

where t_p is the period of the waveform. This derivation is for an unloaded inverter. It shows that the short-circuit current is dependent on β and the input waveform rise and fall times. Slow rise times on nodes can result in significant **(20%)** short-circuit power dissipation for loaded inverters.



Thus, it is good practice to keep all edges fast if power dissipation is a concern. As the load capacitance is increased the significance of the short-circuit dissipation is reduced by the capacitive dissipation $\mathbf{P_D}$.

45 nm PROCESS

As of 2009, 45 nm technology is largely replacing 90 nm and 65 nm technology in leading-edge chip products. However, some products, notably chipsets, have moved from older 130 nm technology to the 90 nm process.

EXISITING SYSTEM:

In the existing system, the clock generator and the clock distribution network was designed separately, if one of

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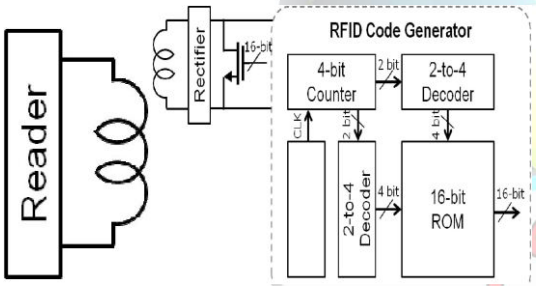
the circuit tends to fail, then the total system will collapse. The clock generator circuit generates clock signal both in active mode and standby mode. This results in leakage power dissipation and dynamic power dissipation.

PROPOSED WORK:

The design of Radio Frequency code generator using controlled clock input and sleep logic that will consume low power. The low power design makes the RFID function easier to implement in flexible transponder. The RFID transponder chip generates 16- bit code and programming in ROM (Read-Only Memory). We design the RFID code generator which consist of counter, decoder, clock generator circuit and read only memory circuit with power gating logic which is used to improve the performance of the circuit and reduce the leakage and dynamic power dissipation of the circuit in 45nm technology.

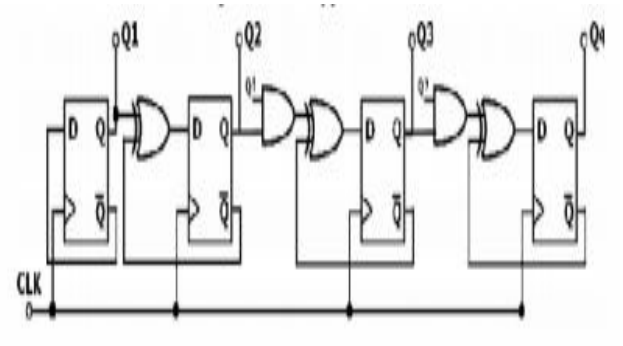


Clock generator circuit

In the proposed system we have designed the clock generator and clock distribution network in the same circuit. The clock generator circuit generates the clock signal and the clock distribution network transfers the clock signal only when the circuit is enabled. The clock generatoroperates only during the active mode and not in the standby mode.

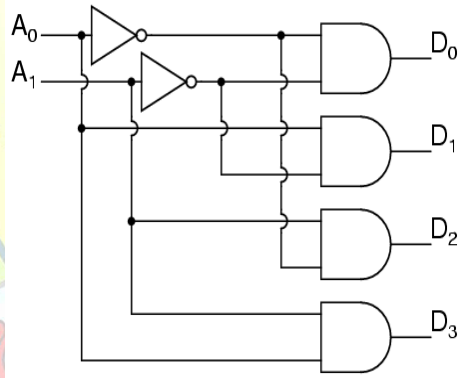
Asynchronous Counters:

Counters, consisting of a number of flip-flops, count a stream of pulses applied to the counter's CK input. The output is a binary value whose value is equal to the number of pulses received at the CK input.



Decoder

A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding.



A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Read only memory

The PROM design was proposed in transponder that stored 16-bit binary data with "1001, 0110, 1010, 0001". There is two control signals from two 2-to-4 decoder, one is data scanned WL and the other is readout signal BL. For memory programming here we used laser program. If readout data is "0", the TFT programmed to the ground. On the other hands, the TFT programmed toV_{DD} and

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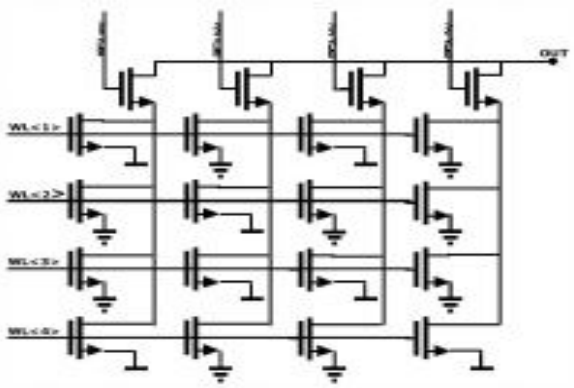
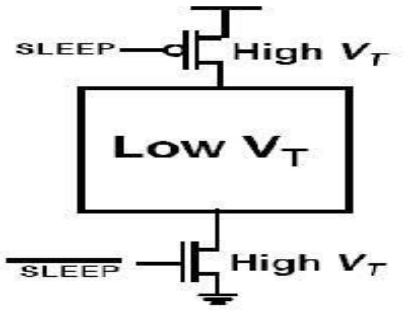
the ROM readout data is "1". The memory output will be latched in a register and sequentially accessed to output buffer, while the register was trigger by system clock as well. The output buffer had to enough capability to driving the modulator.



Sleep transistor logic:

In the sleep transistor logic during the active mode only the header switch is conduct and allows the supply to the circuit. During the standby mode the header switch is not conducted and doesn't allow the power supply to the circuit which is used to eliminate the leakage power dissipation of the circuit.During the standby mode the footer switch is made to conduct and this eliminates the negative feedback of the circuit.



SOFTWARE DESCRIPTION:

TANNER EDA:

Tanner EDA tools for analog and mixed-signal ICs and MEMS design offers designers a seamless, efficient path from design capture through verification. Our aim is to simulate the design of low power RFID code generator using 45nm cmos technology.

CONCLUSION

The design of area efficient low power RFID code generator using 45nm cmos logic has been successfully simulated using Tanner software and the power dissipation has been reduced with reduction in its area.

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