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High speed Belief Propagation Polar Decoder using Overlapping Scheduling Schemes

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Abstract—Polar codes have become increasingly popular recently because of their achieving capacity property. Successive cancellation decoding (SCD) and belief propagation decoding (BPD) are two major approaches for decoding polar codes. Due to the serial nature of the algorithm, SCD suffers from although it requires long latency, less computation as compared with BPD.On the other hand, polar BP decoders have the intrinsic advantage of parallel processing. Therefore, compared with their SC counterparts, polar BP decoders are more attractive for low-latency applications. However, due to their iterative nature, the required latency and energy dissipation of BP decoders increase linearly with the number of iterations. To reduce the computation complexity of several methods have been proposed.

Index Terms—Polar code, BP decoder, energy efficient.

I. INTRODUCTION

Polar code, which is discovered by Arikan recently, is a major breakthrough in coding theory. It is the first known family of error correction codes achieving the Shannon capacity for binary-input discrete memoryless channels. Main attraction polar code is its low coding complexity and channel achieving capacity. Besides achieving the capacity for binary-input symmetric memoryless channels, polar codes were also proved in to be able to achieve the capacity for any discrete and continuous memoryless channel. Moreover, an explicit construction method for polar codes was provided and it was shown that they can be efficiently encoded and decoded with complexity O (n log n), where n is the code length. Since then, polar codes have become one of the most popular topics in information theory and have attracted a lot of attention. Polar code is a best candidate for error correction codes in next generation communication system.

A number of decoding methods have been proposed for polar codes, and among these, successive cancellation decoding (SCD) and belief propagation decoding (BPD) are the two most popular methods. Due to the serial nature of the algorithm, SCD suffers from long latency, although it requires less computation as compared with BPD. Several methods have been proposed to reduce the latency of SC decoders to achieve a high throughput. Moreover, list decoding and stack decoding, which are based on SCD, have been proposed to improve the error-correcting performance for polar codes with short code lengths.

On the other hand, polar BP decoders have the intrinsic advantage of parallel processing. Therefore, compared with their SC counterparts, polar BP decoders are more attractive for low-latency applications. However, due to their iterative nature, the required latency and energy dissipation of BP decoders increase linearly with the number of iterations. The requirement of a large number of iterations results in high computation complexity, and hence makes BPD less attractive than its SC counterpart. To reduce the computation complexity of several methods have been proposed.

II. POLAR CODE OVERVIEW

Polar codes are linear block codes based on the phenomenon of channel polarization, in which

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individual channels are recursively combined and split, such that their mutual information tends toward either 1 or 0. In other words, some of these channels become completely noise-free, while the others become completely noisy. Furthermore, the fraction of noiseless channels tends toward the capacity of the underlying binary symmetric channels.

Polar codes are constructed based on of the polarization effect to achieve the capacity of symmetric channel. An (n, k) polar code is constructed by assigning k information bits and (n-k)'0's at more reliable positions and unreliable positions, respectively. Those fixed '0' bits are usually referred as frozen bits.

Then message bits including frozen bits and information bits are denoted as u in this paper. An (n,k) polar code can be generated in two steps. First, an n-bit message u is constructed by assigning the k reliable and (n-k) unreliable positions as information bits and frozen bits, respectively. The (n-k) frozen bits are forced to 0 and form the frozen set A^{C} The n-bit transmitted codeword x is the product of u and the generator matrix G, where $G=F^{\oplus m}$. $F^{\oplus m}$ is the *m*-th Kronecker power of $F = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ and $m=\log_2 n$. Fig.1 shows the encoding signal flow graph for n = 8 polar codes, where the " \oplus " sign represents the XOR operation,

$u_0 = 1$ $u_1 = 1$			¶	$\begin{array}{c c} 1 & x_0 = 1 \\ \hline 1 & x_1 = 1 \end{array}$
$u_2 = 1$ $u_3 = 0$				$\begin{array}{c} 0 x_2 = 0 \\ 0 x_3 = 0 \end{array}$
$u_4 = 1$	\oplus ¹	\oplus		$x_4 = 0$
$u_5 = 0$ $u_6 = 1$				$ \begin{array}{c c} 0 & x_5 = 0 \\ \hline 1 & x_6 = 1 \end{array} $
$\frac{u_7 = 0}{Input} S$	tage 1	0 Stage 2	Stage 3	$\begin{array}{c c} 0 & x_7 = 0 \\ \hline & \text{Output} \end{array}$

Fig. 1. Encoding signal flow graph of (8.4) polar code

III. BELIEF PROPAGATION DECODING

The BP decoding for polar codes is based on the factor graph representation of the codes. The factor graph for an (n,k) polar code $(n=2^m)$ is an mstage network, which consists of n.(m+1) nodes. Each node is associated with two types of messages: left-to-right messages L and right-to-left messages R. Fig.2 shows the four nodes involved in one basic computation element BE2.



Fig 2.Factor graph of basic computation element BE2 in BP polar decoders.

Firstly, the belief (indicated as log likelihood ratio, LLR) of each node is initiated. The left most source vector nodes in Fig.2 are initiated with zero or positive infinity as Eq.(1) and the right most code word nodes are initiated with channel output LLRs as Eq.(2). Other nodes are initiated with zero

$$R_{i,j} = \begin{cases} 0 \text{ if } j \in A\\ \infty \text{ if } j \in A^c \end{cases}$$

$$L_{n+1,j} = ln \frac{P(y_i|x_i=0)}{P(y_i|x_i=1)}$$

$$(1)$$

In BP decoding, LLRs are passed iteratively from left to right and then from right to left through basic computation elements BE2s to compute the likelihood of information bits. Fig.3 shows an example of a 3-stage factor graph for n = 8 polar codes. Here each stage consists of n/2 = 4 basic computation elements (BEs). During the BP decoding procedure, these messages are propagated and updated among adjacent nodes using the minsum updating rule as shown by the following equations

$$L_{i,j} = g(L_{i+1,2j-1}, L_{i+1,2j} + R_{i,j+N/2})$$
(3)

$$L_{i,j+N/2} = g(Ri,j, L_{i+1,2j-1}) + L_{i+1,2j}$$
(4)

$$R_{i+1,2j-1} = g(R_{i,j}, L_{i+1,2j} + R_{i,j+N/2})$$
(5)

$$\mathbf{R}_{i+1,2j} = \mathbf{g}(\mathbf{R}_{i,j}, \mathbf{L}_{i+1,2j-1}) + \mathbf{R}_{i,j+N/2}$$
(6)

Where

(2)

$$g(x,y) = \log(\cosh((x+y)/2)) \cdot \log(\cosh((x-y)/2))$$
(7)

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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol. 5, Special Issue 12, April 2018 it can be simplified as :

 $g(x,y) \simeq 0.9.sign(x)sign(y).min(|x|,|y|)$ (8)



Fig3. Factor graph for n=8 polar code

After t iterations, the decision can be made based on the final LLR results of source vector nodes as

$$u_j = \begin{cases} 0 & if R_{i,j} \ge 0\\ 1 & else \end{cases}$$
(9)

Due to their iterative nature, the required latency and energy dissipation of BP decoders increase linearly with the number of iterations. The requirement of a large number of iterations results in highcomputation complexity, and hence makes BPD less attractive than its SC counterpart. To reduce the computation complexity of several methods have been proposed.

IV. BP DECODER USING OVERLAPPING SCHEDULING SCHEMES

According to the decoding procedure of BP algorithm, PEs are activated stage-by-stage from left to right in each iteration. Fig. 4 shows an example of this decoding scheme of (16, 8) polar code for 3 iterations. Here, $C_{i,j}^{P}$ indicates that, the propagating messages that belong to the i-th received codeword are updated in the j-th stage of PEs during the p-th iteration. For example, $C_{1,3}^2$ in clock cycle-7 represents that, in order to decode the 1st received codeword, the stage3 is activated and processes the propagating messages in the 2nd iteration. In addition, the arrow in Fig. 4 describes the data dependency in (5.2). Here the black arrow indicates the dependency within the same iteration, and the

red arrow indicates the dependency between consecutive iterations. For example, only after stage 1 and stage 3 finish processing $C_{1,3}^2$ and $C_{1,3}^l$, respectively, their output is sent to stage 2 as its inputs, and then stage 2 is allowed to process $C_{1,2}^2$. From Fig. 4 it can be seen that in each cycle, only one stage is activated while other stages are always idle. For a (n, k) polar BP decoder, this yields a low hardware utilization rate of only 1/m.



Fig4. Original decoding scheme of n=16 BP decoder.

Fig. 4 shows that m-1 stages of PEs are idle in each cycle of polar BP decoding. In order to avoid this under-utilization, overlapped scheduling technique can be used to fully utilize those idle resources. In this section, we discuss the iterationlevel overlapping first. After a careful examination of Fig. 4, we find that in each cycle multiple stages can be activated at the same time. For example, consider $C_{1,3}^2$ in cycle-5 at stage 1. This computation is dependent on output from $C_{1,2}^2$ C in cycle-2 at stage 2. Since stage 2 can process $C_{1,2}^2$ in cycle-2, stage 1 can process $C_{1,1}^{l}$ at the beginning of cycle-3. Therefore, instead of being activated in cycle-5 in the original scheme (see Fig.4), stage1 can now be enabled in cycle-3 to process propagating messages for the 2^{nd} iteration $(C_{l,l}^2)$ without any timing conflict (see Fig. 5). As a result, one clock cycle can be saved by applying this rescheduling approach. Similarly, Fig. 5 shows that the other stages can also be activated earlier. Therefore, this re-scheduling approach can lead to reduction of 4 cycles in latency.

By exploiting overlapped-scheduling, from Fig. 5, it can be seen that, from cycle-3 to cycle-6, some computations belong to either 2nd or 3rd iteration. This overlapped-rescheduling approach leads to great reduction in decoding latency. In general, for an (n, k) polar BP decoder with m-stages of PEs, the proposed iteration-level overlapped scheduling All Rights Reserved © 2018 IJARTET 101



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approach reduces the decoding latency from $m*max_iter$ to $2*max_iter+m-2$ clock cycles, where max_iter is the preset maximum number of iterations. Considering *m* is usually larger than 10 for practical use, the latency can be reduced by approximately 10/2=5 times.



Fig 5. Overlapped-scheduling at iteration level.

Although the above iteration-level overlapped scheduling method can greatly improve the hardware utilization, the schedule in Fig. 5 cannot achieve 100% hardware utilization since some stages still remain idle. In general, due to the data dependency between successive iterations, the maximum hardware utilization rate of iteration-level overlapped scheme is limited to be less than 50%.



Fig 6. 4-level-overlapping at codeword level.

Different from iteration-level overlapping, codeword-level overlapping, as а common technique used in SC decoder designs, can make hardware utilization close to 100%. In this section, apply this technique for BP we decoder optimization. Fig. 6 shows an example of a 4-levelcodeword-overlapping scheme. Here different colors represent propagating messages belonging to different received code words. Compared with original scheme with iteration-level overlapping (see Fig. 4 and Fig. 5), the codeword-level overlapping scheme fully utilizes those idle stages

to process multiple independent received code words. As a result, the hardware utilization rate approaches 100%. In general, for an (n, k) polar BP decoder, maximum m independent received code words can be input to the decoder for overlapped processing. As a result, the processing throughput increases by approximately m times at the expense of an extra m-1 clock cycles, and (m-1) times more memory for storing the cod ewords than that in Fig..4

V. RESULTS AND DISCUSSION.

The simulation results for 8 bit polar decoder which is obtained by simulating the Verilog code for the design shown in figure 7. Xilinx software is used to verify the functionality of my design.







Fig 8. Simulation result of 8 bit Polar decoder using proposed scheme.

Table.1. Timing Analysis

Performance Parameter	Dealy (ns)
Existing Scheme	1.285
Overlapping at iteration level	1.106
Overlapping at code level	1.024

VI. CONCLUSION

In this paper, a novel early stopping method based on overlapping scheduling scheme is proposed for BP polar code decoders. This method not only reduces the average complexity of the BPD, hence reducing the energy consumption during decoding, but also helps to make the decoding faster. This reduces average latency.



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