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DESIGN OF A IIR FILTER WITH HAN CARLSON ADDER BASED MAC

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***Abstract*—Digital filters are basic building blocks in digital signal processing (DSP) systems. DSP techniques improve signal quality or extract important information by removing unwanted parts of the signal. This extraction of the unwanted parts of the signal is possible with the help of filters. A Infinite Impulse Response (IIR) filters role in many of the signal processing applications. IIR filters have much better frequency response than FIR filters of the same order. An IIR digital filter can offer improved selectivity, computational efficiency and reduced system delay. The output is computed using multiply and Accumulate (MAC) operations. In the proposed system a 6th order IIR filter design using more efficient merged multiplier accumulator (MAC) unit .MAC unit contain multiplier and adder. Modified Booth algorithm and Wallace tree architecture is used for efficient multiplication and a conventional carry save adder is for addition. In the proposed MAC unit use a Han Carlson Parallel prefix adder instead of carry save adder. This MAC unit is used to implement basic second order IIR filter circuit because of high speed filter computation operation. From this basic structure higher order filters like 4th and 6th order filter circuit can be implement.**

Keywords*—*IIR filter,MAC unit,Han Carlson adder

I. INTRODUCTION

In signal processing, the function of a filter is to remove unwanted parts of the signal, such as random noise, or to extract useful parts of the signal, such as the components lying within a certain frequency range. There are two main kinds of filter, analog and digital. A digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. Based on the length of impulse response, digital filters are classified into two types 1) Finite Impulse Response (FIR) Filters 2) Infinite Impulse Response (IIR) Filters.

In digital filters, multiplication and repeated addition (MAC) is used to remove unwanted noise content from the original signal. So the MAC unit is the basic building block for result computation in filter circuit. The basic MAC architecture consists of multiplier, adder and register/accumulator. The inputs are *n* bits wide. The multiplier produces a 2*n*-bit result that is added to the value of the previous MAC result from the register (initially it is set to zero) .The performance of conventional MAC is improved by using a multiplier cum accumulator block structure. This MAC that avoids a separate accumulation unit by feeding the previous MAC result as one of the partial products to the multiplier cum accumulator. So the depth of the circuit reduced and performance increased

Multiplier part of the MAC unit can be designed using various methods. Popular multipliers like array multiplier and Wallace tree multiplier [9] are used in MAC unit. Nowadays Booth Wallace tree multiplier is the efficient multiplier and it is used in merged MAC unit design. In this multiplier, the partial products are generated using the Booth method, while their summation is done using Wallace tree structure. This compresses the addition process. The adder is used in adder accumulator configuration, where the multiplication result is added every time to the partial product register. In the existing MAC unit consists a modified Booth Wallace tree multiplier. It is the most efficient and high speed multiplier. The Modified Booth Encoding (MBE) is used for the first step because it cut the number of partial products rows in half. This prevent the extra partial product row, and this save the time of one additional carry save adding stage and the hardware required for the additional carry save adding

The second part of the MAC is accumulator which can be designed in several ways namely, ripple carry adder, carry look ahead adder and carry save adder. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. A carry save adder consists of a ladder of stand-alone full adders, and carries out a number of partial additions. So all these adders takes more delay for sum calculations.

This efficient MAC structure used in the IIR filter design to improve the performance of IIR filter architecture Configurable 6^{th} order IIR filter also implemented. The configurable 6^{th} order IIR filter is made up of three cascaded biquad (2^{nd} order)

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IIR filters and the same is used to perform one 6th order or three 2nd order or one 4th order and one 2nd order IIR filter operations in parallel .For this merged MAC unit is used to design each of this 2nd order filter.

The objective of this paper is to improve the performance of IIR filter architecture using a modified merge MAC unit. This paper describes about the proposed system, a 6th order IIR filter design using more efficient merged multiplier accumulator (MAC) unit .MAC unit contain multiplier and adder. Modified Booth algorithm and Wallace tree architecture is used for efficient multiplication and a conventional carry save adder is for addition. In the proposed MAC unit use a Han Carlson Parallel prefix adder instead of carry save adder. This MAC unit used to implement basic second order IIR filter circuit because of high speed filter computation operation. From this basic structure higher order filters like 4th and 6th order filter circuit can be implement

The paper is organized as, section II states the existing architecture for IIR filter design. Proposed system with modified MAC unit explains in section III and results are stated in section IV, followed by a section V conclusion

II. EXISTING IIR FILTER

This section describes about the existing system that consists of merged multiplier accumulator (MAC) unit .MAC unit contain multiplier and adder. Modified Booth algorithm and Wallace tree architecture is used for efficient multiplication and a conventional carry save adder is for addition. This overall MAC unit used to implement basic second order IIR filter circuit because of high speed filter computation operation. From this basic structure higher order filters like 4th and 6th order filter circuit can be implement. Also for reducing the circuit area folded transformation technique used. So the existing system explains the design of 6th order IIR filter with basic 2nd order with high speed MAC unit.

a. MAC Structure

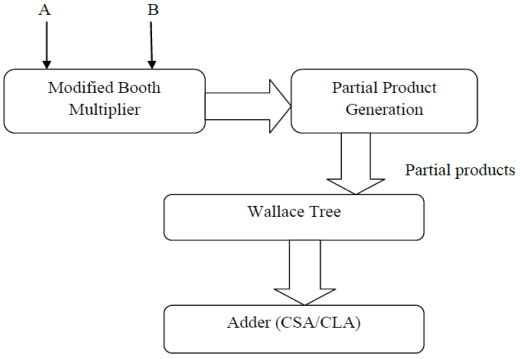

Fig.1.Existing MAC structure

Basic MAC unit contains multiplier and a accumulate adder.in this structure modified Booth multiplier is used because of its high performance.it reduces the number of partial products in multiplication than conventional multipliers. Normal booth multiplier two bits at a time for multiplication. But in modified booth multiplication three bits taken at a time, so it reduces the partial products. Here, Modified Booth algorithm and Wallace tree architecture is used for efficient multiplication. In this multiplier, the partial products are generated using the Booth method, while their summation is done using Wallace tree structure. This compresses the addition process.A conventional carry save adder is for addition and it takes more delay for sum calculation.

b. 2nd order IIR filter

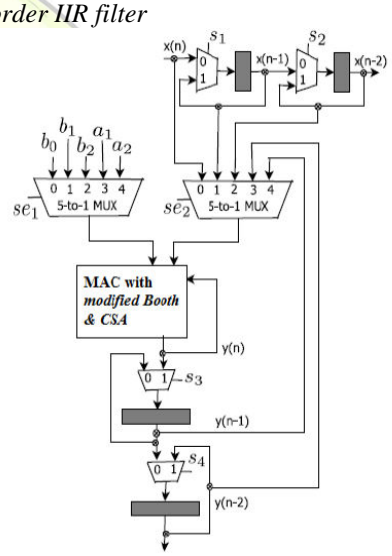

Fig.2.Second order IIR filter

Each 2nd order FIR filter is designed with one multiplier followed by an accumulator (existing MAC).The folded digital filter design is used, where one multiplier followed by one adder is used to find all the multiplication and repeated addition operation using multiplexers and d-flip flops. The multiplexers are used to select the appropriate input/output signal sample values and filter coefficients.

The second order IIR filter design is shown in Fig.2, where Booth algorithm based existing MAC is used to find all the multiply-accumulate values. Here b_0,b_1,b_2, a_1 and a_2 are filter coefficients. The input and output signal sample values are represented as x(n) and y(n) respectively. Here multiplexers play the major role, which select the appropriate input/output signal sample values and filter coefficients for each clock cycle.MAC unit uses the modified Booth algorithm and Wallace tree

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compression for efficient multiplication and a carry save adder (CSA) for addition

c. Configurable 6th order filter

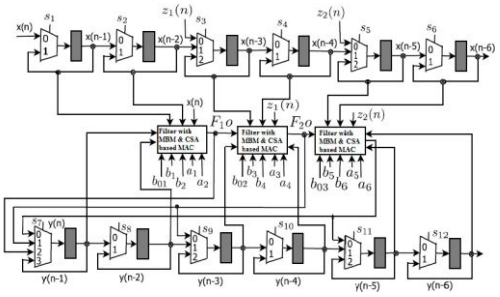

Fig.3.6th order IIR filter

The multi-mode filtering is used to implement higher order filters. The cascade of 2nd order FIR filters is used to vary the order of filter according to the requirement. The configurable 6th order IIR filter is made up of three cascaded biquad (2nd order) IIR filters and the same is used to perform one 6th order or three 2nd order or one 4th order and one 2nd order IIR filter operations in parallel, where merged MAC with Booth and Wallace tree algorithm along with carry save adder is used to design each biquad IIR filters. The proposed configurable sixth order IIR filter design is shown in Fig. 3.6, where three biquad IIR filters (F1, F2 and F3) are cascaded to perform one 6th order or three 2nd order or one 4th order and one 2nd order IIR filter operations.

III. PROPOSED IIR FILTER

d. MAC structure

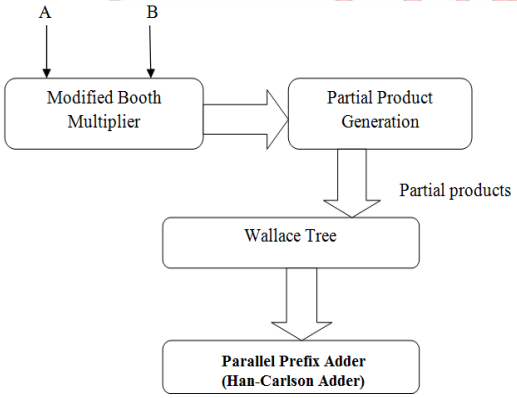

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Fig.4.Proposed MAC unit

In the proposed MAC unit use a Han Carlson Parallel prefix adder instead of carry save adder. This MAC unit used to implement basic second order IIR filter circuit because of high speed filter computation operation. From this basic structure higher order filters like 4th and 6th order filter circuit can be implement using modified merge MAC unit.

In proposed MAC unit, conventional carry save adder is replaced by a parallel prefix adder. Parallel Prefix adder is that it is primarily fast when compared with ripple carry adders. Parallel Prefix adders (PPA) are family of adders derived from the commonly known carry look ahead adders. These adders are best suited for adders with wider word lengths. PPA circuits use a tree network to reduce the latency to O (log2 n) where 'n'represents the number of bits.

e. Parallel Prefix Adder

Parallel-prefix structures are found to be common in high performance adders because of the delay is logarithmically proportional to the adder width. Such structures can usually be divided into three stages as follows: precomputation, prefix tree and post computation.. The pre-processing part will generate the propagate (p) and generate (g) bits. The acquirement of the PPA carry bit is differentiates PPA from other type of adders. It is a parallel form of obtaining the carry bit that makes it performs addition arithmetic faster.

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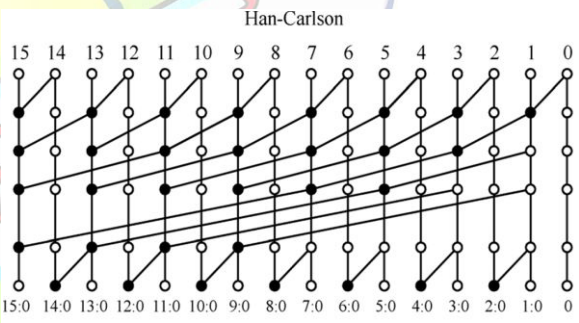

Fig.6.Han- Carlson adder

Han-Carlson adder is a parallel prefix adder. It constitutes a good trade-off between fan out, number of logic levels and number of black cells. Because of this, Han-Carlson 19 adder can achieve equal speed performance respect to Kogge-Stone adder, at lower power consumption and area. The idea of Han-Carlson prefix tree is similar to Kogge Stone's structure since it has a maximum fan-out of 2. The difference is that Han Carlson prefix tree uses much less cells and wire tracks than Kogge-Stone. The cost is one extra logic level. Here black dots represent the prefix operator, while white dots are simple placeholders.

IV. RESULT & DISCUSSION

The following section gives the software implementation results of the paper .Results are simulated using ModelSim software in VHDL language, section by section. Xilinx software used

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Area Components	IIR Filter with ***Carry Save*** Adder Based MAC	IIR Filter with ***Han Carlson*** Adder Based MAC
Slice Register	505	507
LUTs	651	668
Flip Flops	421	423
Delay (ns)	8.3	8.1
Power (mW)	371	358

Table.1. Area Components Analysis

Performance Parameters	IIR Filter with ***Carry Save*** Adder Based MAC	IIR Filter with ***Han Carlson*** Adder Based MAC

Table.2. Performance Parameters Analysis

to measure the delay, area and power parameters. The first section is the result of existing 6th order iir filter with carry save adder based MAC unit and next is the Han Carlson based MAC filter.

1. Existing Structure

a. Sixth order IIR FILTER

Sixth order IIR filter implemented using the basic second order filters. Three 2nd order filters are cascaded serially to obtain a configurable 6th order IIR filter. This sixth order filter includes the merged MAC unit with Booth and Wallace tree structure along with a carry save adder. The output waveform of 6th order configurable IIR filter is shown in fig.8

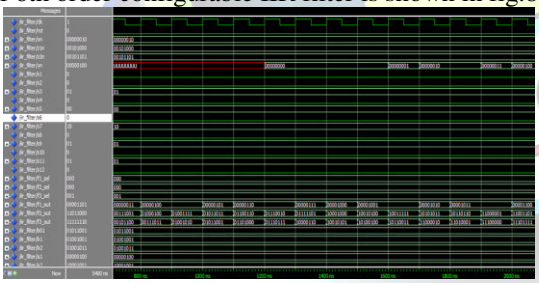

Fig.7. Output waveform of configurable 6th order IIR filter

2. Proposed Structure

b. Sixth order proposed IIR filter

This sixth order filter includes the merged MAC unit with Booth and Wallace tree structure along with a Han Carlson adder. The output waveform of 6th order configurable IIR filter is shown in fig.9

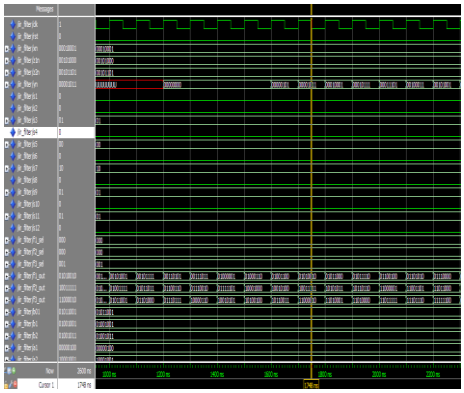

Fig.8.Output waveform of proposed 6th order IIR filter

Synthesis report of the existing system analyzed by Xilinx 14.1 software. Delay, area and power parameters are calculated using this software. Performance parameters like delay, power of the existing IIR filter system is 8.3ns, 371mW respectively. In proposed system delay, power is reduced to 8.1ns, 358Mw respectively

V. CONCLUSION

Verified the simulation results of the existing MAC structure and configurable sixth order filter using Modelsim software in VHDL language .And also calculated the performance parameters like delay, power and area of the existing system. Verified the simulation results of existing IIR filter structure using merged MAC unit with carry save adder and the modified filter structure using parallel prefix adder based MAC unit. Analyzed synthesis report of both existing & proposed system using Xilinx 14.1software. Performance parameters like delay, power is reduced in proposed system. Area slightly increased in proposed system but overall device utilization is same.

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