ISSN2394-3777 (Print)
ISSN2394-3785 (Online)
Available online atwww.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 12, April 2018

Low Power Parity Bit Based Self Controlled Precharge Free Cam

Vinny P.B[#1], Rachana M.K[*2]
M.Tech student in VLSI Design, Assistant Professor, ECE
IES College of Engineering Thrissur, India

Abstract— **Content-addressable memory special type of memory. It is a hardware search engine used for parallel lookup and have several applications such as databases, associative computing, and networking, that require highspeed searches due to its ability to improve application performance by using parallel comparison to reduce search time. . The paper introduces a new aspect in which parity bit computation method is in cooperated with existing SCPFCAM structure.**

Keywords— CAM , ML,PF CAM

I.INTRODUCTION

CAM is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high-speed table lookup.[1-5] Content addressable Memory (CAM) compares input search data against a table of stored data, and returns the address of the matching data .CAMs have a single clock cycle throughput making them faster than other hardware- and software-based search systems. CAMs can be used in a wide variety of applications which requires high search speeds.

CAM is useful for high-performance forwarding, which performs the search in a single clock cycle. In a CAM the user inputs the contents to be searched and the cam gives back the address location CAM stores the data in its memory through bitline drivers. The input data driver feeds the search content to CAM, which performs the search operation. It produces the match address, if any stored data matches with the search content [7]. A sense amplifier is used to access the match information (hit/miss). Each search is performed followed by a precharge phase, a constraint to the faster search frequency. Designing a high-speed CAM for larger word lengths is a challenging task. Fig. 1 shows a simplified block diagram of a CAM. The input to the system is the search word that is broadcast onto the search lines to the table of stored data. The number of bits in a CAM word is usually large, with existing implementations ranging from 36 to 144 bits. A typical CAM employs a table size ranging between a few hundred entries to 32K entries, corresponding to an address space ranging from 7 bits to 15 bits. Each stored word has a match line that indicates whether the search word and stored word are identical (the match case) or are different (a mismatch case, or miss). The match lines are fed to an encoder that generates a binary match location corresponding to the match line that is in the match state. An encoder is used in systems where only a single match is expected. In CAM applications where more than one word may match, a priority encoder is used instead of a simple encoder. A priority encoder selects the highest priority matching location to map to the match result, with words in lower address locations receiving higher priority. In addition, there is often a hit signal (not shown in the figure) that flags the case.in which there is no matching location in the CAM. The overall function of a CAM is to take a search word and return the matching memory location.

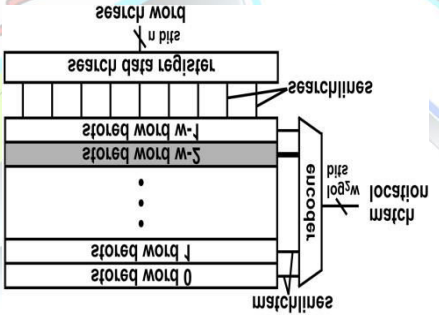

Fig 1 conventional organizatio

A is performed in cam through three phases: data write, precharge, and data search. NAND-type ML CAM cell, as shown in Fig 2, consists of one SRAM cell and a pair of nMOS transistors in the comparison circuit and one nMOS transistor (M9) in evaluation logic. The bit line pair (BL, BL) has been used to store the data in the CAM cell and search-line pair (SL, SL) is used to search the content in CAM cell. Before performing a search, all MLs must be precharged to the supply voltage by keeping search-lines at low. If the search content matches with thedata, ML discharges to a low value

ISSN2394-3777 (Print)
ISSN2394-3785 (Online)
Available online atwww.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 12, April 2018

[ground (GND)]; otherwise ML remains at a precharged value.

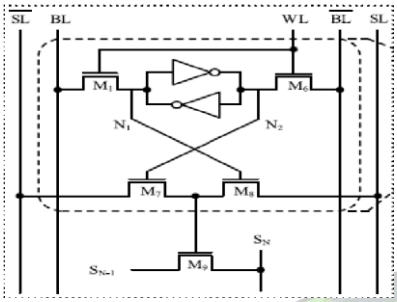

Fig 2 Nand type CAM

This paper gives an detailed analysis of the cam structures SCPF CAM which is heavily used for the high speed applications. In the third section introduces the idea of the parity bits. Later this parity bit method is in cooperated With SCPF CAM generates a new CAM Structures The paper is analyzed in ModelSim with the help of VHDL language .

II.CAM STRUCTURES

So far the development of the cam is done with precharging of the matchlines. Ie, In a conventional CAM, before performing a search, all matchlines (MLs) need to be precharged. This consumes more power as well as reduces the performance and frequency of operation due to requirement of an extra precharge phase. this is an disadvantage.

a.Precharge-Free CAM

The development of a CAM structure is carried out with a PRE signal, which ends up at a lower speed of search operation. this drawback has been eliminated by removal of the PRE phase. Instead, they used control bits (CBs), which reduced the overall search time by one level. In a CAM, the first operation is write, followed by precharge, and then search. However, in the PF-CAM architecture, the write is followed directly by the search phases. The operation of the PF-CAM is as follows .the main functions of cam is bit
storage and bit comparison

- While storing the data, CB is set to a high value (logic1). This setting of CB turns M0 OFF and, simultaneously, M1,……MN−1 will be turned OFF ,MD0 ,……MDN−1are N, which will provide GND directly to the gate of M1,……MN−1,
- Once the data are stored, CB is reset (0) and this will turn ON M0 as M0 is a pMOS, since the source of M0 isconnected as a control to M1, thus S0 value is passed to the gate of M1, which is an nMOS. If CAM cell-1 is matched, M0 will pass logic high to M1, which will result in turning ON of M1. If CAM cell-2 is also matched, then in a similar fashion logic high will be passed to M3 from CAM cell-2, and likewise a cascaded chain of CBs will be passed from to another. If there is a mismatch at any cell, then the forthcoming cells will be turned OFF.

This structure gives advantage by reduction in the number of SC paths, which in turn results in overall reduction of power; however, due to cascading of CAM cells overall, the speed of search operation is significantly reduced. To avoid this problem, the SCPF-CAM architecture is proposed.

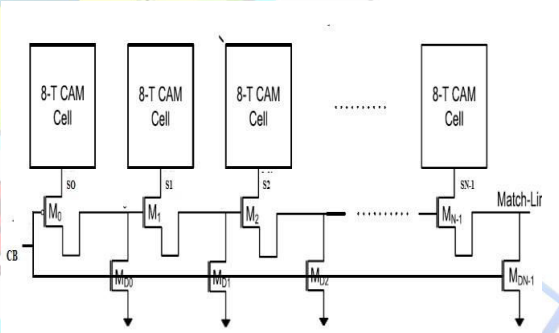

Fig 3 Precharge Free CAM [1]

b.Self-Controlled Precharge-Free CAM

The CAM precharges and evaluates all the MLs for every PRE cycle during the low and high level of the PRE signal, respectively. Problems detected by the earlier methods are

- The speed of the search operation is restricted by the precharge phase.
- Dependence among CAM cells restricts the speed of search operation and this affects the overall performance. NAND-type ML suffers from the charge sharing problem.

In SCPF-CAM, the advantage of the PF-CAM structure is exploited; moreover, drawbacks of the precharge-based earlier reported circuits (which was cascading) are also taken care of by removing

ISSN2394-3777 (Print)
ISSN2394-3785 (Online)
Available online atwww.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 12, April 2018

dependence among different CAM cells. The advantage ofthe proposed architecture is the design of larger word lengths with higher performance at a higher frequency of operation. Owing to the larger delay metric in PF-CAM, it is not useful for forming longer word lengths and cannot operate at a higher frequency of operation.

Fig. 4 illustrates the SCPF-CAM structure, which solves the all the mentioned problems present in the precharge-based CAMs and improves the speed of operation compared to the PF-CAM architecture.. Two major contributions are made: 1) self-control operation, where the charge stored at the node S controls the ML transistors, thereby avoiding the dependence on previous ML value; and 2) the scheme eliminates the precharge phase to provide a higher search frequency. The SCPF-CAM is self-controlled; the node (S) value of the 8T CAM cell controls the evaluation logic and produces the output. If the search content matches the prestored data, then it passes a high value through M9; otherwise it passes a low value through M10 to the ML.

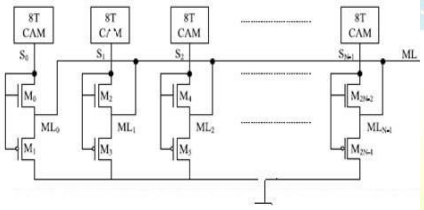

fig 4 Self Controled Precharge Free Cam[2]

The minimum amount of time required in the conventional

CAM operation is

$$T_{Total} = T_{precharge} \pm T$$

However, in the proposed design the minimum requirement

is T_{Tote}

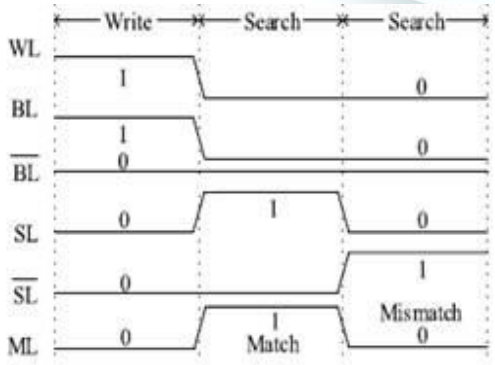

Fig 5 operational phases[1]

III. ARCHTECTURE OF PROPOSED SYSTEM

Content addressable memory (CAM) is a type of solid-state memory in which data are accessed by their contents rather than physical locations. It receives input search data, i.e., a search word, and returns the address of a similar word that is stored in its data-bank. Since all available words in the CAMs are compared in parallel, result can be obtained in a

single clock cycle. Due to its parallel match-line comparison, It consumes more power. In all above mentioned systems , there might be huge delay and power consumption. So in my proposed system a technique adopted to reduce it. Here introduced a versatile auxiliary bit to boost the search speed of the CAM at the cost of less than 1% area overhead and power consumption

The parity bit based CAM design is shown above consist of the original data segment and an extra one-bit segment, derived from the actual data bits. only the parity bit, i.e., odd or even number of ―1‖s is used. The obtained parity bit is placed directly to the corresponding word and ML. Thus the new architecture has the same interface as the conventional CAM with one extra bit.

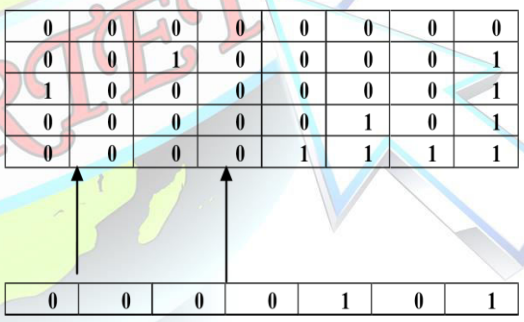

Fig 6 parity bit Concept

During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance. delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, In the case of a matched in the data segment the parity bits of the search and the stored word is the same, thus the overall word returns a match. When 1 mismatch occurs in the data segment numbers of ―1‖s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two

ISSN2394-3777 (Print)
ISSN2394-3785 (Online)
Available online atwww.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 12, April 2018

mismatches in the data segment the parity bits are the same and overall we have two mismatches.

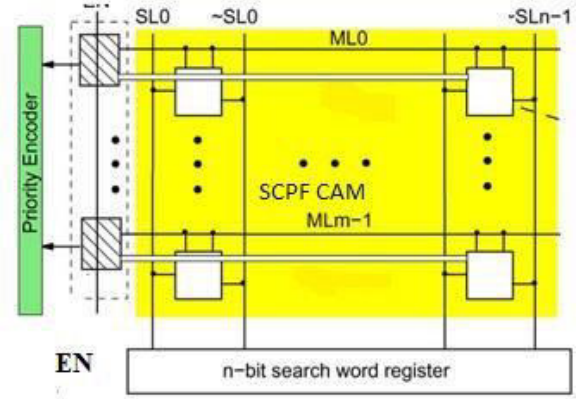

Fig 6 Proposed Structure

The parity bit used here act as a enable .parity bit is obtained by the counting the number of ones. Based on the parity the match lines are divided in to odd lines and even lines . Ie if the en equals one then even match lines are enabled . By doing so the time take to search data will be small.

III.RESULT & DISCUSSION

The following section gives the software implementation results of the paper .Results are simulated using ModelSim software in VHDL language, section by section. Xilinx software used to measure the delay, area and power parameters..

1.Existing Structure

a.PFCAM

From the figure given above ,it is given that control bit plays an important role.It is set to high during writing process so there won't be any output. Control bit is reset . output will available according to the inputted address location. If the inputted address location is not in the router table so the output will be a unknown value

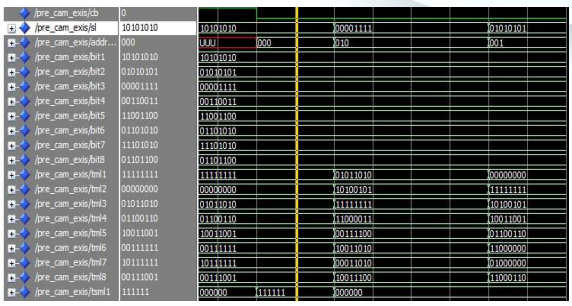

Fig.7.Output waveform of existing of the PFCAM

b.SCPF CAM

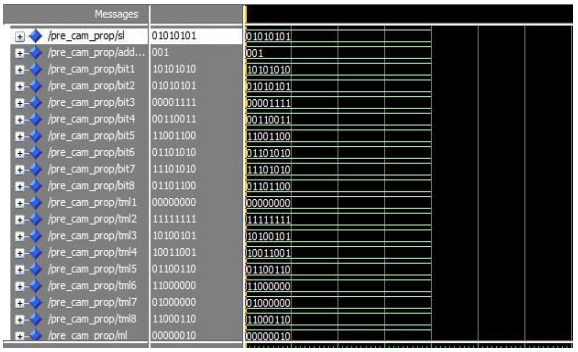

Fig.8. Output waveform of SCPFCAM

Here only difference is there won't be any control bit. output merely the same. The main advantages there will be a considerable amount of reduction in case of delay and Here it shows the modelsim simulation .it will have has high speed comparing the former one

2.Proposed System

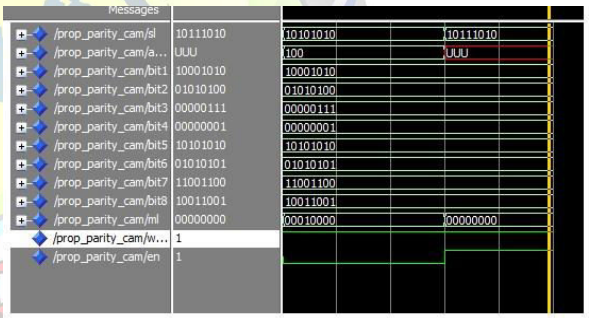

Fig.9.Output waveform of PBSCPF-CAM

Synthesis report of the existing system analyzed by Xilinx 14.1 software. Delay, area and power parameters are calculated using this software. Performance parameters like delay, power of the existing system is 3.05ns, 31mW respectively.

Table I . performance analysis

Performance factors	SCPF CAM	PB-SCPF CAM
Delay (ns)	3.05	2.95
Power(W)	0.051	0.051

From the table I, We can examine that the delay has Reduced rather than the SCPF CAM . the main aim of the proposed system is to reduce dealy since it is has high importance in the field of communication as well as in the Internet routers. So the should be done in a Less amount of time.

ISSN2394-3777 (Print)
ISSN2394-3785 (Online)
Available online atwww.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 12, April 2018

Then only an efficient system can be Formed. in the case of power also. there is no sudden increase even though an extra bit is added to the system The same goes for the area also

Table II. Area

components	SCPF CAM	PBSCPF CAM
Slice register	52	18
LUT	56	23
Flipflops	3	2

From the table analysis given above we can clearly see the Difference in the resources used by the both systems .

IV.CONCLUSION

CAM has wide range of applications which requires high speed search . A SCPF-CAM structure is proposed for highspeed applications which exhibits the least ML delay among the compared designs. The proposed scheme e. uses the idea of parity bit computation along with SCPF-CAM. it can reduces the Power consumption as well as the increases the speed of the operation. verified the simulation results of the existing system using Modelsim software in VHDL software and also found the performance parameters. A part of the proposed system is also simulated and also verified

ACKNOWLEDGMENT

I express my sincere thanks to my guide Ms. Rachana M K .for her valuable guidance and useful suggestions, which helped me throughout this work.

REFERENCES

[1] K. Pagiamtzis and A. Sheikholeslami, (2006)—Content-addressable memory (CAM) circuits and architectures: A tutorial and survey,‖ IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 712–727.

[2] V. M. Zackriya and H. M. Kittur,(2013) —Selective match-line energizer content addressable memory (SMLE-CAM),‖ Int. J. Appl. Eng. Res., vol. 8, no.

[3] Bremler-Barr and D. Hendler,(2012) —Spaceefficient TCAM-basedclassification using gray coding,‖ IEEE Trans. Comput., vol. 61, no. 1, pp. 18–30,

[4] P.-T. Huang and W. Hwang, (2011)—A 65 nm 0.165 fJ/bit/search 256 × 44TCAM macro design for IPv6 lookup tables,‖ IEEE J. Solid-State Circuits, vol. 46, no. 2, pp. 507–51.

[5] N. Mohan and M. Sachdev, (2004)—Low power dual matchline content addressablememory,‖ in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), vol. 2, , pp. 633–636.

[6] C. A. Zukowski and S.-Y. Wang, (1997)—Use of selective precharge for lowpower contentaddressable memories,‖ in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), vol. 3, pp. 1788–1791.

[7] H. Jarollahi, V. Gripon, N. Onizawa, and W. J. Gross, (2015)—Algorithm and architecture for a low-power content-addressable memory based on sparse clustered networks,‖ IEEE Trans. Very Large Scale Integr. (VLSI)Syst., vol. 23, no. 4, pp. 642–653,

[8] H. Miyatake, M. Tanaka, and Y. Mori, (2001)—A design for high-speed lowpower CMOS fully parallel content-addressable memory macros,‖ IEEE J. Solid-State Circuits, vol. 36, no. 6, pp. 956–968.

[9] S.-J. Ruan, C.-Y. Wu, and J.-Y. Hsieh,(2008) —Low power design of precomputation-based content-addressable memory,‖ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 3, pp. 331–335

[10] S.-J. Ruan, C.J. Wuh (2003)—A low-power precomputation-based fully parallel contentaddressable memory,‖ IEEE J. Solid-State Circuits, vol. 38, no. 4, pp. 654–662,

[11] K. Maurya and L. T. Clark,(2011) —A dynamic longest prefix matchingcontent addressable memory for IP routing,‖ IEEE Trans. Very

ISSN2394-3777 (Print)
ISSN2394-3785 (Online)
Available online atwww.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 12, April 2018

Large Scale Integr. (VLSI) Syst., vol. 19, no. 6, pp. 963–
972,

AUTHORS

Vinny.P.B, currently pursing PG in VLSI Design from IES college of Engineering, Thrissur, Kerala, India. Shereceivedher B.Tech and Communication from SNMIMT,Maliankara, Thrissur, kerala, India in 2015.Her interested research areas are low power VLSI design and digital system design

Ms.Rachana M.K., currently working as Assistant Professor in Department of Electronics and Communication Engineering at IES College of Engineering, Thrissur, Kerala, India. She received her B.Tech. in Electronics and Communication Engineering from Cochin university of Science and Technology in 2005 and M.E degree in VLSI Design from Anna University, Chennai in 2015. Her research interests are VLSI Design and Embedded System Design. [1]