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Enhancement of power quality using multiple output SMPS based Zeta converter

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Abstract—Multiple output Switched Mode Power Supplies (SMPSs) for personal computers (PCs) normally depict extremely bad power quality indices at the utility interface such as total harmonic distortion of the input current being more than 80%, power factor being lower than 0.5 and output voltage regulation being very poor. So, they violate the limits of harmonic emissions set by international power quality standards. In this paper, a non-isolated power factor corrected (PFC) converter is being proposed to be used at the front end to improve the power quality of an SMPS for a PC. The front end converter is able to reduce the 100 Hz ripple in its output that is being fed to the second stage isolated converter. The performance of the front-end Zeta converter is evaluated in three different operating conditions to select the best operating condition for the proposed SMPS system. The performance of the proposed SMPS is simulated and a laboratory prototype is developed to validate its performance. Test results are found to be in line with the simulated performance under varying input voltages and loading conditions and all the results demonstrate its enhanced performance.

Index Terms --Power factor corrected Zeta converter, unity power factor, power quality, SMPS, multiple outputs

I. INTRODUCTION

N the present era, personal computers (PCs) have become a increases if these PCs are used in large numbers which creates serious problems like overloading the neutral conductor, noise, de-rating of the transformer, voltage distortion etc. [3-5]. To end these problems, improved PQ SMPSs that are capable of drawing a sinusoidal input current at unity power factor (UPF) and yielding stiffly regulated output voltages, are extensively being researched. Employing various power factor corrected (PFC) single-stage and two stage converters effect a perceivable PQ improvement in these SMPSs [6-10]. PQ improvement is visible in the form of low total harmonic distortion (THD) in the ac mains current and power factor being close to unity at the point of common coupling (PCC). This is achieved even under varying loads and supply voltage conditions. In a single-stage SMPS, ac supply is connected to a DBR whose output is processed by a multi-output PFC isolated dc-dc converter for obtaining dc voltages. The reliability of this single-stage SMPS is good; however, the output capacitors used are of very high value to reduce the 100 Hz ripple content. So, the rating of any single-stage SMPS is limited to about 200 W to avoid prohibitively high capacitance value. For medium power ratings, two stage SMPS is a commonly accepted solution in the SMPS market for PCs. The first stage is meant for improving the power quality at the PCC and for I part of our day to day activities from business to education to infotainment. Switched Mode Power Supply (SMPS) is an integral part of the computer that converts ac to multiple numbers of suitable dc voltages to impart power to different parts of the PC. It contains a diode bridge rectifier (DBR) with a capacitor filter followed by an isolated dc-dc converter to achieve multiple dc output voltages of different ratings. The uncontrolled charging and discharging of the capacitor result in a highly distorted, high crest factor, periodically dense input current at the single phase ac mains; this violates the limits of international power quality (PQ) standards such as IEC 61000-Ultrasonic ranging module HC - SR04 provides 2cm - 400cm non-contact measurement function, the ranging accuracy can reach to 3mm. The modules includes ultrasonic transmitters, receiver and control circuit. The basic principle of work Using IO trigger for at least 10us high level signal. The Module automatically sends eight 40 kHz and detect whether there is pulse signal back. IF the signal back, through high level , time of high output IO duration is the time from sending ultrasonic to returning. Test distance = (high level time× velocity of sound (340M/S) / 2. Figure 3 shows the image for Ultrasonic sensor stage. The selection of operating mode of the front end converter may be in Discontinuous Conduction Mode(DCM) if the cost is a major consideration; if not, Continuous Conduction Mode (CCM) is adopted that reduces device stresses, despite the fact that CCM uses two voltage and one current sensors which naturally makes it costlier. Therefore, a DCM operation of the front end PFC converteris referred in PCs where only one voltage sensor is needed for sensing and control. A boost converter is a common choice as a PFC in various industrial applications. However, it cannot be used if a wide range of ac mains voltage is to be taken care of [11]. Similarly, due to limited output voltage range buck converters are not preferred for computer power supply [12]. Non-isolated buck- boost PFC converter configurations are the best suited for maintaining a constant dc output voltage irrespective of wide variations in ac supply voltages. Different buck-boost converters configurations and their application to SMPS are reported in the literature [13-19]. A conventional buck-boost converter has a low component count. However, the output current is pulsating in nature which increases the ripple in voltage. The buck-boost Cuk converter is not preferred due to the polarity of the output being reversed which gives rise to various design issues. SEPIC also depicts a pulsating output current. As the output stage of the power supply is very sensitive, this pulsating current is not desirable. The fly

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back converter suffers from leakage inductance problem which imposes a limit on its rating. To eliminate these issues, a Zeta PFC converter is employed as a PFC converter in many research papers. It provides a continuous output current with a low ripple output voltage along with a high level performance which is highly recommendable for PCs. The dynamic modeling of the Zeta converter is carried out using state space averaging technique in [20-24]. The suppression of lower order harmonic content leads to reduction in EMI of a PFC ac- dc converter operating in DCM as discussed in [25]. An isolated converter is required at the output for yielding multiple dc output voltages in an SMPS for PCs. An isolated half-bridge dc-dc converter is preferred here because of excellent core utilization and less device stress [26-29]. This paper presents power quality improvement in a multiple output SMPS that yields regulated dc output voltages irrespective of line and load variations. A Zeta PFC converter is still unexplored for the development of computer SMPSs that are capable of drawing a purely sinusoidal current with unity PF, offering low rippled output which is the prime requirement of PCs. In this work, three different operating modes of the Zeta converter have been analyzed and compared to select the best operating mode for a computer power supply application [23-24]. The proposed SMPS is designed, modeled and simulated in MATLAB/ Simulink platform [30] to validate the design. Then, an experimental prototype is built in the laboratory and tests are conducted on it. The recorded test results on the developed prototype are in line with the simulation results confirming the validity of the design.

II. PROPOSED PFC ZETA CONVERTER BASED SMPS CONFIGURATION

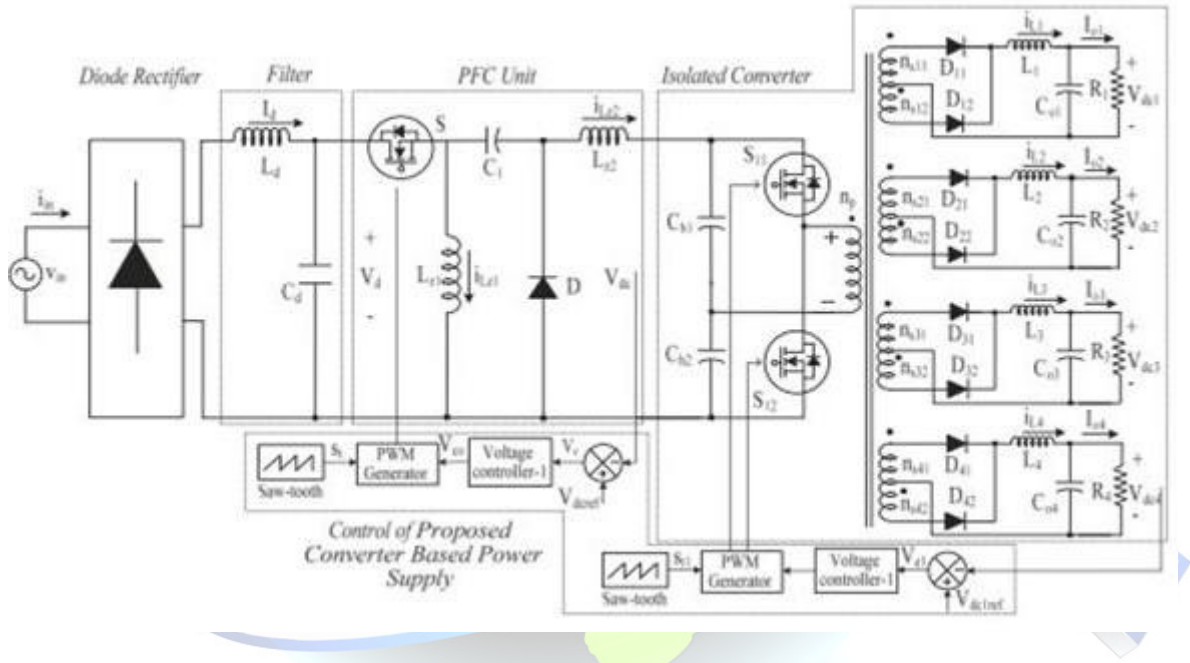

Fig. 1 shows the system configuration of a PFC Zeta converter based multi-output SMPS topology. At the input, a DBR with filter is connected to a non-isolated Zeta converter. It consists of two inductors Lz1 and Lz2, one intermediate capacitor C1, one high frequency switch S and one diode D. This PFC converter regulates the output dc voltage and draws a sinusoidal current from the ac mains at unity PF. Three different DCM conditions (i.e. input inductor DCM, intermediate capacitor DCM and output inductor DCM) are considered here to choose the best operating condition of the front end PFC converter. In the DCM operation, the current becomes zero either in the input inductor or output inductor, or the voltage across the intermediate capacitor becomes zero for some duration in one switching cycle. The output dc voltage is regulated using a Proportional-Integral (PI) voltage controller. The regulated output dc voltage is connected to an isolated converter for achieving multiple dc voltages at the output. The isolated converter consists of two equal valued input capacitors, two switches, one high frequency transformer (HFT) and filters. The filters are used in each output winding to reduce the output voltage and current ripples. Only one of the output voltages is directly sensed and the other output voltages are controlled by the duty cycle of the isolated converter. The winding that is selected for control action is of the largest power rating among all the outputs. Further, to reduce the component stresses, the isolated converter is designed in CCM. Another voltage PI controller is used here to regulate the output voltage. The performance of the proposed PFC Zeta converter based SMPS is demonstrated for a wide variation in the input voltages from 170V to 260V and loads with the input power quality indices recorded for each of these operating conditions.

III. OPERATING PRINCIPLE OF THE PROPOSED SMPS

The operation of the proposed SMPS is studied to analyze its behaviour in one switching cycle. Three different conditions (input inductor in DCM, intermediate capacitor in DCM, output inductor in DCM) have been considered for

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the PFC Zeta converter to select the best operating condition. A. PFC Converter Operation When Input Inductor is in DCM

Fig. 2 shows the operation of a PFC Zeta converter when the input inductor is in DCM. The current in the input inductor remains zero for some time in one switching cycle while the current in the output inductor and voltage across the intermediate capacitor remain non-zero.

1) Mode I: When the PFC switch S turns on, the current in the input inductor Lz1 and output inductor Lz2 start increasing and the voltage across the capacitor starts decreasing.
2) Mode II: When S is turned off, diode D starts conducting as shown in Fig. 2(b). The stored energy in Lz1 starts decreasing and continues until the current iLz2 equals the negative of the current iLz1. The voltage across the intermediate capacitor C1 starts increasing.
3) Mode III: Both switch S and diode D are off in this period of one switching cycle as shown in Fig. 2(c). This state lasts until the start of the next PWM cycle. The input inductor current iLz1 remains zero ensuring the DCM condition.

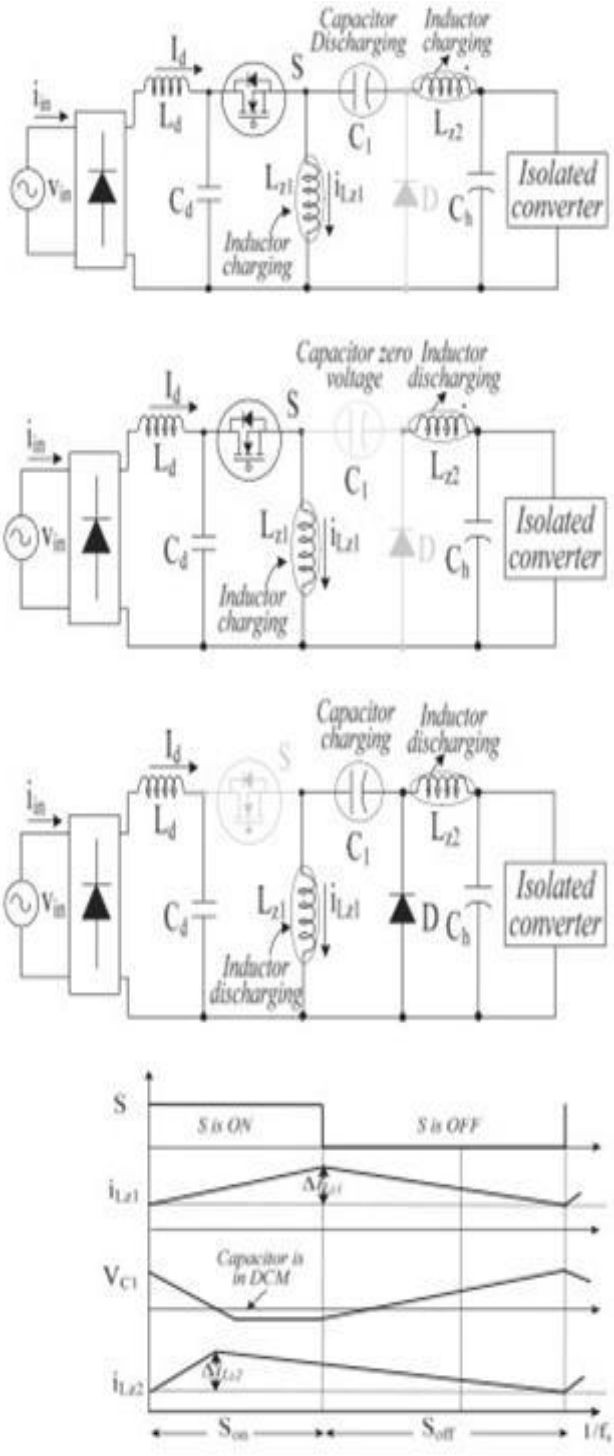

Fig. 2. Operating modes of the PFC Zeta converter in one switching cycle when Lz1 is in DCM, (a) When input inductor is charging, (b) When input inductor is discharging,

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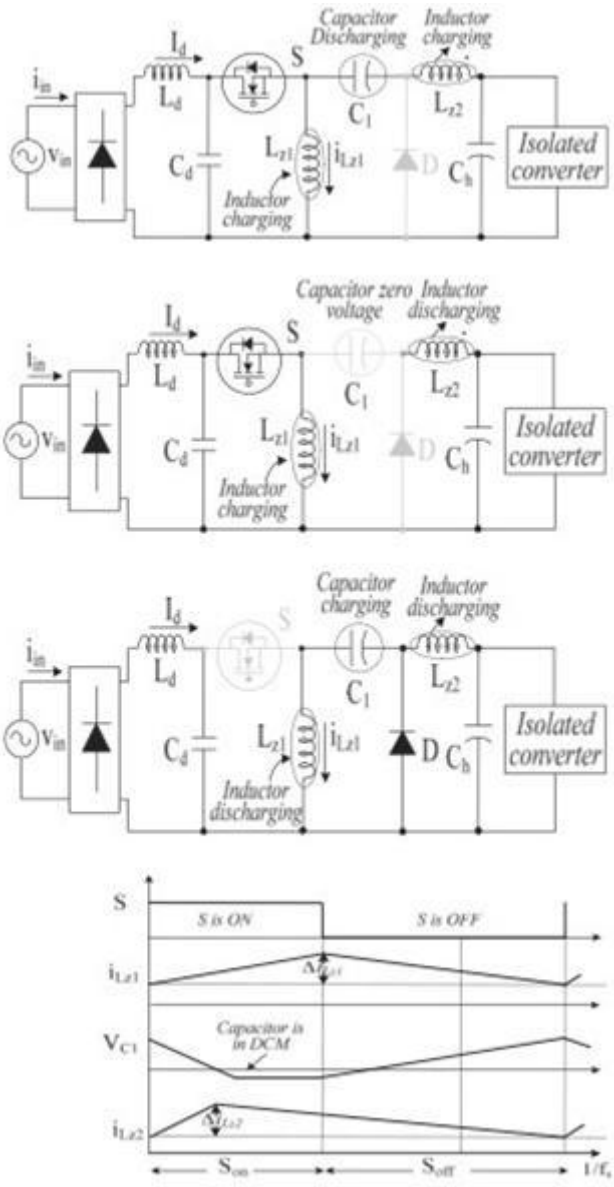
(c) when input inductor is in zero current mode, (d) Waveforms of various components in one switching cycle B. PFC Converter with Intermediate Capacitor in DCM The operation of a PFC Zeta converter, when the inter mediate capacitor is operating in DCM, is shown in Fig.3. The three switching states are described as follows:

1) Mode I: When switch S turns on, the currents in inductors Lz1 and Lz2 are increasing while the intermediate capacitor discharges through the output inductor Lz2; the voltage across the output capacitor increases.
2) Mode II: In this mode, switch S is in conduction state but the intermediate capacitor C1 is completely discharged and the voltage across C1 becomes zero. In this condition, output inductor Lz2 continues to supply energy to the output capacitor.
3) Mode III: Switch S now turns off, input inductor Lz1 is discharging through the intermediate capacitor. The output inductor Lz2 is discharging through the isolated converter while maintaining continuous conduction.Fig. 3. Operating modes of the PFC Zeta converter in one switching cycle when C1 is in DCM (a) When capacitor is discharging, (b) When capacitor is in zero voltage mode, (c) When capacitor is charging, (d) Waveforms of various components in one switching cycle

C. PFC Converter with Output Inductor in DCM The DCM operation of the output inductor in one switching cycle is shown in Fig. 4. The output inductor is designed in DCM and therefore, the current in the output inductor remains zero for a certain time period in one switching cycle. The different modes of conduction in one switching cycle are described as follows.

Mode I: The PFC switch S turns on; the input voltage supplies energy to inductor Lz1. The intermediate capacitor discharges through the output inductor Lz2. The currents in Lz1 and the output inductor increase linearly.

Mode II: The switch S turns off and diode D turns on as shown in Fig. 4(b). The stored energy in Lz1 is transferred to the capacitor C1; the output inductor energy is fed to the isolated converter. This stage continues until the current iLz1 equals the negative of the current iLz2.



Mode III: The switch and diode both are off in this duration of one switching cycle as shown in Fig. 4(c). This state lasts until the start of the next PWM cycle. The output inductor current remains zero in the remaining time ensuring the DCM condition.

B. Performance of Proposed SMPS under Varying Input Voltages Fig. 10 shows the recorded test results of the proposed SMPS under rated load and input voltage conditions which show that the PF is unity with THD of input current being 2.9%. Fig. 11(a) shows the input voltage, input current and the output voltage of the Zeta converter along with the output current. The output voltage is maintained constant due to closed loop control. The output voltages of the second stage converter i.e., +5V output and +3.3 V output along with their input current is reduced and it is maintained sinusoidal with unity PF. The THD of ac mains current at light load is observed as 4.5% as shown in Fig. 14(c) which adheres to the limit set by IEC standard [1]. Thus, a satisfactory performance with acceptable input current THD is obtained at the ac mains varying input voltages and loads. Both the voltages are regulated stiffly to the specified values. Fig. 11(d) shows the test results of the

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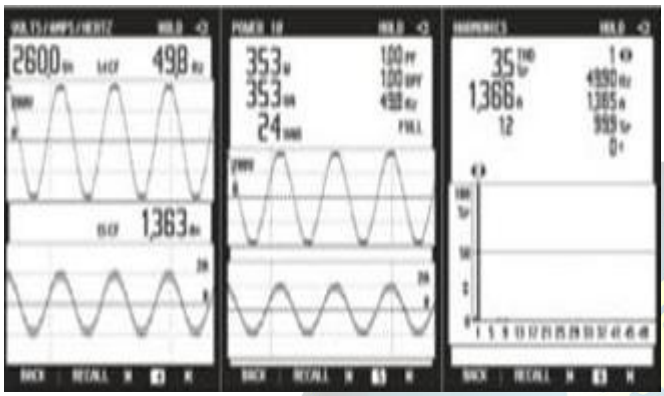
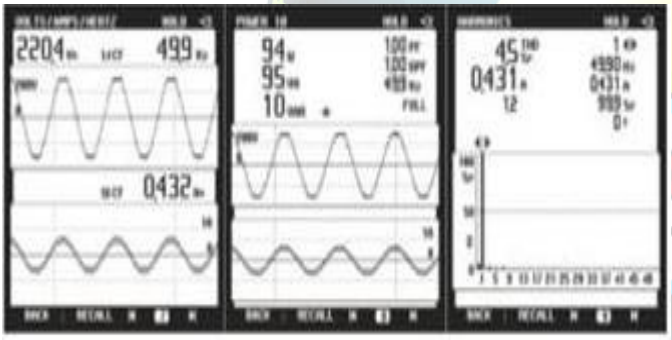
input inductor current which is maintained in CCM while the output inductor current touches zero in each PWM cycle maintaining DCM asshown and the enlarged view is shown in Fig. 11(f). The capacitor voltage, input voltage and current are shown in F. simulated results of the proposed SMPS. The maximum voltage and current of the switch are shown in Fig. 11(h) which shows that the voltage stress is 580V which is acceptable for a 220V input voltage. Test results of the proposed power supply during wide input voltage variations are shown in Figs. 12 and 13. The THD of the input current at 170V and 260V are respectively 2.3% and 3.5% and PF is unity as shown in Table-III falling within the IEEE-519 standard limit.





IV. CONCLUSION

A DCM operated front end PFC converter cascaded with a multiple output isolated converter has been used for the design. of an SMPS for PCs. It has been designed, modeled, simulated and developed for input power quality improvement and output voltage regulation. All the dc output voltages are regulated by controlling only one output voltage. Three different modes of operation of the front end converter have been carried out in simulation to select the best possible operation especially based on device stresses. Finally, the best suited mode of operation for the front end converter has been implemented in an experimental prototype. Test results obtained from the prototype conform to the ones obtained via simulations. From the recorded test results, it is evident that the proposed power supply is able to mitigate power quality problems that are present in the conventional SMPS systems. Based on these results, it is concluded that the proposed SMPS configuration in PCs is expected to yield improved THD of ac mains current with almost unity PF under wide range of input voltages and loads The voltage ripple calculated is 9.39V which is higher than the one calculated for the proposed SMPS for the same value of capacitor.

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