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Implementation of 32nm FINFET Dynamic Comparator for Flash type ADC

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Abstract-- In order to reduce the circuit complexity and area, the simple arrangement of the dynamic comparator is designed. Power consumption is the important parameter in VLSI circuits. To reduce the power consumption of the circuit many methods are proposed in the past. A FINFET comparator using dynamic latch, suitable for high-speed Analog-to-Digital Converter (ADC) with high speed and low power dissipation is presented. This design is planned to be proposed in Flash type ADC. This circuit combines the good features of the resistive isolating comparator and the differential current sensing comparator. The design has been carried out in LT SPICE and HSPICE using 32nm FINFET technology. The Simulation results are verified with supply voltages of 1.6V, 1.8V and 2.0V respectively. In Existing result shows that the power is least dissipated in 1.6V which is 0.7899 mW, but it has the longest propagation delay of 0.715 ns. In contrast, the 2.0V supply produced 1.471 mW and a shorter delay of 0.550 ns.

Index Terms— Dynamic latch comparator, Flash ADC, FINFET, differential current sensing comparator.

I. INTRODUCTION

The term FinFET explain a non-planar, double-gate electronic transistor engineered on associate SOI substrate. The distinctive feature of the FinFET is that the conducting channel is wrapped by a slender semiconductor "fin" that forms the body of the device and the fin thickness determines the effective channel length of the device [1]. A FINFET structure has been shown in fig.1 which depicts the gate and channel arrangements between source and drain in FinFETs. A number of material can be used to from substrate and channel. Here, Indium-Gallium-Arsenide to form p-type substrate FinFETs were introduced to overcome the Short Channel Effects(SCE) and they are having some distinct characters that makes it different from earlier FETs.

The essential building block of many analog circuits is the comparator, especially in Analog to Digital converters. Its interface between digital and analog domain often defines the resolution and speed of the entire ADC. There are many proposed topologies on how the technology should be distributed which aim to minimize the power consumption and maximize the data transfer [2].

Now a day's mostly we are using Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) circuits because of the need to translate analog signal to digital signal and vice versa. A comparator plays a basic role in most electronic applications. Due to the large number of comparisons in some ADC structures, such as flash ADCs, the speed and the power consumption of the comparator have important influences on the performance of ADC [3]. High speed ADC is the key component in the area of analog and/or digital interface with the increasing demands for a high speed ADC. At the same time, the speed of the comparator is the main factor to the speed of the ADC [4]. A high speed ADC is very critical in some digital system and with the requirement to prolong the battery life of the system; a comparator with low power consumption is needed. There are many types of ADC available nowadays, example like Flash ADC, Sigma Delta ADC, dual slope converter an successive approximation converter. There is a trade-off between speed and resolution, for which literature has presented different techniques to enhance the performance of a comparator.

One of the more advanced ADC technology is the Sigma Delta ADC or ΔΣ. Sigma Delta is one of the analog to digital converters which are ideally for converting signals over a wide range of frequencies from direct current to several megahertz with a very high resolution results. This paper proposes and demonstrates the analysis and design of a dynamic latch comparator. Its design pursues a high resolution at a considerable speed by optimizing the design of the amplifier and the latch. The proposed preamplifier extensively decreases the effects of the offset voltage errors due to device mismatch. Also, the topology isolates the latch and the input nodes. This prevents any trouble due to the kickback noise. The proposed latch is designed to achieve the lowest time constant limited by our topology using the study presented in [9] [10]. The signal path between the preamplifier and latch is controlled by transmission gates which as shown in [11] provide an additional gain at the output signal of the amplifier due to the charge insertion phenomenon.

The Analog to Digital Converter(ADC) converts the mean of an analog voltage into the mean of an analog pulse frequency and counts the pulses in a known interval so that the pulse count separated by the interval gives an perfect digital representation of the mean analog voltage during the interval. This intermission can be chosen to give any desired resolution

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or accuracy. The method is cheaply produced by modern methods; and it is widely used.

In sigma delta modulation, the analog signal is quantized by a one-bit comparator. output of the comparator is changed back to an analog signal with a 1-bit DAC, and subtracted from the input after passing through an integrator. Thus, a good comparator design is the focused of this paper.

II. STUDY OF FINFET

Scaling is one of the key factor of any new technology and it governs the design metrics of the complete technology. With the scaling up to sub-micro region, single-gate MOSFETs has served the purpose but as designing moves down in ultra sub-micro region, the further scaling of single gate MOSFETs leads to a number of Short Channel Effects which directly affects the various performance criteria and to resolve these effects, Multi-gate MOSFETs are designed and one of the most widely used and efficient is FinFET. FinFET is classified as a type of multi-gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET). A multi-gate transistor incorporates more than one gate in to one single device. In FinFET, a thin silicon film wrapped over the conducting channel forms the body. The name has been derived from the fact that the structure, when viewed, looks like a set of fins. The thickness of the device determines the channel length of the device. The channel length of a MOSFET is said to be the distance between the source and drain junctions. It is a non-planar, double gate transistor which based either on the Bulk Silicon-On-Insulator (SOI) or on silicon wafers . It is based on the single gate transistor design. It is based on the single gate transistor design. There are two types of FinFets:

1. Bulk FinFet
2. SOI FinFet

The 'types' of finfets are nothing but the 'base' onto which it is fabricated. This means that FinFets can be made either on SOI wafers or regular silicon wafers.

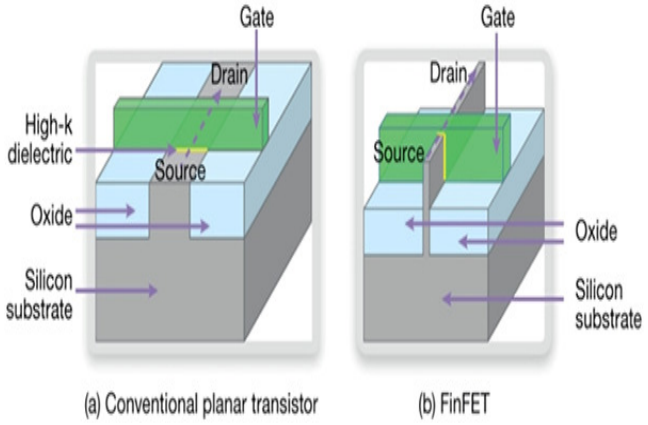

Fig. 1: FinFET

The gate of the FinFet is wrapped around (a wrap-around gate) which reduces leakage current thereby increasing effectiveness. Since the fabrication of MOSFET, the channel length of the device has been shrinking constantly so as to fabricate compact and fast devices. The following parameters related to MOSFET highlight the need for smaller, compact devices and explain why the MOSFET is not the suitable choice for the same. The shorter section of the gate electrode is known as the length and the longer section is called the width. As the channel length of a MOSFET reduces, the short-channel effects increase.

III. MATHEMATICAL ANALYSIS

A. *Propagation Delay*

Propagation delay is the time required by the input to produce the corresponding change in the output signal [4, 5]. The propagation delay in the comparator generally varies as a function of the input. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. A larger input voltage will result in a smaller delay time. the propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. The propagation delay of a comparator can be express as in equation (1):

$$\text{Propagation delay} = (\text{tplh} + \text{tphl})/2 \quad (1)$$

Where

tphl = delay time when output change from high to low
tplh = delay time when output change from low to high

B. *Speed*

Speed is the inverse of the propagation time delay. The speed of a comparator can be calculated using equation (2):

$$\text{Speed} = 1/(\text{propagation time delay}) \quad (2)$$

C. *Power Dissipation*

Power dissipation is the rate at which energy is dissipated from electrical circuits. It is measured in watts. Dynamic comparator power dissipation is given approximately by equation (3):

$$\text{Power} = f \times C \times V_{DD}^2 \quad (3)$$

Where

f = output frequency
V_{DD} = the supply voltage
C = output capacitance

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For high frequency circuit operation, the trade-off must be made between speed and power dissipation. Speed will be mainly affected by the slew rate requirements and load impedance. The lower the load resistance, the more current will be needed to achieve the desired speed of operation. The gain of the comparator will influence the speed and the power dissipation. The gain can be increased by increasing the power supply voltage.

IV PROPOSED DESIGN

In the future circuit, the proposal is to combine the charge sharing comparator and output buffer circuit. The comparator combines the features of both the resistive dividing network and differential current sensing comparator. Therefore, the comparator consists of two stages. Figure 2 shows the charge sharing topology for the dynamic latch comparator circuit.

In Figure 3, resistive comparing circuit for regenerative mode is used in series with DGNMOS transistor DGNMOS_9 in order to get a low power consumption. Besides that, DGPMOS transistor for pre charging circuit is absent during reset mode and DGNMOS transistor DGNMOS_1 for output pass transistor is nearly to Vdd/2 for the equalization of both voltage. The latch now is disconnected from Vdd and ground with the aid from transistor DGPMOS_1 and DGNMOS_9.

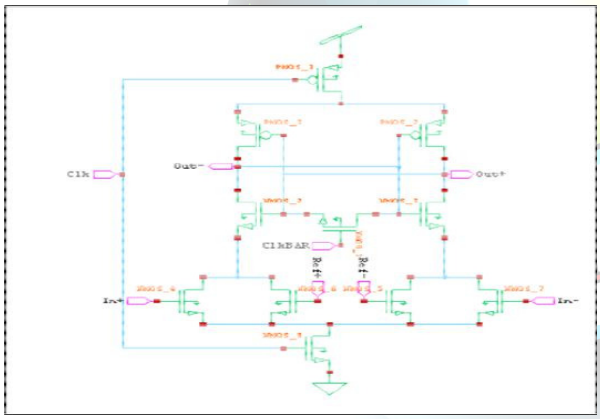

Fig. 2: Charge sharing topology for dynamic latch comparator

Figure 3 he output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. The digital output converts the output of the latch stage to a full scale digital level output (logic 1 or logic 0). The output buffer stage should be able to accept a differential input signal (Out + and Out-from the charge sharing shows the output buffer circuit. This circuit is also known as post amplifier. Basically, the circuit receives the information from the latch and produces a digital output signal. T circuit and will not have slew-rate limitations.

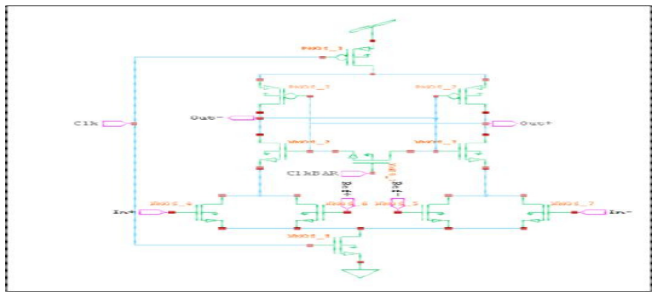

Fig. 3: Output buffer circuit

V. SIMULATION AND RESULT

The schematic of the dynamic latch comparator is shown in Figure 4 which consists of both stages which are the dynamic charge sharing comparator along with the output buffer stage.

Now, the two ended output of dynamic charge sharing comparator (Out+ and Out-) in Figure 2 become the input to the buffer circuit in Figure 4. Thus, making the two ended output of dynamic charge sharing comparator is being converted into single ended output which is labelled as output.

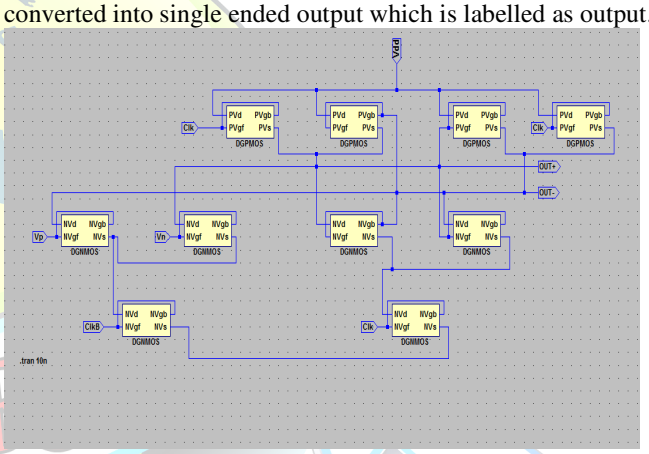

Fig. 4: Proposed dynamic comparator circuit

Transistor sizing is important in ensuring the correct output of the comparator [6]. Table 1 shows all the sizing of the transistors used in this design. It is based on FINFET technology of 32nm The right sizing is critical and will also affect the speed of the circuit. The preamplifier was designed to achieve a high gain-bandwidth product. Its specifications were, a high gain at 40MHz, consuming less than 500µW and low variance in the threshold voltage. For the latch, since the speed was limited by the amplifier bandwidth, larger transistors were designed to mitigate the effects of the variability between the thresholds voltages.

Table 1. Transistor dimension (µm) of the dynamic comparator circuit in Figure 4.

Transistor	**Technology** 32nm
M1, M4, M5, M7, M10, M11	5
M2, M3	10

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M6, M13, M14, M16, M18, M20	8
M8, M9, M12, M15, M17, M19, M21	4

The circuit in Figure 3 is tested with a supply voltage of 2.0V, 1.8V and 1.6V respectively. The reference voltage is +1 V and -1 V.

A. Transient Analysis

For the transient response, the input voltage sources (In+ and In-) are a pulse voltage sources and the reference voltage sources are a DC voltage sources. The input signal is compared with the reference voltage during evaluation mode (Clk = 1). When the input signal voltage (In+ or In-) is greater than the reference voltage (Ref+ or Ref-), the output (Out+ or Out-) is high and vice versa. Besides that, it is also found the output (Out+ and Out-) nodes are 180˚ (degree) out of phase to each other. The comparator converted the input voltage (V_{IN}) into logic "1" or "0" by comparing the VIN with a reference voltage (V_{REF}). If V_{IN} is greater than V_{REF} the output is "1'', otherwise it is "0".

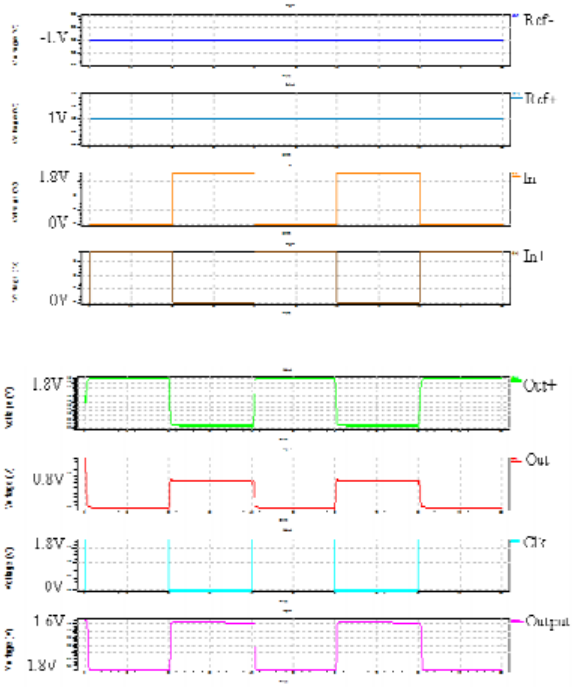

Fig. 5. Transient response of dynamic comparator circuit using power supply of 1.6V.

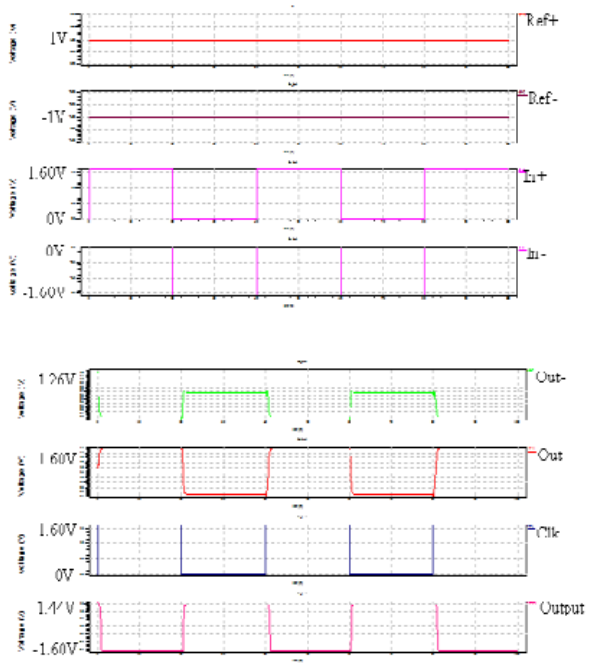

Fig. 6. Transient response of dynamic comparator circuit using power supply of 1.8V.

Figure 5, 6 and 7 show the transient response of the designed comparator using 32nm FINFET technology, for a 2.0V power supply, 1.8V and 1.6V respectively. The results show that the comparator is working perfectly even though different power supply is applied. As compared to the result in [7], the proposed circuit can work better because it can be operated with a power supply as low as 2.0V with a correct output and using a smaller FINFET technology.

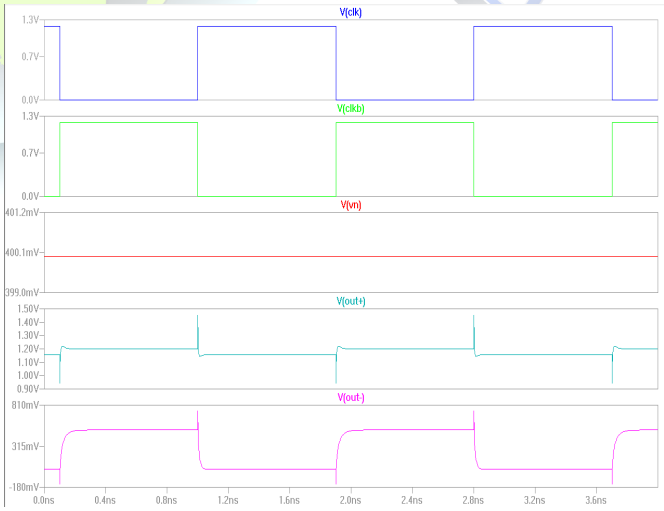

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Fig. 7. Transient response of dynamic comparator circuit using power supply of 2.0V

B. Delay Analysis

Figure 8, 9 and 10 prove the delay in the output waveforms with different power supply. Table 2 shows the comparison of the propagation delay obtained from the delay analysis done on each power supply.

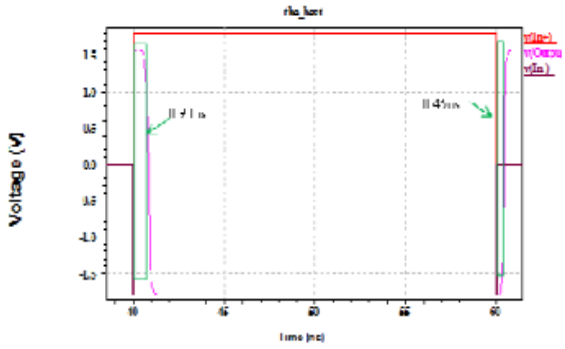

Fig. 8. The output waveform when power supply is 1.6V

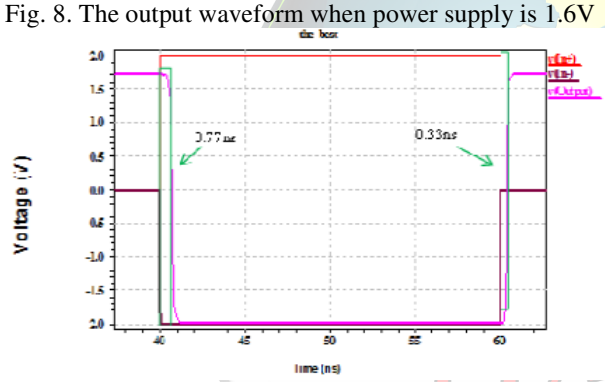

Fig. 9. The output waveform when power supply is 1.8V

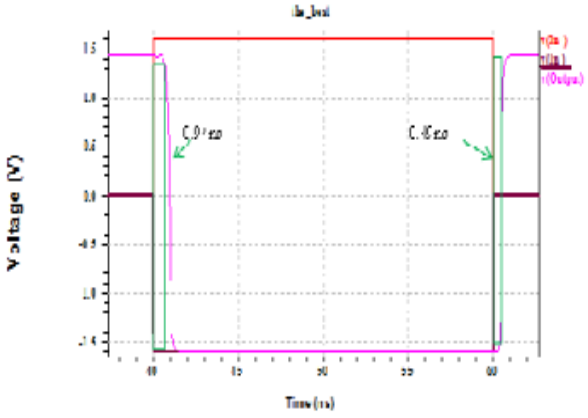

Fig. 10. The output waveform when power supply is 2.0V

Table 2. Comparison of the propagation delay using different supply voltage

Power supply (V)	output		Propagation delay (ns)
	tplh (ns)	tphl (ns)	
2.0	0.33	0.77	0.550
1.8	0.45	0.90	0.675
1.6	0.49	0.94	0.715

As expected, it is found that a higher power supply voltage will result in a smaller delay time as shown in Figure 9.

C. Power Analysis

The power (P) drawn from the power supply is proportional to the supply current and the supply voltage. From Table 3, it is found that the power dissipation is least when the power supply used is 2.0V. As expected, the value is higher when a lower power supply is used.

Table 3. Power dissipation of comparator with different power supply

Power supply (v)	Power dissipation (mW)
2.0	0.7899
1.8	1.2293
1.6	1.4709

VI. LAYOUT OF THE COMPARATOR

The layout of the complete low power dynamic latch comparator circuit using 32nmis shown in Figure 11. This layout minimizes the area by sharing the drain and source connections between FINFET. By doing so, the final area size for the circuit is very small and compact. Figure 11 shows the layout versus schematic (LVS) result. The LVS result verified that the layout and the schematic circuit are equal.

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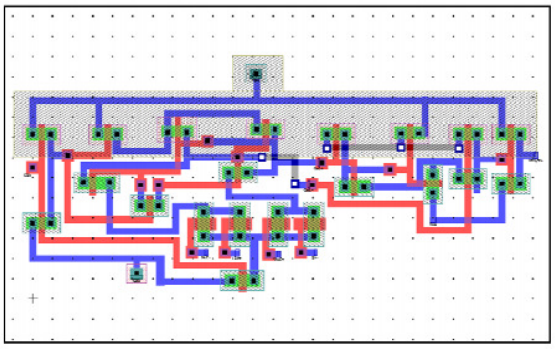

Fig. 11 .Layout of Dynamic Latch comparator

VII. CONCLUSION

The speed and the power consumption of the comparator have important influences on the performance of ADC. Both are equally important, but usually user cannot get these two parameters hand in hand. It is found from this research that the power dissipation is least with a 2.0V power supply, however the propagation delay also lower as compared to the other two power supplies. In conclusion, by using of LT spic, HSPICE simulation result will be done at the supply voltage of 2.0V. Further research and modification will be done on the circuit to lower the power consumption as the overall result of the power dissipation is slightly off than the targeted value.

REFERENCES

[1] Hu Chenming, "FinFET and other New Transistor Technologies", *seminar in University Of California*, July 2011.

[2] P. M. Figueiredo, and J. C. Vital. "Low kickback noise techniques for CMOS latched comparators", *Circuits and Systems International Symposium Proceedings*, pp.1-537-40 vol.1, 23-26 May 2004.

[3] G. Yongheng, C. Wei, L .Tiejun, and W. Zongmin. "A novel 1GSPS low offset comparator for high speed ADC", *5th International Joint Conference on INC, IMC and IDC, IEEE Computer Society, Seoul*, pp.1251-1254, 25-27 August 2009.

[4] M. Miyahara, Y. Asada, D. Paik and A. Matsuzawa. "A low-noise self-calibrating dynamic comparator for high-speed ADCs", *IEEE Asian Solid-State Circuits Conference*, 2008.

[5] W. Singh. "Study and design of comparators for high speed ADCs", *Unpublished thesis, University of Thapar, Patiala*. Retrieved from http://dspace.thapar.edu:8080/dspace/bitstream/10266/1654/1/ on 24th Febuary 2015.

[6] Lalit Madhab Dhal and Anshuman Pradhan. "Study and analysis of different types of comparators", *Unpublished thesis 2013, National Institute of Technology, Rourkela*. Retrieved from http://ethesis.nitrkl.ac.in/5184/1/ on 24th Febuary 2015.

[7] C. J. Solis, and G. O. Ducoudray. "High resolution low power 0.6µm CMOS 40 MHz dynamic latch comparator" *IEEE Transaction on Circuit and System*. pp. 1045-1048. DOI: 10.1109/MWSCAS.2010.5548824, 2010.

[8] P. Uthaichana and E. Leelarasmee. "Low power CMOS dynamic latch comparators," *TENCON 2003, Convergent Technologies for Asia Pacific Region Conference*, pp. 605-608, 2003.

[9] Worapishet, A.; Hughes, J.B.; Toumazou, C.; , "Double-regenerated switched-current comparator," *Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on* , vol.3, no., pp.1531-1534 vol.3, 1999.

[10] Matthews T.W "On the effective sampling time of regenerative comparators," *Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on* vol., no., pp.638-641, 10-13 Aug. 2008

[11] Sheikhaei, S.; Mirabbasi, S.; Ivanov, A.;"A 0.35 µm CMOS comparator circuit for high-speed ADC applications," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on* , vol., no., pp. 6134-6137 Vol. 6, 23-26 May 2005.

[12] Sarman K Hadia, Rohit R. Patel, Dr. Yogesh P. Kosta, "FinFET Architecture Analysis and Fabrication Mechanism", *International Journal of Computer Science*, Vol. 8, Issue 5, No 1, September 2011

[13] Revathy T R, "Double Tail Comparator Using FinFET", *International Journal of Modern Trends in Engineering and Research*, Volume 02, Issue 06, June – 2015

[14] Nagarathinam S, David S, "An Improved Comparator Structure For 8-Bit SAR ADCs : A Review", *International Journal of Pure and Applied Mathematics*, Volume 117 No. 8, 145-148, 2017

[15] Laxmi Kumre , N.V.Ramesh, "Design and Implementation of Flash Analog to digital Converter", *Elsevier, Proceedings* (2017) 2214-7853

[16] Manju Panwar, "A Review on Performance of Comparator in Analog to Digital Converter", *International Journal of Recent Development in Engineering and Technology*, Volume 6, Issue 2, February 2017

[17] Christophe Erdmann, Edward Cullen, Damien Brouard, Roberto Pelliconi, Bob Verbruggen, John Mcgrath, Diarmuid Collins, Marites De La Torre, Pierrick Gay, Patrick Lynch, Peng Lim, Anthony Collins, Brendan Farley, "A 330mW 14b 6.8GS/s Dual-Mode RF DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz", *IEEE International Solid-State Circuits Conference*, 2017

[18] Nizamuudin. M, "Simulation Study of Low Power Comparator for A-D Converter", *International Journal of Advance Research, Ideas and Innovations in Technology*, Volume3, Issue1, 2017

[19] Razavi.B, "Deign of Analog CMOS Integrated Circuits," *Tata McGraw-Hill*, Delhi, 2002.

[20] Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters" 2nd Edition, *Springer International Edition*.

[21] John F. Wakerly, "Digital Design Principles and Practices", 3rd Edition, *Pearson Education*.

[22] Douglas A.Pucknell & Kamran Eshraghian, "Basic VLSI Design", 3rd Edition, *Prentice Hall of India Pvt.Ltd*.