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Quasi-z-source based cascaded multilevel inverter and isolated dc/dc converters for distributed power generation

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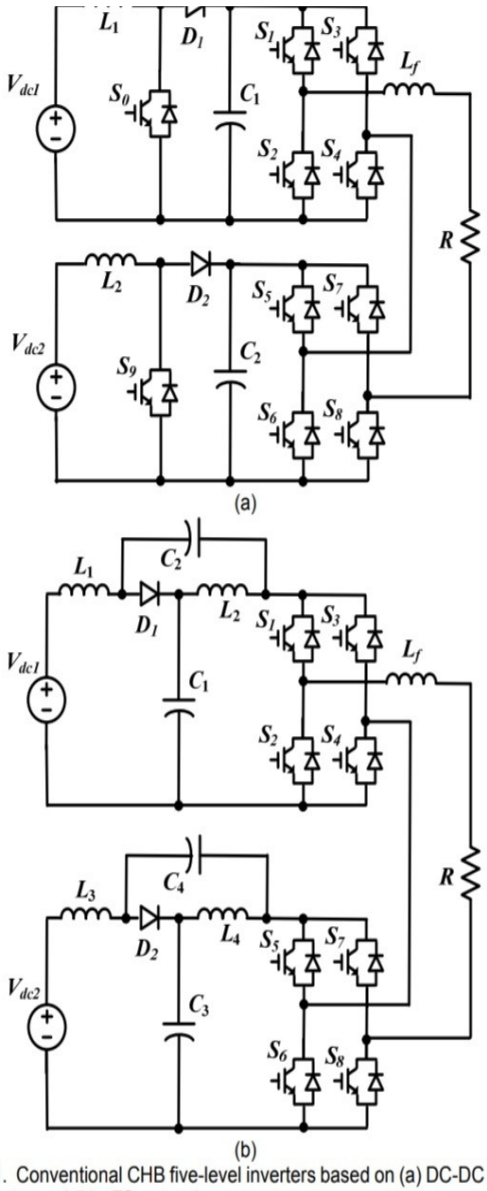
***Abstract*—Latterly, multilevel inverters have become more attractive for researchers due to low total harmonic output voltage and low electromagnetic interference (EMI). This paper proposes a novel single-stage quasi-cascaded H-bridge five-level boost inverter (qCHB –mL BI). The proposed multi-level inverter has the adventages over the cascaded H-bridge quasi-Z-source inverter (CHB-q ZSI) in cutting down passive components. To increase the output voltage level of the converter a new step up dc/dc converter, Voltage fed quasi- Z-source multilevel inverter with continuous input current on the primary side,1Φ isolation transformer and VDR are designed, which will reduce the THD for distributed power generation. Improve the voltage level with low harmonics. Reduce the total harmonic distortion. Improved efficiency. Reduce the cost.**

I. Introduction

Multilevel inverters have recently received many attentionsfrom researchers due to their advantages over the conventional three-level pulse-width modulation (PWM) inverters. The advantages of the multilevel inverters are as follows: improved quality output waveforms with lower total harmonic distortion (THD), smaller filter size and lower electromagnetic interface (EMI) [1]. Three general multilevel inverter topologies are: flying capacitors, neutral point clamped (NPC), and cascaded H-bridge (CHB) inverters. Among these topologies, the CHB inverter has unique advantages in modularity and its contribution of high power. These advantages make the CHB inverter an attractive option for many applications such as uninterruptible power supplies (UPS), grid-connected system, StatCom system, motor drive, etc. [2]–[11]. However, the traditional CHB multilevel inverter is a buck DC-AC power conversion, where the peak AC output voltage is limited by the total DC source voltages. In [12] and [13], an additional DC-DC boost converter is demanded for each module in the CHB topology to achieve the high AC output voltage when the DC input voltages are low. Adding DC-DC boost power converter results in low efficiency andhigh cost. Fig. 1(a) shows the conventional two- stage CHB boost- buck/boost voltage. However, the CHB-qZSI in [15]-[23] and the AFE-CHB inverter in [24] use a large number of passive elements with raising the size, cost, and weight of the power cascaded system.

A quasi-switched boost (qSB) network in [25]-[27] is used to replace the qZS network. In comparison to the qZS network, the qSB network uses one less capacitor, one less inductor, one more diode and one more switch in front of the main H-bridge circuit. An isolated high



ig. 1. Conventional CHB five-level inverters based on (a) DC-DC boost converter and (b) qZS network.

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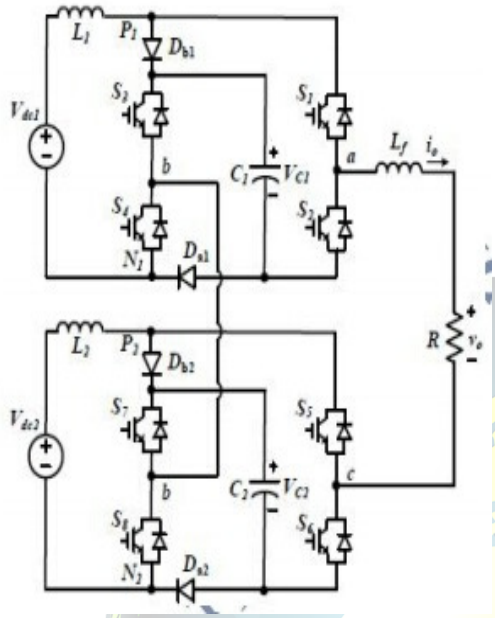


five-level inverter (CHB-BFLI) [12]. Two capacitors, two boost inductors, two diodes, ten switches, one filter inductor and a resistive load are utilized in the conventional CHB-BFLI. The boost DC-DC converter is used to control the DC-link voltage on each H-bridge circuit. As shown in Fig. 1(a), both the top and bottom switches in the same leg cannot be switched on simultaneously because the DC-link capacitor is connected to each leg in parallel. And a dead-time between two switches in the leg must be used to avoid short circuit in the DC source [14].

CHB quasi-Z-source inverter (qZSI) with single-stage power conversion was proposed in [15] and [16]. Fig. 1(b) shows the CHB five-level qZSI [15], where a qZS network with two capacitors and two inductors is connected to each H-bridge circuit. In the CHB-qZSI, a shoot-through (ST) state is used to boost voltage without any damages in the power circuit. In one switching period, the number of the ST states in the single-phase qSBI is two. Therefore, the operating frequency of the inductors is twofold the switching frequency. In the CHB-qZSI, the input DC current is continuous with low ripple. Each module in the CHB qZSI can produce the same DC-link voltage by control the ST duty cycle. An effective control method, including system-level control and PWM for single-phase CHB-qZSI based grid-tie photovoltaic (PV) power system is presented in [17]. Three-phase CHB-qZSI's control is proposed and demonstrated in [18] for application to PV power systems. A qZS modular cascaded converter is addressed in [19] for dc integration of high-power PV systems. Energy stored CHB-qZSI based PV power generation system is proposed in [20]. Fault-tolerant CHB inverters using Z-sourced network are investigated in [21] and [22]. A cascaded transformer-based multilevel inverter using single Z-source network is presented in [23]. An active-front-end (AFE) CHB multilevel inverter based on dual-boost/buck converter is proposed in [24]. Like the CHB-qZSI, the AFE-CHB inverter also has the shoot-through immunity and

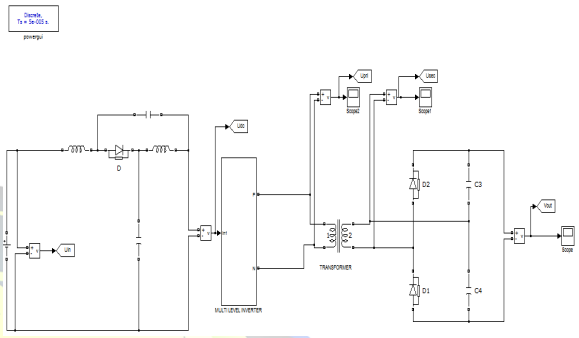
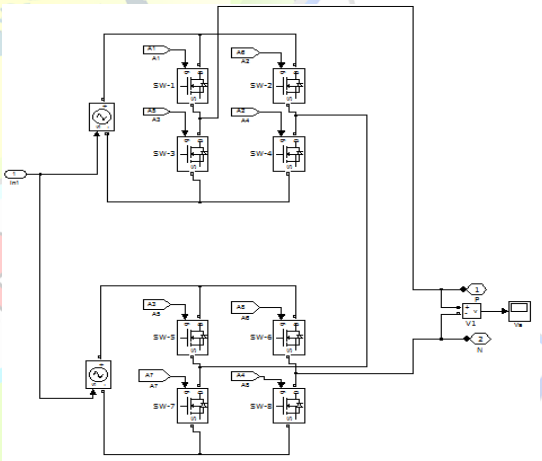


Fig. 2. Proposed qCHB-FLBI topology.



sub blocks in multilevel inverter

step-up DC-DC converter is proposed in [27] based on the qSB network. In this paper, a new single-stage quasi-cascaded H-bridge five-level boost inverter (qCHB-FLBI) is proposed. In the proposed qCHB-FLBI, the qSB network as presented in [27] is used in each module. The main features of the proposed qCHB-FLBI are five-level output voltage with boost voltage

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ability, reduction in a number of passive components and shoot-through immunity. Section II presents the proposed cascaded topology. Comparison with the conventional CHB five-level inverters is addressed in Section III. Simulation results are shown in Section IV. The experimental results are presented in Section V

II. PROPOSED TOPOLOGY

The configuration of the proposed single-stage qCHB-FLBI is illustrated in Fig. 2. The

$$L_1 \frac{di_{L_1}}{dt} = V_{c1} \quad . \qquad (1)$$

proposed inverter consists of two separate DC sources, two quasi-boost inverter (qBI) modules and an inductor filter connected to the resistive load in series. Each qBI module contains one capacitor, one boost inductor, four switches and two diodes. The output voltage of the proposed qCHB-FLBI has five levels.

A. Operating Principles

Assuming that two qBI modules have the same parameters, the qBI module 1 in the proposed system is used to analyze the operating principle. Fig. 3 shows the operating modes of the qBI module 1 in the proposed inverter.

In the shoot-through (ST) state 1, as shown in Fig. 3(a), both $S_1$and $S_2$are turned on. $D_{a1}$is conducting, while $D_{b1}$is blocking.If S_3 is turned on, the output voltage of the qBI module 1 is – V_{C1}. Else, it equals zero. The inductor $L_1$is charged from thesource. We have:

$$L_1 \frac{di_{L_1}}{dt} = V_{c1} \quad . \qquad (1)$$

In the ST state 2, S_3 and S_4 are turned on as shown in Fig. 3(b). $D_{a1}$is blocking, while $D_{b1}$is conducting. If $S_2$are turned on, theoutput voltage of the qBI module 1 is $-V_{C1}$. Else, it equals zero. The inductor L_1 is also charged in this state, and its voltage is calculated as (1).

In the non-shoot-through (NST) state 1, as shown in Fig. 3(c), both S_1 and S_3 are turned on. In the NST state 4, as shown in Fig. 3(f), both S_2 and S_4 are turned on. The output voltage of the qBI module 1 in both NST states 1 and 4 is zero.In the NST state 2, as shown in Fig. 3(d), both S_2 and S_3 are turned on. The output voltage of the qBI module 1 is $-V_{C1}$.In the NST state 3, as shown in Fig. 3(e), both S_1 and S_4 are turned on. The output voltage of the qBI module 1 is V_{C1}.During the non-shoot- through (NST) states as shown in Figs. 3(c)–3(f), D_{a1} and D_{b1} are conducting. The capacitor C_1 is charged from V_{dc}, while the inductor L_1 transfers energy from the DC voltage source to the main circuit. The H-bridge circuit is equivalent as a current source, i_{PN1}. We get:

$$L_1 \frac{di_{L_1}}{dt} = V_{dc} - V_{C1} \quad . \qquad (2)$$

In one switching period, T, each leg has twice short circuits alternatively. From (1) and (2), the average inductor voltage is

where $T_0/T = D_1$ is a ST duty ratio in each leg of module 1; T_0 is total ST time intervals in one leg.
In a steady state, the average inductor voltage should be zero. We get:

Similarly, we also obtain the capacitor voltage on the module 2 as

$$V_{C2} = \frac{1}{1 - 2D_2} V_{dc2} \qquad (5)$$

B. PWM Scheme for the Proposed Inverter

Fig. 4 shows a phase-shifted sinusoidal pulse-width modulation (PS-SPWM) strategy for the proposed

$v_{control}$are compared to a high -frequency triangle voltage, V_{tri1}, to produce control signals for the $S1$and $S2$ switches. Two DC voltages, $V_{SH}$and $-V_{SH}$, are compared to V_{tri1} to produce the $S0a$control signal. Then $S0a$is added to the control signals of
switches $S1$ and $S2$ to produce the ST states. Likewise, the V_{tri1} is shifted in 90° to create another high-frequency triangle voltage, V_{tri2}. $v_{control}$ and $-v_{control}$ are compared to V_{tri2} to produce control signals for the $S3$and $S4$ switches. $V_{SH}$and$-V_{SH}$are compared to the $V_{tri2}$to produce a $S0b$control signal.The $S0b$ is then added to the control signals of switches $S3$ and $S4$to produce the ST states. As a result, the output voltagev_{ab}ofH-bridge module 1 has three levels.
Similar for the second H-bridge module, two control voltages ($v_{control}$ and $-v_{control}$) are shifted in 180° to produce the output voltage v_{cb} of the H-bridge module 2. The output voltage v_{ac} of
the cascaded system is a subtraction of v_{ab} and v_{cb}. Therefore,

$$B = \frac{Dc\ link\ voltage}{Input\ voltage} = \frac{80}{40} = 2$$

$$D_s = \frac{1 - \left(\frac{1}{B}\right)}{2} = 0.25$$

$$U_{c1} = \frac{1 - ds}{(1 - 2ds)} * V = \left(\frac{1 - 0.25}{1 - 2(0.25)}\right) * 40$$

$$= 60v$$

$$U_{c2} = \frac{(0.25)}{(1 - 2(0.25))} * 40 = 20v$$

the output voltage of the proposed qCHB-FLBI produces five levels as shown in Fig. 4.

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simulation output
GATINGSIGNALFOR40V,

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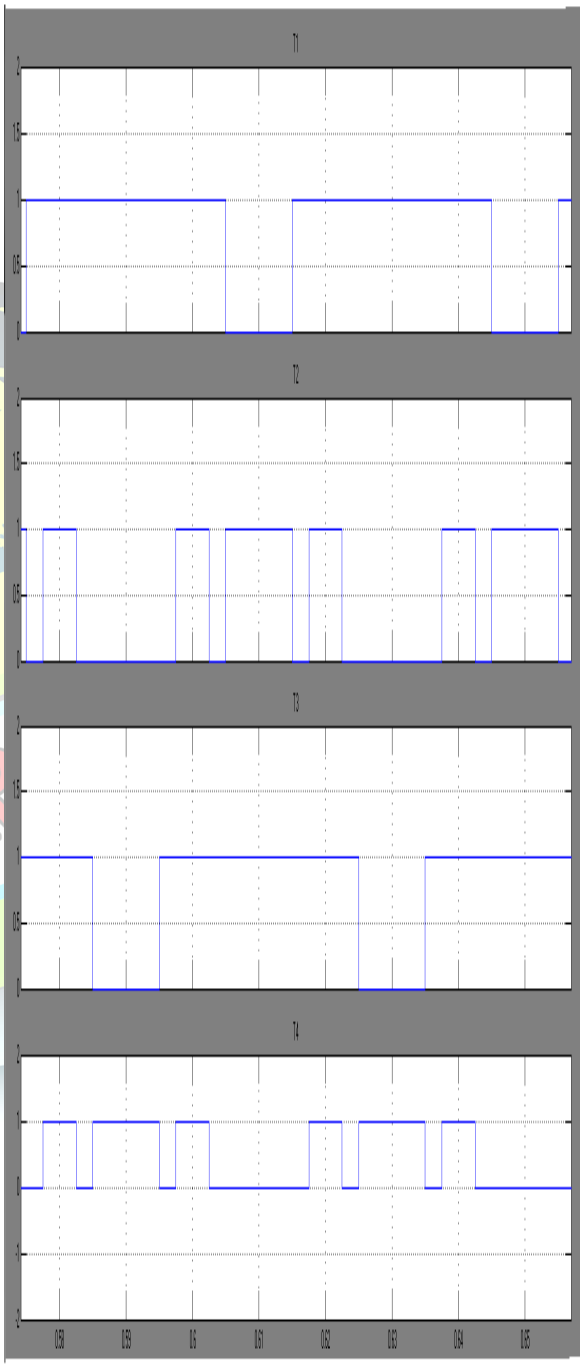
DS=0.25



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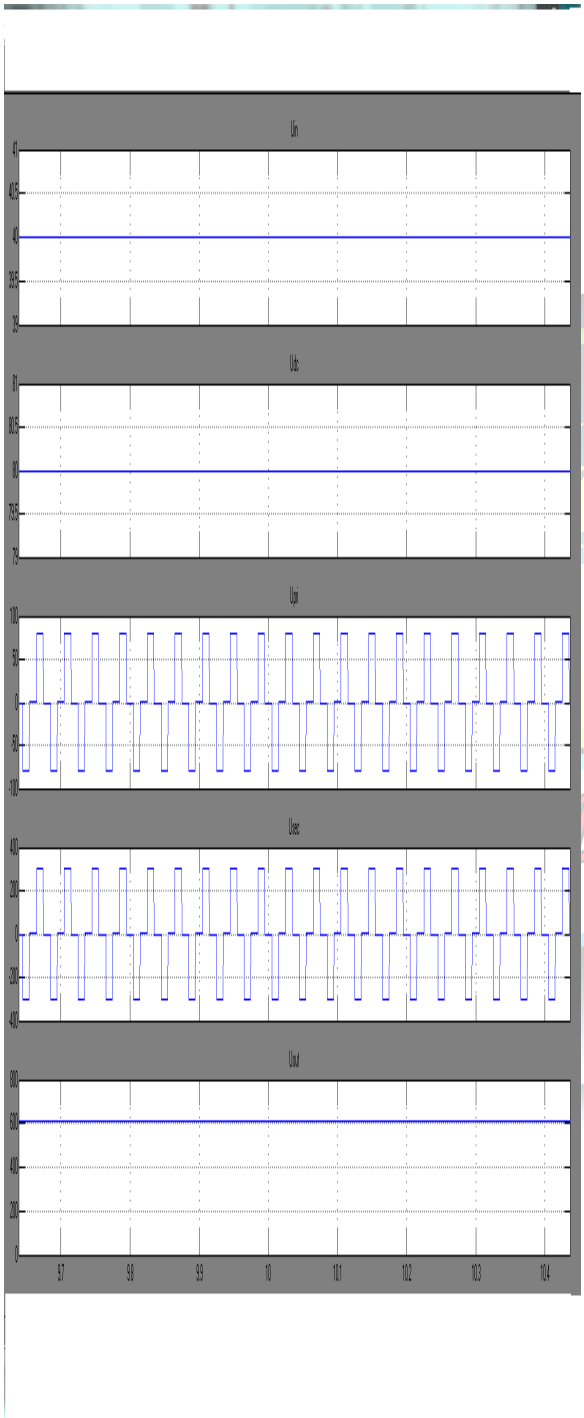
STIMULATION OUTPUT F0R 40V



Because the number of the ST states in the proposed qCHB-FLBI in one switching period is four as shown in Fig. 4, the operating frequency of the inductors in the proposed inverter is fourfold the switching frequency. In the CHB-qZSI, the operating frequency of the inductors is twofold the switching frequency. Therefore, the high-frequency current ripple on inductors of the proposed qCHB-FLBI is a half that of the CHB-qZSI.

C. Solving Unbalanced DC Source Problem in the Proposed Inverter

In order to achieve a good quality of the output voltage as shown in Fig. 4, the capacitor voltage in each module must be the same. From (4) and (5), the ST duty cycles D_1 and D_2 in each module are used to control the capacitor voltages V_{C1} and V_{C2}, respectively. When the DC input voltage in each module isunbalanced, D_1 is different from D_2 to keep $V_{C1} = V_{C2}$. The difference between D_1 and D_2 results in generating the DC offset at the output voltage. To remove the DC offset of the output voltage, a capacitor C_d is added to the output of the proposed inverter. Fig. 5 shows the proposed inverter under unbalanced DC source condition, where the capacitor C_d is connected between b_1 and b_2 nodes to filter the DC component at the output. Assuming $V_c = V_{C1} = V_{C2}$, the DC offset voltage is calculated as

$$V_{cd} = \frac{\frac{D_1}{1}V_{dc}}{1 - 2D_1} - \frac{\frac{D_2}{2}V_{dc}}{1 - 2D_2} = (D_1 - D_2) \cdot V_C. \quad (6)$$

Because the subtraction between D_1 and D_2 is too small, the voltage stress on C_d is very low. Therefore, the effect the size and cost of the capacitor C_d to overall cascaded system is trivial. Note that the current rating of capacitor C_d should carry the entire load current during operation of the circuit.

III. COMPARISION WITH CONVENTIONAL CHB INVERTERS

Table I compares the passive and active components of the CHB-qZSI, the cascaded H-bridge boost-five-level inverter (CHB-BFLI) and the proposed qCHB-FLBI. In comparison with the CHB-qZSI [15] as shown in Fig. 1(b), the proposed qCHB-FLBI in Fig. 5 uses one less capacitor, two less inductors, and two more diodes. Compared with the CHB-BFLI
as shown in Fig. 1(a), the proposed inverter uses two less switches and one more capacitor. However, the CHB-BFLI has a shoot-through problem. The operating frequency of the inductors in the proposed inverter is fourfold the switching frequency of the H-bridge circuit, while it is twofold in the CHB-qZSI. Therefore, the high-frequency current ripple on inductors of the proposed qCHB-FLBI is a half that of the CHB-qZSI.

TABLE I
COMPARISON BETWEEN THE PROPOSED QCHB-FLBI AND THE CONVENTIONAL FIVE-LEVEL INVERTERS

	qCHB-FLBI	CHB-qZSI	CHB-BFLI
Number of inductors	2	4	2

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Number of capacitors	3	4	2
Number of diodes	12	10	12
Number of switches	8	8	10
Shoot-through immunity	Yes	Yes	No
Input current	Continuous	Continuous	Continuous
Inductor frequency	$4f_s$	$2f_s$	f_B

where fs and fB are the switching frequency of the H-bridge circuit and the switching frequency of the boost DC-DC converter, respectively.

TABLE II
VOLTAGE STRESSES OF THE PROPOSED QCHB-FLBI AND CHB-qZSI

		Proposed inverter	CHB-qZSI
Capacitor voltage	$VC1$	$\frac{1}{1-2D_1}V_{dc1}$	$\frac{1-D_1}{1-2D_1}V_{dc1}$
	$VC2$	$\frac{1}{1-2D_2}V_{dc2}$	$\frac{D_1}{1-2D_1}V_{dc1}$
	$VC3$	Not appear	$\frac{1-D_2}{1-2D_2}V_{dc2}$
	$VC4$	Not appear	$\frac{D_2}{1-2D_2}V_{dc2}$
	VCd	$(D_1-D_2).V_C$	Not appear
Diode voltage stress		$\frac{1}{1-2D_1}V_{dc1}$	$\frac{1}{1-2D_1}V_{dc1}$
Switchvoltage stress	S_1-S_4	$\frac{1}{1-2D_1}V_{dc1}$	$\frac{1}{1-2D_1}V_{dc1}$
	$S5$- $S8$	$\frac{1}{1-2D_2}V_{dc2}$	$\frac{1}{1-2D_2}V_{dc2}$

TABLE III
SIMULATION AND EXPERIMENT PARAMETERS

Parameters		Values
Power rating		1.2 kVA
Inverter output voltage		110 Vrms
Output frequency		50 Hz
Inductors ($L1$, $L2$)		2 mH
Capacitors	$C1$, $C2$	4.4 mF/ 200 V
	Cd	4.7 mF/ 25 V
load	Inductor (L_f)	3 mH
	Resistor (R)	40 Ω
Switching frequency	(f_s)	10 KHz

Because the CHB-qZSI has the same feature in shoot-through immunity as the proposed qCHB-FLBI, the voltage stress comparison between two inverters is addressed. Table II compares the governing equations of the proposed qCHB-FLBI to the CHB-qZSI. As shown in Table II, the capacitor voltages of the proposed inverter are higher than those of the CHB-qZSI. However, total capacitor voltage stresses in each module of both inverters are the same. The voltage stress on diodes and switches of the proposed inverter equals to that of the CHB-qZSI.

IV. SIMULATION RESULTS

In order to test the operating principle of the proposed qCHB-FLBI as shown in Fig. 5, PSIM simulation is used. Table provides a list of the simulation parameters for the proposed qCHB-FLBI. The ON-resistance of all switches is set to 0.27 Ω in the simulation.

Fist, we set $V_{dc1} = V_{dc2} = 50$ V to confirm the properties of the proposed inverter under balanced DC-source condition. Fig. 6 shows the simulation results for the proposed qCHB-FLBI when both input voltages are the same. As shown in Fig. 6(a), the output voltage of the proposed inverter has five levels; and the load voltage is 110 V_{rms}. From Fig. 6(a), we can see that both the capacitor C_1 and C_2 voltages are boosted to 116 V in the steady state and the peak-to-peak voltage on C_1 and C_2 capacitors is 9 V. The DC-link voltage of each module is the square waveform as shown in Fig. 6(b).

Next, we increase the input voltage of module 2 (V_{dc2}) to 60V, while V_{dc1} = 50V to test the properties of the proposed inverter under unbalanced DC-source condition. Fig. 7 shows the simulation results for the proposed qCHB-FLBI when V_{dc1} = 50 V and V_{dc2} = 60 V. As shown in Fig. 7(a), the output voltage of the proposed inverter has five levels and the load voltage is 110 V_{rms}. From Fig. 7(a), we can see that both the capacitor C_1 and C_2voltages are also boosted to 116 V in the steady state, and thepeak-to-peak voltage on C_1 and C_2 capacitors are 9 V. As shown in Fig. 7(a), the average value of the capacitor C_d filter voltage is very low, about 6 V. Therefore, the size of capacitor filter C_d is pretty small and it does not affect the total size and weight of proposed inverter. The dc-link voltage of each module is the square waveform as shown in Fig. 7(b). Because the ST duty cycle of module 1 is higher than that of module 2, the five-level output voltage has a high distortion in the positive half cycle as shown in Fig. 7(a). On the contrary, the five-level output

voltage has a high distortion in the negative half cycle when the ST duty cycle of module 1 is lower than that of module 2.

Table IV compares the simulated THD of the output current between the CHB- qZSI and the proposed qCHB-FLBI. The same parameters as the proposed inverter were used to simulate the CHB-qZSI. From Table IV, we can observe that the THD of the output current of the proposed inverter is lower than that of the CHB-qZSI.

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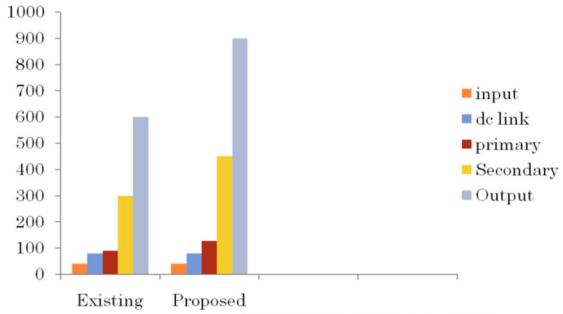
COMPARISIONS TABLE

PARAMETERS	EXISTING	PROPOSED
Primary voltage	90v	106.5v
Secondary voltage	300v	400v
Output voltage	600v	900v
THD	0.98	0.47

comparision chart



A 1.2-kVA prototype was constructed in the laboratory to verify the properties of the proposed qCHB-FLBI in Fig. 5. Fig. 8 shows an implementation photo of the proposed inverter. Fig. 9 shows a gating signal generation circuit based on TMS320F28335 DSP. Eight IRFP460 MOSFETs were controlled by insulated TLP250 amplifiers. Four DSEI60-06A diodes were used in the proposed inverter. The inductance of L_1 and L_2 is 2 mH. Two 200-V/2200-µF capacitors are connected in parallel to obtain 4400-µF capacitance of capacitors C_1 and C_2as shown in Fig. 8, while the $C_d$capacitor is 4.7 mF/ 25 V.The filter inductor is 3 mH, and the resistor load is 40 Ω. The switching frequency is 10 kHz. The V_{dc1} and V_{dc2} input voltages are varied from 50 V to 60 V, while the AC output voltage is 110 V in RMS. Two separate sources (V_{dc1} and V_{dc2}) were

generated as follows. A three-phase step- down transformer was connected to a 220/380-V utility grid. Two of three output voltages of the transformer were used to generate two separate DC voltages through a single-phase diode rectifier and a filter capacitor. The experiment parameters are also shown in Table III.

Experiment results are measured on the TPS 2024B and MSO2024B Tektronix electronic oscilloscopes, and Hioki 3197 power quality analyzer. The current waveforms are measured through the current transducer (LEM LA 25-P).

A. Case 1: V_{dc1} = V_{dc2} = 50 V

Fig. 10 shows the experimental results for the proposed qCHB-FLBI when both input voltages are the same. The output voltage of the proposed qCHB-FLBI has five levels and the measured load voltage is 110 V_{rms}. In the steady state, the measured capacitor C_1, C_2 and C_d voltages are 129 V, 129 V and 0 V, respectively. The peak-to-peak voltages on capacitor C_1 and C_2 are 8 V. The dc-link voltage of each module is the square waveform as shown in Fig. 10(d). The measured THD values of the output voltage and current are 1.2% and 1.5%, respectively.

B. Case 2: V_{dc1} = 50 V and V_{dc2} = 60 V

Fig. 11 shows the experimental results of the proposed qCHB-FLBI under unbalanced DC source condition (V_{dc1} = 50 V and V_{dc2} = 60 V). The proposed qCHB-FLBI produces five-level voltage at the output, and the measured load voltage is 110 V_{rms}. In the steady state, the measured capacitor C_1, C_2 and C_d voltages are 129 V, 129 V and 7 V, respectively. The peak-to-peak voltages on capacitor C_1 and C_2 are 8 V. The DC-link voltage of each module is the square waveform as shown in Fig. 11(d). The measured THD values of the output voltage and current are 1.3% and 1.8%, respectively. The results in the experiment are identical to those in the simulation. Table IV also shows the comparison between the simulated and measured THD values of the output current. The experimented THD of the output current is higher than simulated value. Note that the THD value of the output voltage and current in Figs. 10(f) and 11(g) is measured upto 50th hamonics by Hioki 3197 power quality analyzer.

C. Dynamic Response

A simple proportional–integral–derivative (PID) controller is used to control the capacitor voltage of each module. A block diagram of the capacitor voltage controller is shown in Fig. 9.

The sensing capacitor voltage of each module is compared to the reference value. The output error of the comparator is entered into the PID controller. Then, the PID controller output produces the control value of shoot-through duty cycle. A limiter is used to ensure the shoot-through duty cycle in range of [0.2, 0.35]. The modulation index is fixed at 0.65.

VI. CONCLUSION

The multilevel inverter was introduced as a solution to increase the converter operating voltage. The multilevel voltage source inverter is recently applied in many industrial applications . This type of multilevel configuration provides low harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The step-up dc/dc converter with high-frequency isolation for the distributed power generation system increases the power density, system stability

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