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Design of SRAM Using Read and Write Assist Techniques for High Performance in Low Power Applications

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Abstract- Power dissipation in VLSI circuits has become increasingly important for modern portable devices. In the proposed work inductor based supply boosting can be replaced by programmable booster level pulse generator. In static RAM(Random Access Memory) and logic in deep 32-nm Silicon On Insulator (SOI) FinFET technologies. Furthermore, adjusting the boost pulse generator allows for minimum voltage. In these programmable booster techniques that optimize the boost pulse and supply booster can varying the voltage level simulations also reveal the optimal combinations boost voltage, where the static random access memory can be rendered fully functional in the absence of any assist circuitry. These enhancements allow for a reduction in the power required for boosting through optimizing boost buffer sizes and shaping the boost pulse width. The design has been carried out in LT spice and HSPICE using 14nm FinFET technology. To maintain the wide range of operation from low to high voltage to achieve the optimal power and performance of operating voltage

Index Terms— Boosted supply, FinFet, inductors, low-power electronics, low Vmin, 8T, static random-access memory (SRAM).

I. INTRODUCTION

Power efficient and low-voltage SRAM will be a key enabler for emerging hardware paradigms. For example, IoT (internet-of-things) chips and deep learning accelerators will most likely target lower operating voltages than high-performance processors. The scaling of high-performance and dense SRAMs, however, pose challenges from process, voltage, temperature variability and functional yield perspectives. Lowering voltage further aggravates the variability problem. Many efforts are made to achieve minimum voltage for functionality Vmin. To maintain the functionality at lower voltages for 6T/8T SRAM cells various techniques, such as, dual and dynamic power supplies, boosting technologies. Some of the notable ones are static and dynamic dual power supply, usage of devices for the cell, shorter bit lines, usage of write assist techniques, the addition of transistors in an SRAM cell, and the usage of technology,

e.g., silicon on insulator (SOI) versus bulk and non planar versus planar. The power supply remains one of the key knobs for reducing power consumption; however, lowering the power supply requires a balancing act for maintaining Vmin in order to achieve functionality as well as the performance of SRAM cells and latches. Functionality here can be best described in terms of cell write ability, read stability, and data retention, which strongly depend on process, voltage, and temperature variations. Furthermore, for high performance processors, it is important to maintain wide range of operation from low to high Vdd to achieve the optimal power and performance operating point for the given situation.

The operation of SRAM arrays at near threshold voltages still poses a challenge due to variability and functional yield difficulties when lowering supply voltages. Researchers have proposed techniques to improve stability for conventional 6T/8T cells, which include dual static as well as dynamic power supply boosting techniques using charge pumps and assist techniques targeting specifically arrays.

However, many of these techniques result in area, power, and/or supply voltage penalties. Recent trends show that static and separate power supplies are commonly used for arrays. The approach of using a static dual supply for the SRAM cell, the word line, and/or the logic comes at the cost of an extra power supply that adds complexity to the design as well as power. As an alternative to static dual supply, a charge pump methodology was proposed to boost only the word line however, extending this approach to the entire array would

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increase area and power. Likewise, the word line may be dynamically boosted supply with a 50% duty cycle To alleviate some of the power consumption overhead of a 50% duty cycle boost, "a step-down" dynamic word line boost is applied to only word line drivers with a much reduced duty cycle ,While this step-down approach reduces power, the lower voltages may lead to SRAM arrays functionality issues, which get worse as the desired beta and gamma ratios of SRAM cells cannot be achieved in scaled technologies and especially in FinFET technologies.

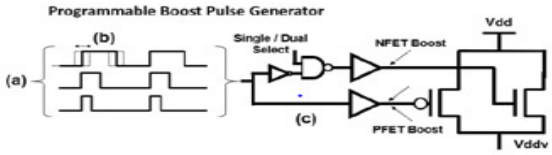

Fig 1 Programmable boost pulse generator.

The need to maintain optimal functionality across a wide range of operating voltages is an increasingly important requirement. For example, IoT applications may target operation at near threshold voltages, at the cusp of Vmin, to minimize power consumption. In terms of throughput oriented accelerators for deep learning, the target voltage would typically be higher than IoT to maintain performance, but a lower voltage than conventional processors to in-crease parallelism. Secondly, SRAM is often a crucial component of deep learning architectures, since neural network weights are often stored in SRAM

II METHODOLOGY SCHEMES

To reduce variability and improve performance at lower voltages beyond existing techniques we have proposed a FinFET based supply boosting technique for an entire macro, including logic and memory. This paper further investigates the boosting concept and goes beyond the initial hardware measurements presented providing programmable techniques that allow improved near threshold voltage (NTV) operation and power consumption across a wide voltage range.

A.SUPPLY BOOSTING CONCEPT

A FinFET to provides more capacitance between the gate and channel than a planar device. This capacitance can be harnessed using the circuit. when the gate switches from Gnd to Vdd and coupling between the gate and source provides a boost to increase the virtual supply voltage (Vddv) connecting the macro. Employing this boosted supply, when needed, im-proves the read and write functionality of 6T or 8T SRAM cells, allowing for single supply low Vdd operation. With its positive threshold voltage it is advantageous to use an NFET as a boost de-vice. The upward swing of the boost control will block the PFET in low voltage

B. ENHANCED BOOSTING TECHIQUES

In enhanced boosting techniques can be illustrates the novel aspects of the proposed programmable booster circuit. This circuit allows for a programmable pulse across three dimensions, (a) a variable pulse width, (b) a variable pulse phase, and (c) a selection of pulse strength versus power trade-off. Within a production macro, this programmable booster would be auto-calibrated using a BIST (built-in self-test) circuit to store optimized booster settings across various operating voltages, customizing the boost pulse for the specific array or array bank.

In terms of implementing a variable pulse width, pulse generators are often used for other purposes on-chip, e.g., a local clock driver for a transparent latch, thus the design effort and area cost for realizing such a circuit is low. A second aspect of the proposed programmable circuit is the pulse phase, which can be accomplished by selecting among multiple inverter delays. Next, independently-controlled NFET and PFET boost signals and selection of the number of boost buffers allows modifying the performance versus power tradeoffs for supply boosting at a fine grain. This technique can be realized with multiple boost control signals to select drive strength.

In SRAM Supply boosting include two variables to our simulations: 1) the booster size, 2) whether the boost is from single or dual boost signals. We measure the booster size by the number of fins in the final booster stage, i.e., 200, 400, or 600 fins. For the single boost data points, half the booster cells are connected to the PFET and half to the NFET. Thus, the active number of boost fins is effectively cut in half, i.e., 100, 200, or 300.

To illustrate the advantages of the proposed programmable

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boost circuit we begin with simulation results from the variable booster sizing technique. We present simulation results to show the Vddv effects that are not directly measurable from the test chip. We then

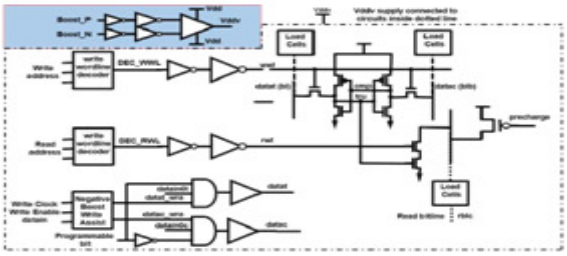

Fig 2. Booster and array cross-section for simulation.

C. BOOSTING VIA CIRCUIT LEVEL CAPACITIVE COUPLING

The base technique exploits the unique capacitive coupling effect in a FinFET device to dynamically boost the virtual macro supply voltage during active mode, thus improving the access performance and Vmin in the presence of variability. We also utilize interconnects to increase the capacitive coupling and thereby boost the power supply for the full macro. A negative bit line write-assist technique is also incorporated to further improve write-ability yield technique is also incorporated to further improve write-ability yield. The proposed scheme requires only a single supply and exploits the capacitive coupling from the gate and channels of a FinFET to its source. The basic circuit consists of two opposite polarity FETs in parallel with drains connected to Vdd. The boost transistor consists of an n-type FinFET with its gate controlled by the "BOOST" signal. Their common source forms a virtual Vdd (Vddv). In standby, BOOST is "Low", thus the virtual array supply voltage is at Vdd.

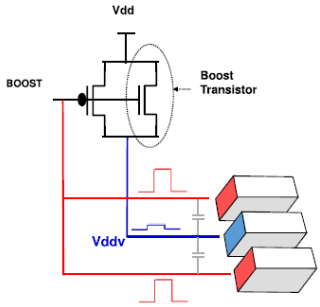

Fig 3. Transistor boosting and interconnect boosting.

III. STUDY OF FINFET

The new experimental SRAM design contains a 36Kb array shows the test chip block diagram. The architecture of the array consists of 256 entries with 144 bits per entry and has 1 read and 1 write port. The FinFET is a technology that is used within an integrated circuits and it is available for discrete devices. However the technology is becoming more sizes within integrated circuits. To provide very much high level of integration with less power consumption. In this technology to be reduced the power, operating voltage, sizes, static leakage current and operating speed.

The thickness of the device determines the channel length of the device. The channel length of a MOSFET is said to be the distance between the source and drain junctions.

It is a non-planar, double gate transistor which based either on the Bulk Silicon-On-Insulator (SOI) or on silicon wafers. Then working principle of FinFET is similar to that of conventional MOSFET.

14nm FinFET TECHNOLOGY

It is a process technology for an ideal high performance power efficient in volume applications. FinFET transistor provides a semiconductor device it is used to fabrication node following the technology. It consumes 63% direct power and 53% device area in high intrinsic gain. Based on 14nm technology with an higher density 8% and faster in 23%. FINFET operate at a lower voltage as a result of their lower threshold voltages.

IV SIMULATION AND WAVEFORMS

Thus, we developed a new booster approach that "wraps" the entire SRAM macro by booster circuits consisting of the booster header and buffers to attain the gain to drive the booster header. This wrapper-based booster approach, used for the first time in this 2nd generation test chip, allows constructing the booster circuits using only standard cells. The final stage of the booster structure is a standard cell inverter modified so that the Gnd terminals is connected to Vdd as well as with PFET and NFET gate connections separated to allow two boost signals as shown in the fig 4.

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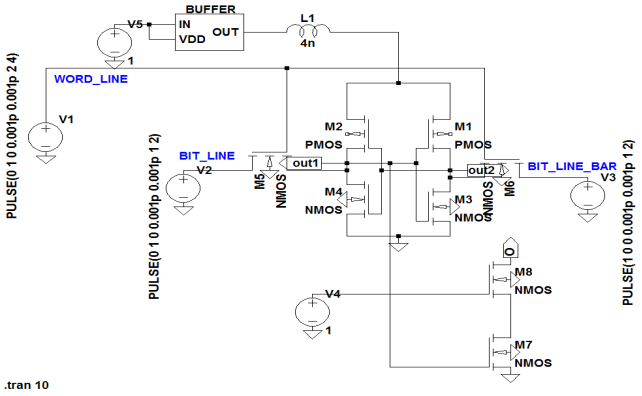
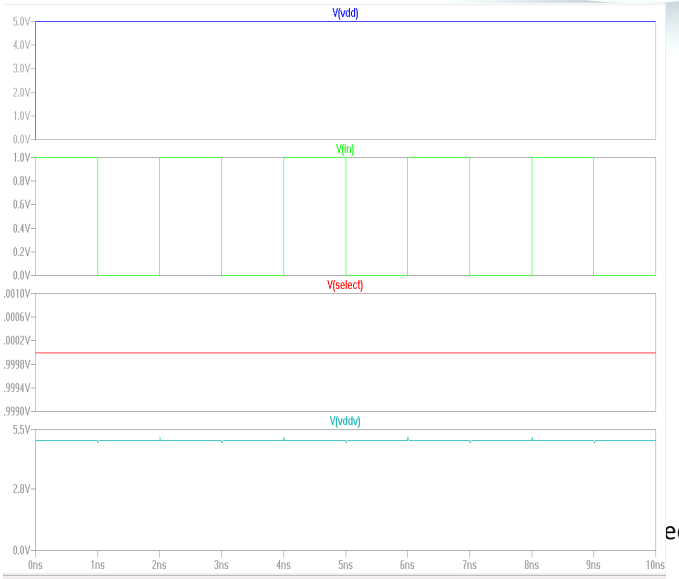


Fig 4. Schematic diagram of voltage level boosted SRAM cell

To reduce variability and improve performance at lower voltage of existing techniques. We have proposed a FinFET technology based programmable supply boosting technique to provide an lower voltage.

When gate switches from ground to Vdd and coupling switches between gate and sources. Then to improve programmable supply boosting technique. Both the inverter and buffer obtained the signals as input, Vdd, and output. In double gate PMOS and NMOS are programmed in pulse width modulator. Pulse width modulator to vary the signal according to input signals and message signals.

In proposed boost programmable pulse generator begin with simulation results to shown as Vddv. Here we include two variables of an simulations such as to boost the signals. In generator to boost the sizes and whether it can improve



double boost pulse generator. In double gate technology is an microelectronic circuit used for logic and an memory chips. In NMOS transistor are faster than PMOS transistor is an single chip to improve their

Voltages. In supply boosting programmable boost pulse generator is designed with an FinFET technology can be assigned. In another mode is switched only one gate and Apply bias to be a second gate. In the proposed system 14 nm FinFET technology is used to reduce the power and to determine the area power product.. HSpice & LTSpice are the major tools used for the design and generation of the

Fig 5 Proposed Waveform Of voltage level boosted SRAM cell

Waveform. The techniques have been applied in SRAM cell to obtained a minimum voltage for programmable boost pulse generator

In this techniques circuit level capacitive coupling requires only a single supply and capacitance coupling requires from gate and channel of FINFET to its source and as shown in the fig 5. The various circuit level techniques have been applied to transistor in SRAM cell being used for caches and their efficiency is compared

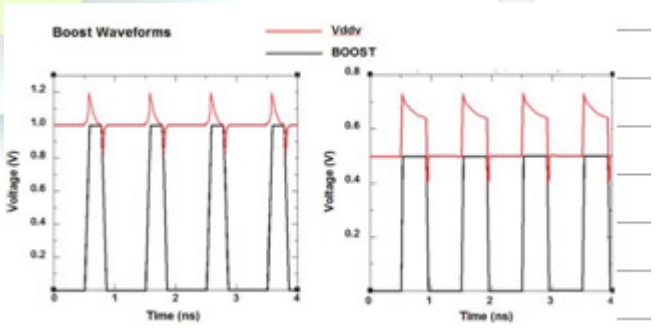


Fig 6. Boost waveforms at (a) high frequency (b) Low frequency.

In coupled and programmable sizing of NFET and PFET boosting signals, boost pulse width shaping and boost pulse phase shifting. Adjusting these programmable techniques .Allows optimizing the boosting approach from low Vmin

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operation to higher voltage operation with reduced power. Consider an boost waveform signals compare in low and high

Reference	SRAM density(Mb)	Vmin (v)	Type/Tech/size
[5] karl et al.	11.1	0.6	6T/40nm/84 kb
[6] Rooseleer et al.	0.0316	1.2	6T/40nm/256kb
[9] kulkarni et al.	0.403	Improve by 180mv	8T/22nm/12 kb
[13] pilo et al.	0.021	0.7	6T/22nm/512kb
[20] koo et al.	5.1	0.495	8T/14nm/512kb
Existing system	2.21	0.4	6T/CMOS technology
Proposed system	2.01	0.2	8T/FinFET Technology

frequency. To avoid the data leakage and reduce power consumption level in resonant supply voltages. Double gate MOSFETs (DGFET) is a MOSFET that has two gates to control the channel.

Its main advantage is that of improved short channel effects. Now a day FinFET is usually used for design. The reason behind it is short channel effects which provides better precision more compactable compared to other device. The Proposed technique shows reduced power consumption, delay and Power Delay Product (PDP) when compared to existing designs. The proposed designs are simulated using the HSPICE simulation tool at 14 nm FinFET technology.

V RESULT ANALYSIS

Table I:Comparison of inductor and programmable booster

In conventional based booster circuit involves the inductor based booster circuit, so it produces more eddy current loss. Due to eddy current loss, the circuit not suitable for high frequency. Then compare to proposed system the booster and SRAM is poor. It results in booster circuits 5.2V to 5V as input in above method.

Here we have to proposed the eddy current loss is avoided by replacing the inductor. The programmable booster circuit provides better results for higher frequency. Here the booster is designed with FinFET. So it provides better synchronization. To improve the design in terms of SRAM density, minimum voltage, access time are compared and shown as Table I.

VI.APPLICATION—IOT (INTERNET OF THINGS)

In interconnection through the internet of coupling devices embedded in both sending and receiving data. To better illustrate the design consideration for proposed boosting techniques. In IOT applications can be similar to new programmable boost pulse generator. Then the wide range of operation from low to high voltage to achieve an optimal power and performance of an high voltage. In IOT specified network of physical devices, home appliances and other items to be embedded.

IOT is a system of interrelated computing devices. It can be provided with unique identifiers and ability to transfer data over a network without computer interaction. In the vast area network the devices can be connected to internet. By using these low power processor, accelerators and IOT applications to be improved the capacitive boosting techniques.

VII CONCLUSION

In summary it has different results of DGMOS FinFET and to reduces the power. Further other modules are designed to using dual gate MOSFET. SRAM behaviour of FinFET technology is investigated and compare with 14nm technology. In SRAM in supply boosting it differentiate the FinFET technology to consume less power than a CMOS technology. In CMOS technology overcome with 14nm FinFET technology can be reduces the short channel effect. The results shows reduction of power dissipation, area, delays using an FinFET technology. In programmable supply boosting technique to provide an lower voltage and can improve double boost pulse generator.

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