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Design and Implementation of SPWM Based Asymmetrical Multilevel Inverter with Less Switches

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Abstract: Multilevel inverter have obtained more and more attention in recent years and new analysis with a wide variety of control strategies have been developed. An Asymmetrical multilevel inverter, a new analysis increases a level of output with reduced lower order harmonics and total harmonic distortion. In our prototype, only concentrated on the design and implementation of new analysis in a single phase thirty one level cascaded H-bridge multilevel inverter with the help of only eight switches, four diodes and four DC sources. The aim of our model is to extend the number of levels with a few number of switches and sources at the output. In our model, various carrier pulse width modulation techniques are used. It can be minimized the total harmonic distortion and boost the output voltages. The various switching analysis have been discussed in our model. Sinusoidal pulse width modulation (SPWM) is used to achieve high quality output with lower harmonics. It is justified that the new topology can be suggested to single phase thirty one level cascaded H-bridge inverter for better performance in comparison to conventional method. The simulation is completed by MATLAB/SIMULINK software. Module output voltage satisfies the harmonics standard (IEEE519).

Keywords– Asymmetrical Multilevel Inverter, Cascaded H-Bridge Multilevel Inverter, lower order harmonics, Total Harmonic Distortion(THD), SPWM

I. INTRODUCTION

Multilevel inverters have been innovated as necessary for cost benefits with wide range of applications. They have been in the focus for decades because of interesting features such as high quality output voltage, operation in high voltage/power, low stress on switches, etc. Multilevel inverters have the advantages like reduced EMI/RFI generation, minimum total harmonic distortion and can operate on several voltage levels compared with the conventional two-level inverter. Harmonics are reduced due to multi-switching and output is approximately a sine wave so the filter design and cost arereduced[1]. A multilevel inverter is a power electronic device which is capable of producing desired alternative voltage level at the output using multiple lower level DC voltage as an input. Multilevel converter have become one of the most widely used power converters in electrical field. The two level inverter need to be operated at higher frequency by using pulse width modulation (PWM) technique. Thus the switches undergo high switching losses. In order to overcome this disadvantage, MLI has been proposed with increasing the number of DC voltage sources in the input side. Sinusoidal waveform can be generated

at the output[2]. Multilevel converters are different arrangements of semiconductor switches with DC links to create n-level output waveform which are divided into three main categories: Neutral point clamped(NPC) inverter or Diode clamped inverter, Flying Capacitor(FC) inverter or Capacitor clamped inverter, Cascaded H-Bridge(CHB) inverter[3].

The main drawback of NPC is when the number of level increased, more number of clamped diodes are required. Also FC has the drawback of complex in inverter control and high switching loss. As compared with DC and FC inverter, CHB require less number of components in each level. When the number of semiconductor switches decreases, the switching losses also decreases and efficiency of entire system get increased[1,4]. For this reason, cascaded multilevel inverter is used. A CMLI made up of from series connected single full bridge inverter, each with their own isolated DC bus. This MLI

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can generate almost sinusoidal waveform voltage from several separate DC sources, which may be obtained from solar cells, fuel cells, batteries, ultra-capacitors, etc.,.This type of converters does not need any transformers or clamped diodes or flying capacitors[5].

MLI consist of basic unit and full wave converter unit. Basic unit generates only zero and positive levels. Full wave converter unit generates positive as well as negative voltage levels as required[6,7].The MLI is used for renewable energy sources such as fuel cell, wind and photovoltaic. The multilevel inverter can operate at both fundamental switching frequency and high switching frequency PWM. A Multilevel inverter is not only achieves high power rating but also improves the performance of the whole system[8]. Multilevel inverter has two major classifications: Symmetric MultilevelInverter and Asymmetric Multilevel Inverter (AMLI). AMLI is more advantageous than the symmetric one, because it produces more number of levels with same number of switches by having unequal voltage sources. As a result, the installation space and total cost of an asymmetric cascaded multilevel inverter is lower[9,6].

This paper focuses on the development of asymmetric multilevel inverter with least number of switches which produces thirty one output voltage levels. The performance parameters of this multilevel inverter such as THD for different modulation indices will be computed. Finally, the feasibility of the proposed inverter will be verified through simulation results by using MATLAB/ SIMULINK.

II. INVERTER

The inverter is a power electronic circuit which converts the DC to AC power, used in power backup at home. Now a days, Multilevel Inverters are used in high power switching application. The Fig. 1 and Fig. 2 shows the output waveform for inverter and multilevel inverter. Multilevel Inverter consists of several switches used in industrial applications, Railway Traction Drives and Electrical Vehicle etc.,[10,11]

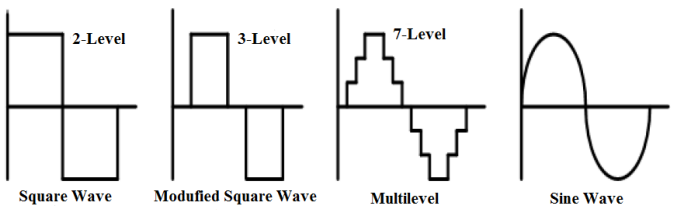

Fig.1Inverter output waveform

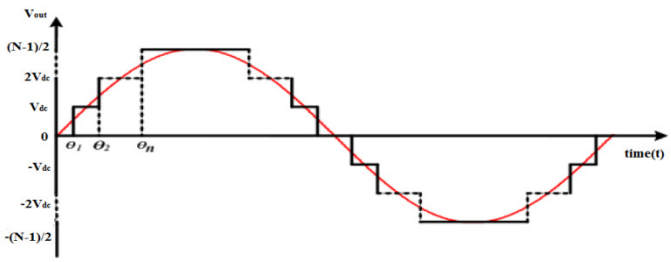

Fig.2Generalised stepped waveform for multilevel inverter(MLI)

III.MODULATION TECHNIQUES

The modulation techniques are used for switching the switches used in module. By using this, the switches are triggered by different category. Among it, multicarrier pulse width modulation is mostly used one. There are two types of modulation techniques available. Each type has further classifications which is explained in below. The Fig. 3 shows various types of modulation techniques.

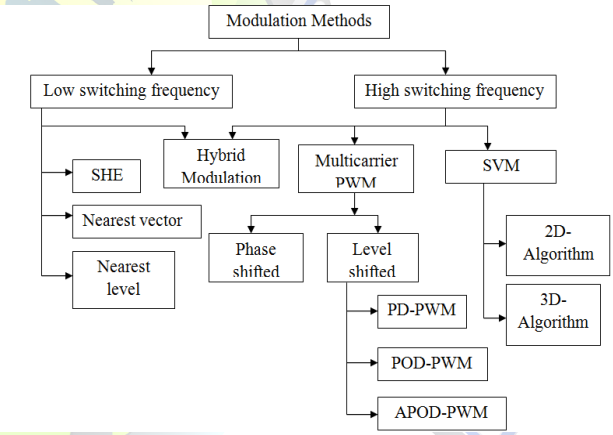

Fig. 3Types of modulation techniques

A. *Level Shifted PWM (LS-PWM)*

It is one type of multicarrier pulse width modulation.N-1 carrier signals are used which are vertically shifted to each other. A level-shifted PWM can be classified in three types.

a. *1) Phase Disposition PWM (PD-PWM):*In Phase Disposition all the carrier signals are in same. The Fig. 4 shows the gate pulse generation for PD-PWM.

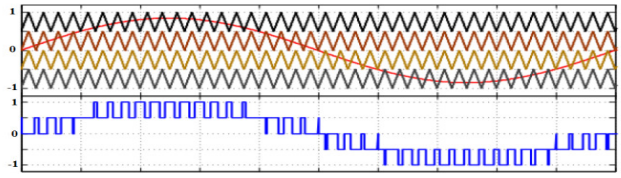

Fig.4PD PWM

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b. *2) Phase Opposition Disposition PWM (POD-PWM):*In Phase Opposition Disposition all the carrier signals above the zero are out of phase with those below the zero by 180º.The Fig. 5 shows the gate pulse generation for PD-PWM.

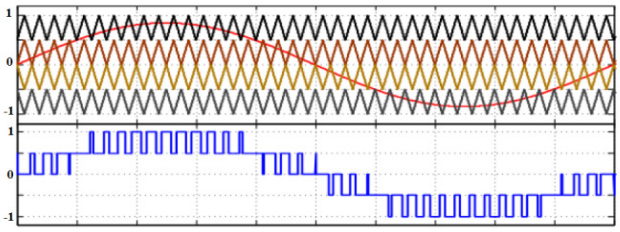

Fig.5POD PWM

c. *3) Alternative Phase opposition Disposition PWM (APOD-PWM):*In Alternate Phase Opposition Disposition all the adjacent carrier signals are out of phase by 180º.The Fig. 6 shows the gate pulse generation for PD-PWM.

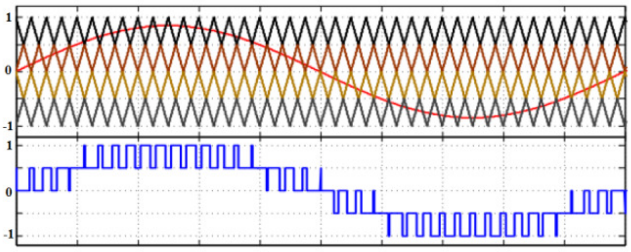

Fig.6APOD PWM

IV.STRUCTURE OF PROPOSED SYSTEM SINGLE PHASE MULTILEVEL INVERTER

Multilevel inverter use number of power semiconductor switches to generate stepped waveform.If level of inverter goes on increasing the output voltage of inverter gets more steps generating a staircase waveform which is a replica of sine waveform. Thus by increasing levels of inverter overall THD of inverter output voltage gets reduced. But there is a problem associated with multilevel inverter. More number of switches increases a drive cost. Also complexity associated with SPWM signal generation for more switches is increased[12].

This method shows a new topology of asymmetrical multilevel inverter with a new component arrangement including 8 IGBT switches, 4 diodes and 4 unequal DC sources ($1V_{dc}$, $2V_{dc}$, $4V_{dc}$, $8V_{dc}$). This arrangement synthesizes the voltage sources produces 31 levels (15positive level, 15negative level and one zero level).This configuration consist of level generator and H-Bridge unit for producing required output. The level generator unit is used for producing the required levels and the H-Bridge unit used for convert it into AC source (i.e.)produce both positive and negative cycles. The SPWM (Sinusoidal Pulse Width Modulation) control technique is used and it gives pulses to switches for operation.THD (Total Harmonic Distortion) is also reduced.The Fig. 7 shows the block diagram.

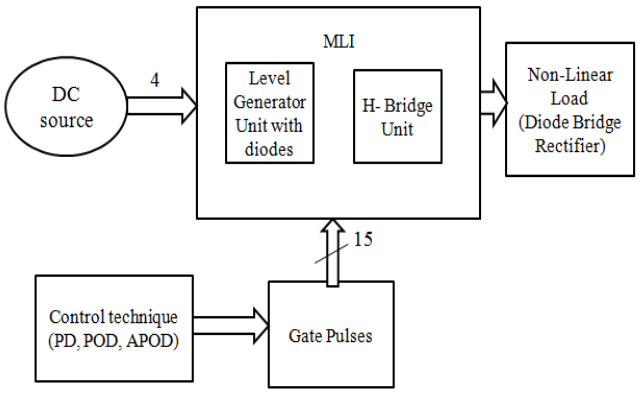

Fig.7 Block diagram

For generating output voltage levels, two switches must be turned ON in full bridge inverter unit, one from upper switches and other from lower switches. To get positive voltage H1 and H2 switches are in ON state and to get negative voltage H3 and H4 switches are in conduction state. The difference between values of sources improves performance of multilevel inverter and enhances the number of levels.

The design of pulse generation circuit makes the topology differs from other so as to obtain the unique pulse pattern to trigger the switches at the proper instant. All the switches in this topology is unidirectional. In this topology, reduced switches are used to develop thirty one levels and it makes the circuit user friendly and switches reduction benefits in low switching losses.

The maximum output voltage, number of power electronic devices, and number of levels for proposed asymmetric multilevel inverter are formulated as

$$V_{0max} = (2^n - 1) * V_1 \quad (1)$$

$$N_{IGBT} = n+4 \quad (2)$$

$$N_{Level} = 2^{(n+1)} - 1 \quad (3)$$

where n represents the number of voltage sources used in asymmetric multilevel inverter.

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TABLE I

CALCULATION OF NUMBER OF CONTROLLED SWITCHES FOR DIFFERENT NUMBER OF VOLTAGE SOURCES

Number of voltage sources	*Number of levels*	*Number of switches required*	*Maximum output voltage (V)*
1	*3*	*5*	*20*
2	*7*	*6*	*60*
3	*15*	*7*	*140*
4	*31*	*8*	*300*
5	*63*	*9*	*620*

The above equations are used to design a multilevel inverter of any level. The table below shows the number of switches and voltage sources required for different levels of MLI.

A. Low inductive circuit diagram

This circuit is only applicable to low inductive type load. If

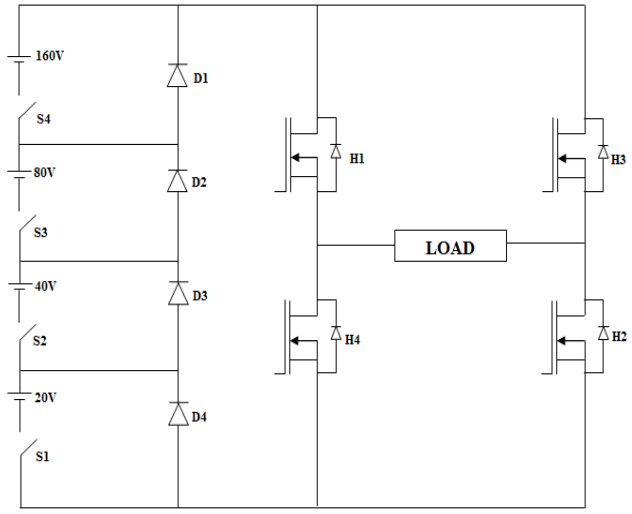

Fig. 8Structure of a 31 level MLI for low inductive load

any high inductive load is connected to this circuit, the output has spike with respect to load value. The THD value becomes high when connecting high inductive load. The Fig. 8 shows the circuit diagram for low inductive load.

TABLE II

SWITCHING TABLE FOR LOW INDUCTIVE LOAD

SWITCHES								OUTPUT VOLTAGES
S1	S2	S3	S4	H1	H2	H3	H4	Vo
1	0	0	0	1	1	0	0	20
0	1	0	0	1	1	0	0	40
1	1	0	0	1	1	0	0	60
0	0	1	0	1	1	0	0	80
1	0	1	0	1	1	0	0	100
0	1	1	0	1	1	0	0	120
1	1	1	0	1	1	0	0	140
0	0	0	1	1	1	0	0	160
1	0	0	1	1	1	0	0	180
0	1	0	1	1	1	0	0	200
1	1	0	1	1	1	0	0	220
0	0	1	1	1	1	0	0	240
1	0	1	1	1	1	0	0	260
0	1	1	1	1	1	0	0	280
1	1	1	1	1	1	0	0	300
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	-20
0	1	0	0	0	0	1	1	-40
1	1	0	0	0	0	1	1	-60
0	0	1	0	0	0	1	1	-80
1	0	1	0	0	0	1	1	-100
0	1	1	0	0	0	1	1	-120
1	1	1	0	0	0	1	1	-140
0	0	0	1	0	0	1	1	-160
1	0	0	1	0	0	1	1	-180
0	1	0	1	0	0	1	1	-200
1	1	0	1	0	0	1	1	-220
0	0	1	1	0	0	1	1	-240
1	0	1	1	0	0	1	1	-260
0	1	1	1	0	0	1	1	-280
1	1	1	1	0	0	1	1	-300

B. High inductive load circuit diagram

This circuit is only applicable to both low and high inductive type load. The spike is produced due to charging anddischarging of inductor at output side. When all the switches are in OFF condition (i.e. zeroth level), the inductor get discharge back. This is the reason for producing spike. This discharge avoided by using diode D5. The Fig. 9 shows the circuit diagram for low inductive load.

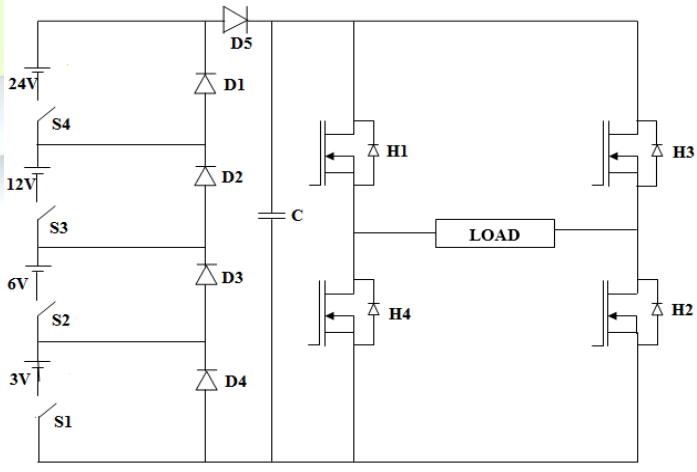

Fig. 9 Structure of a 31 level MLI for high inductive load

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TABLE III

SWITCHING TABLE FOR HIGH INDUCTIVE LOAD

SWITCHES								OUTPUT VOLTAGES
S1	S2	S3	S4	H1	H2	H3	H4	Vo
1	0	0	0	1	1	0	0	3
0	1	0	0	1	1	0	0	6
1	1	0	0	1	1	0	0	9
0	0	1	0	1	1	0	0	12
1	0	1	0	1	1	0	0	15
0	1	1	0	1	1	0	0	18
1	1	1	0	1	1	0	0	21
0	0	0	1	1	1	0	0	24
1	0	0	1	1	1	0	0	27
0	1	0	1	1	1	0	0	30
1	1	0	1	1	1	0	0	33
0	0	1	1	1	1	0	0	36
1	0	1	1	1	1	0	0	39
0	1	1	1	1	1	0	0	42
1	1	1	1	1	1	0	0	45
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	-3
0	1	0	0	0	0	1	1	-6
1	1	0	0	0	0	1	1	-9
0	0	1	0	0	0	1	1	-12
1	0	1	0	0	0	1	1	-15
0	1	1	0	0	0	1	1	-18
1	1	1	0	0	0	1	1	-21
0	0	0	1	0	0	1	1	-24
1	0	0	1	0	0	1	1	-27
0	1	0	1	0	0	1	1	-30
1	1	0	1	0	0	1	1	-33
0	0	1	1	0	0	1	1	-36
1	0	1	1	0	0	1	1	-39
0	1	1	1	0	0	1	1	-42
1	1	1	1	0	0	1	1	-45

The capacitor value of this circuit is depending on value of inductance at output side. This capacitor is used to filtering the spike present at output side when high inductive load is connected. So, the output has no spike ant also THD is get reduced. The regeneration for inverter is not supported by this circuit. But regeneration of the inverter is not considered. Here, the circuit is only designed for reducing THD with less number of components.

V. CONTROLLER PLATFORM

There are three types of control or modulation techniques available. There are 15 carrier signals used for producing 31 levels of output. The carrier is triangular wave and the reference is sinusoidal wave. When the reference wave magnitude higher than carrier wave, the gate pulses are generated. The carrier signal magnitude and phase angle for these types are different.

A. Phase Disposition (PD)

In this type of modulation technique, the all carrier signal magnitudes and phase angle are same. So, the separate carrier for positive and negative levels are not required. Only 15 carrier signal are enough for producing both positive and negative signals which is required for 31 level of output. The Fig. 10and Fig. 11 shows controller diagram for phase disposition and its gate pulse generation.

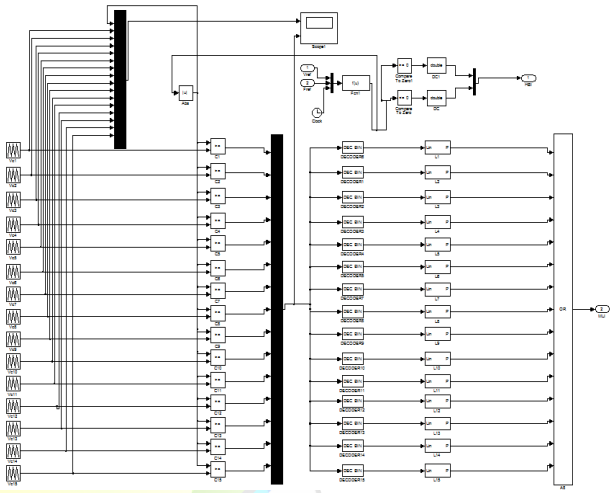

Fig. 10 PD controller diagram

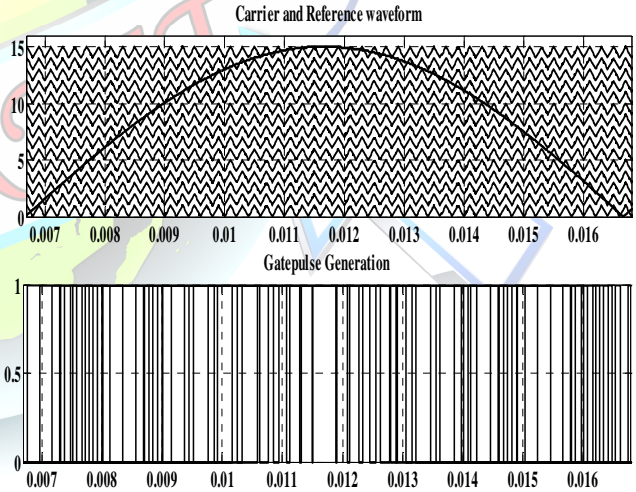

Fig. 11 Carrier, Reference and Gate pulse generation for PD

B. Phase Opposition Disposition (POD)

In this type of modulation technique, the all carrier signal magnitudes are same. But, the phase angle of carrier signal above the zeroth axis is in phase and the below the zeroth level is out of phase by 180 degree. So, the separate carrier for positive and negative levels are required. The Fig. 10 shows controller diagram for phase opposition disposition.

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The Fig. 11 and Fig. 12 shows controller diagram for positive carrier and its gate pulse generation.

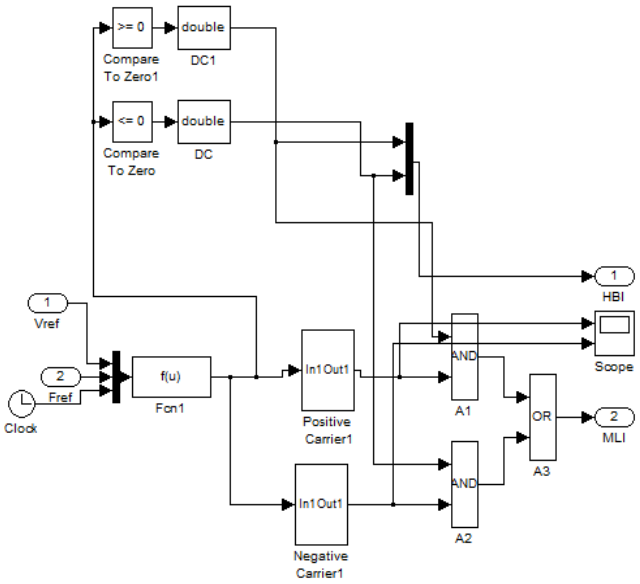

Fig. 12 POD controller diagram

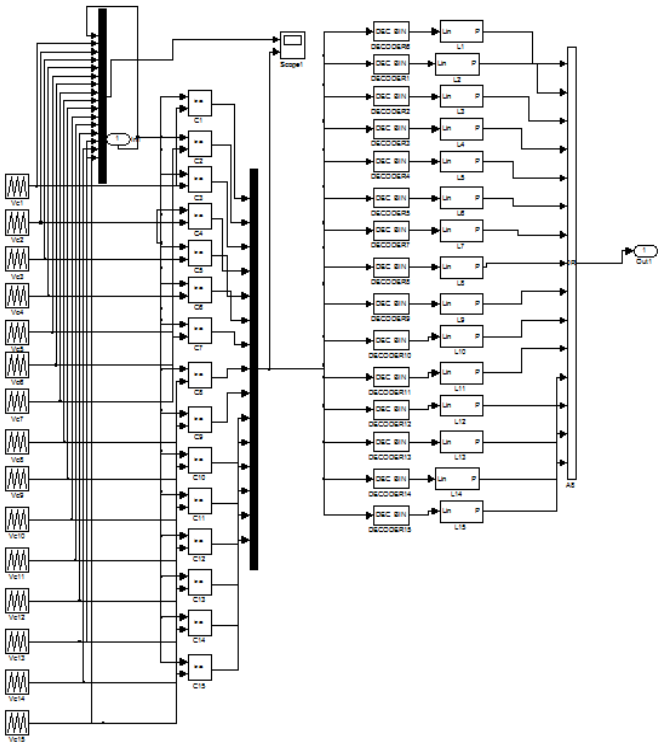

Fig. 13 Controller diagram of positive carrier

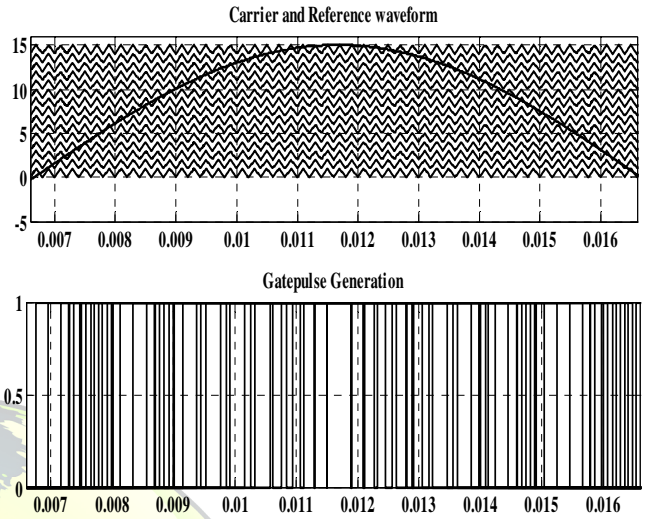

Fig. 14 Carrier, Reference and Gate pulses of positive carrier

Fig. 13 and Fig. 14 shows controller diagram for negative carrier and its gate pulse generation.

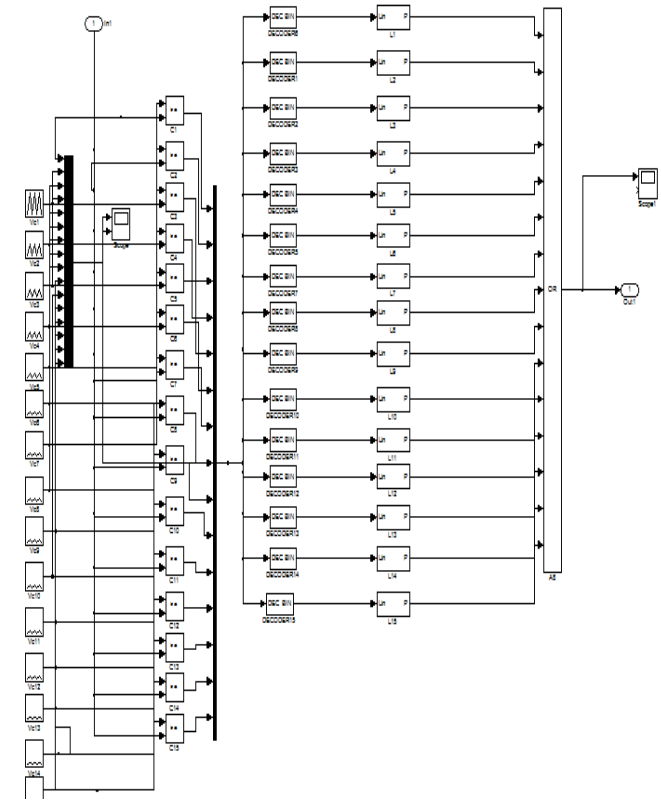

Fig. 15 Controller diagram of negative carrier

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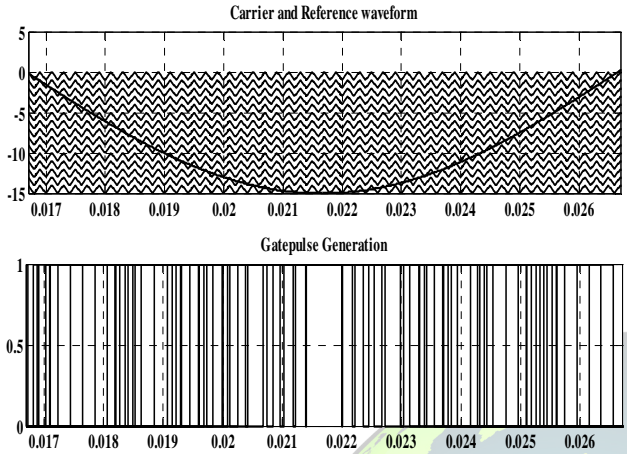

Fig. 16 Carrier, Reference and Gate pulses of negative carrier

C. *Alternative Phase Opposition Disposition (APOD)*

In this type of modulation technique, the all carrier signal magnitudes are same. But, the phase angle for carrier is out of phase by 180 degree. So, the separate carrier for positive and negative levels are not required. Only 15 carrier signal are enough for producing both positive and negative signals which is required for 31 level of output. The Fig. 17 and Fig. 18 shows controller diagram for Alternative phase opposition disposition and its gate pulse generation.

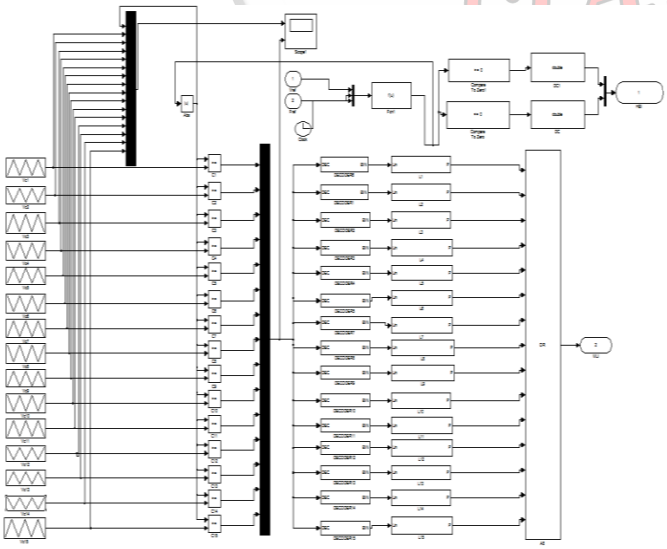

Fig. 17 APOD controller diagram

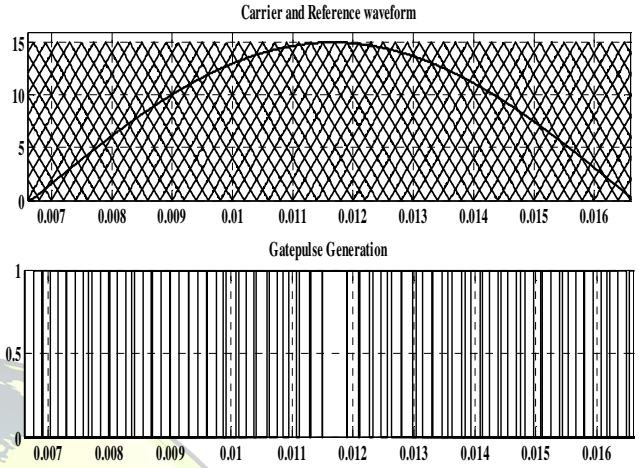

Fig. 18 Carrier, Reference and Gate pulses for APOD

VI. SIMULATION MODELLING

Simulation modelling show the both low and high inductive load simulation diagram of inverter output voltage and current for 31levels using different level shifted PWM techniques.. The specifications of this circuit is also listed in below table. The below figure shows the simulation diagram of proposed method by using MATLAB/SIMULINK.

A. *Simulation diagram of low inductive load*

The Fig. 19 Shows the simulation diagram which is used for only resistive and low inductive load. Otherwise, it has some magnitude of spike which is depending on inductive value at load side.

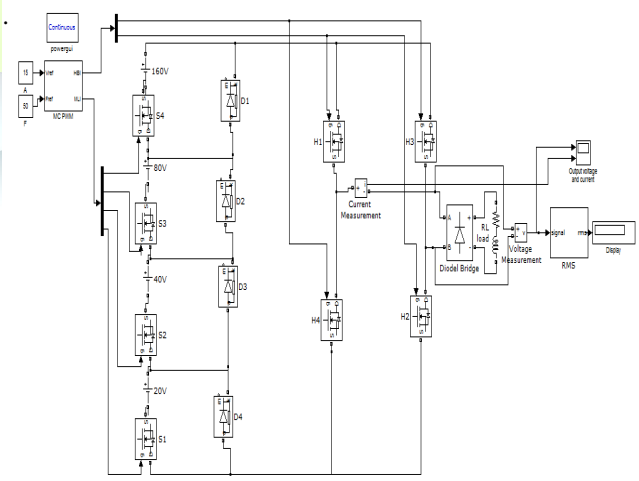

Fig. 19 Simulation diagram of low inductive load for proposed module

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TABLE IV

SPECIFICATIONS OF LOW INDUCTIVE LOAD FOR PROPOSED MODULE

COMPONENT	*VALUES*
DC source, V_1	*20 V*
DC source, V_1	*40V*
DC source, V_1	*80V*
DC source, V_1	*160V*
Load Resistor, R	*10 ohm*
Load Inductor, L	*1 mH*
Fundamental Frequency, F_S	*50 Hz*
Carrier Frequency, F_C	*5 kHz*

TABLE V

SPECIFICATIONS OF HIGH INDUCTIVE LOAD FOR PROPOSED MODULE

COMPONENT	*VALUES*
DC source, V_1	*3 V*
DC source, V_1	*6 V*
DC source, V_1	*12 V*
DC source, V_1	*24 V*
Load	*Single phase induction motor*
Fundamental Frequency, F_S	*50 Hz*
Carrier Frequency, F_C	*5 kHz*

B. Simulation diagram of high inductive load

The Fig. 20 Shows the simulation diagram which is used for highly inductive load. The capacitor used in this circuit remove the spike when using high inductive load and producing the nearer sine wave.

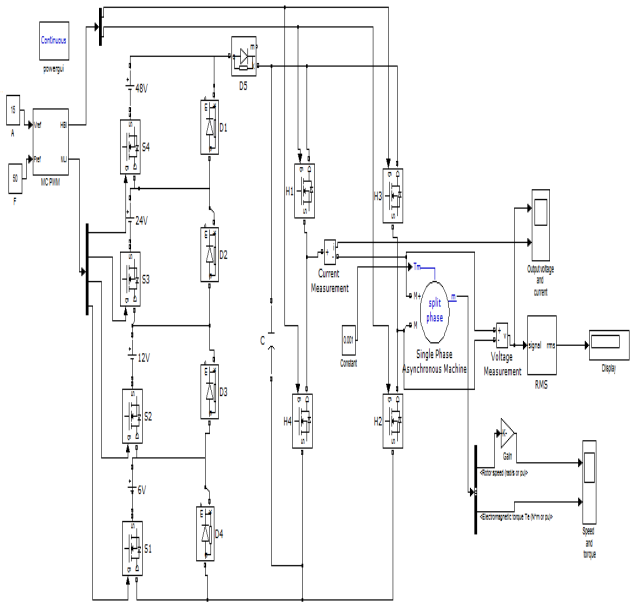

Fig. 20 Simulation diagram of high inductive load for proposed module

VII. SIMULATION RESULT

Simulation result show variation of overall THD of inverter output voltage and current for 31levels using different level shifted PWM techniques. The following results shows output response for both low and high inductive load and also shows THD variations for both loads. The proposed multilevel module is simulated by MATLAB to examine the performance of proposed module. The below figures shows the simulation diagram of output voltage and current for both loads by using MATLAB/SIMULINK.

A. For low inductive load

In low inductive load, the resistance effect is low compared with inductance. In starting stage of inductance, this circuit is applicable.

1) PD technique

In PD technique, the voltage and current are in same phaseand it produces 31 levels of output with low distortions for low inductive load which is satisfied IEEE standards.The output waveform is nearer to sine wave.The voltage and current waveform for proposed method is shown in Fig. 21 and Fig. 22 forPD technique.

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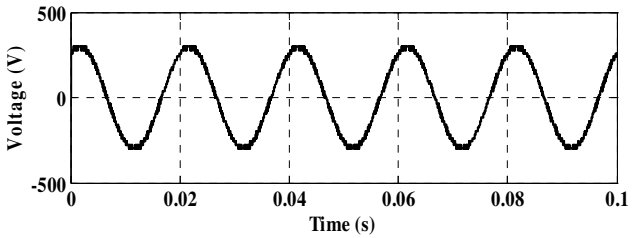

Fig. 21Output voltage waveform of low inductive load for PD technique

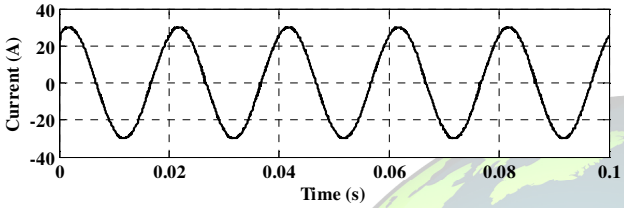

Fig. 22Output current waveform of low inductive load for PD technique

The Fig.23 and Fig.24 shows FFT window of 31-level inverter output voltage and current using PD technique.

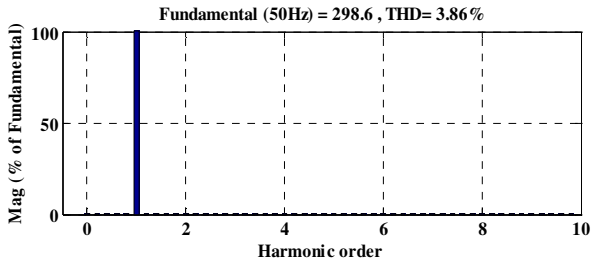

Fig. 23THD ofoutput voltage for low inductive load

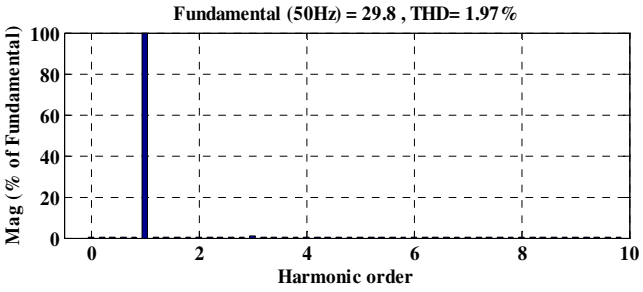

Fig. 24THD ofoutput current for low inductive load

2) *POD technique*

In POD technique, the voltage and current are in same phase and it produces 31 levels of output with low distortions for low inductive load which is satisfied IEEE standards. The output waveform is nearer to sine wave.The voltage and current waveform for proposed method is shown in Fig. 25 and Fig. 26 for POD technique.

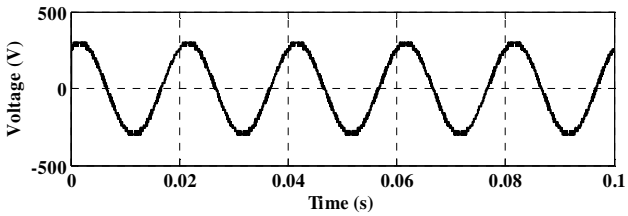

Fig. 25Output voltage waveform of low inductive load for POD technique

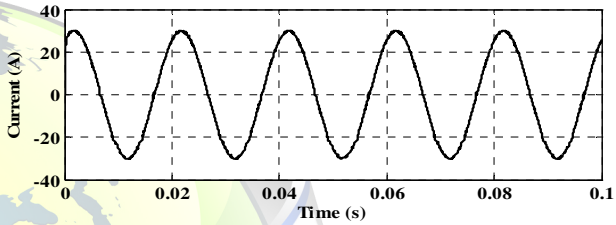

Fig. 26Output currentwaveform of low inductive load for POD technique

The Fig.27 andFig.28 shows FFT window of 31-level inverter output voltage and current using POD technique.

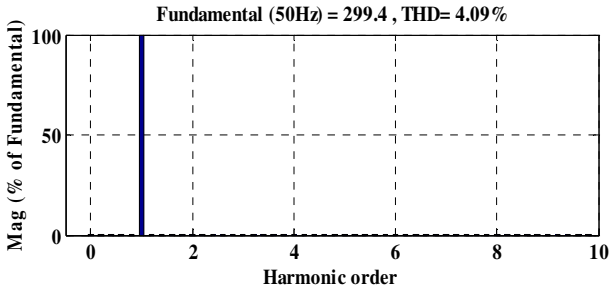

Fig. 27THD of output voltage for low inductive load

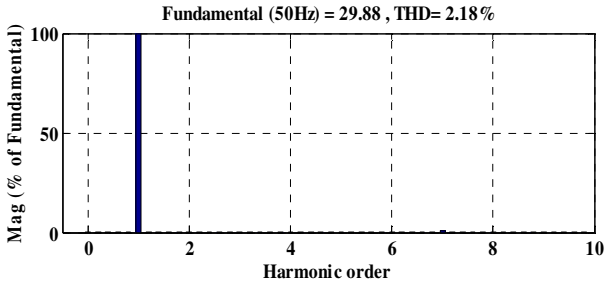

Fig. 28THD of output current for low inductive load

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3) *APOD technique*

In APOD technique, the voltage and current are in same phase and it produces 31 levels of output with low distortions for low inductive load which is satisfied IEEE standards. The output waveform is nearer to sine wave. The voltage and current waveform for proposed method is shown in Fig. 29 and Fig. 29 for APOD technique

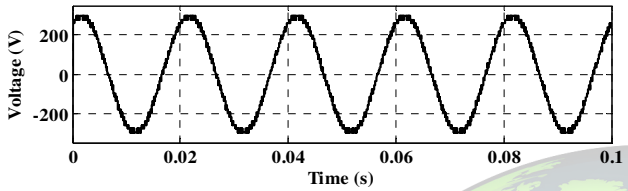

Fig. 29Output voltage waveform of low inductive loadfor APOD technique

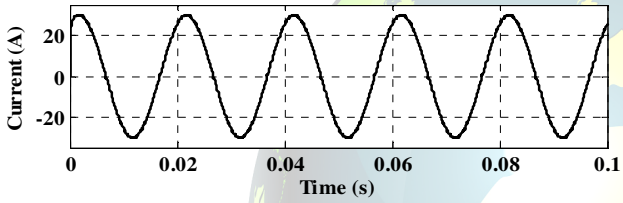

Fig. 30Output current waveform of low inductive load for APOD technique

The Fig. 30 and Fig. 31 shows FFT window of 31-level inverter output voltage and current using APOD technique.

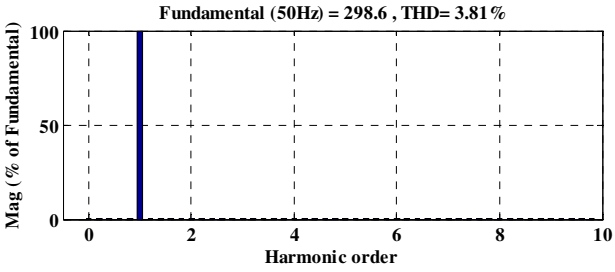

Fig. 31THD of output voltage for low inductive load

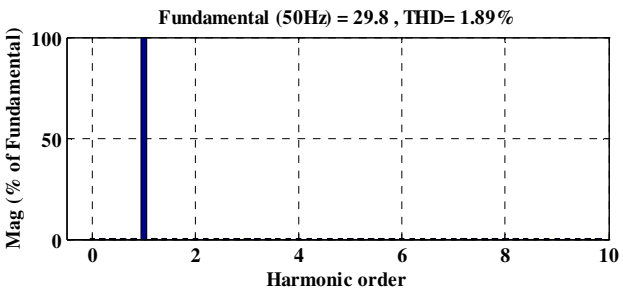

Fig. 32THD of output current for low inductive load

B. *High inductive load*

In high inductive load, the resistance effect is low compared with inductance. In extreme stage of inductance, this circuit is applicable

1) *PD technique*

In PD technique, the voltage and current are in same phase and it produces 31 levels of output with low distortions for highinductive load which is satisfied IEEE standards.The output

waveform is nearer to sine wave.The voltage and current waveform for proposed method is shown in Fig. 33 and Fig. 34 for PD technique.

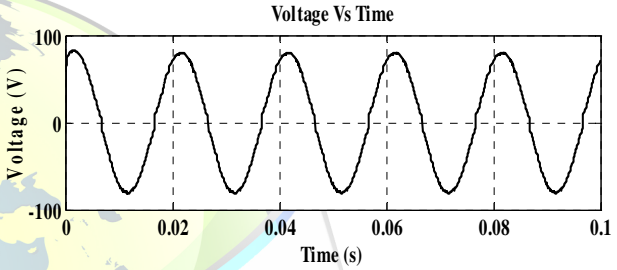

Fig.33 Output voltage waveform of high inductive load for PD technique

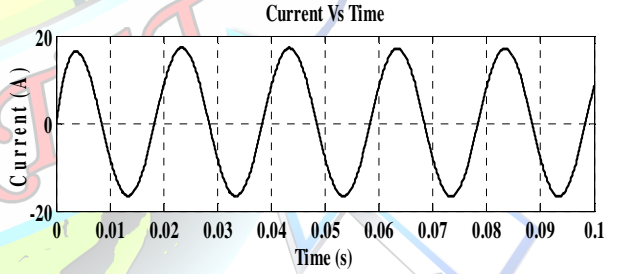

Fig. 34 Output current waveform of high inductive load for PD technique

The Fig. 35 and Fig. 36 shows FFT window of 31-level inverter output voltage and current using PD technique.

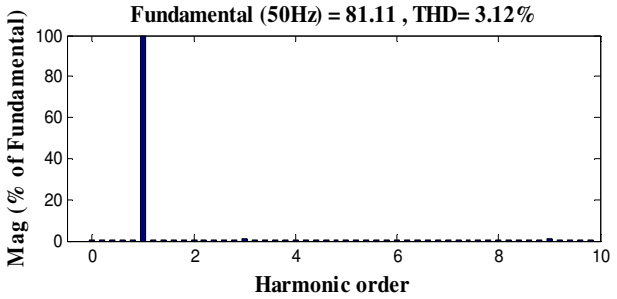

Fig. 35 THD of output voltage for high inductive load

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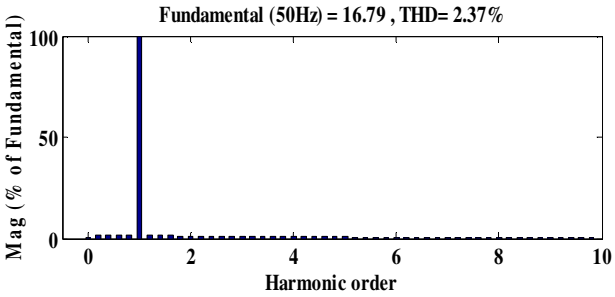

Fig. 36 THD of output current for high inductive load

2) *POD technique*

In POD technique, the voltage and current are in same phase and it produces 31 levels of output with low distortions for high inductive load which is satisfied IEEE standards. The output waveform is nearer to sine wave.The voltage and current waveform for proposed method is shown in Fig. 37 and Fig. 38 for POD technique.

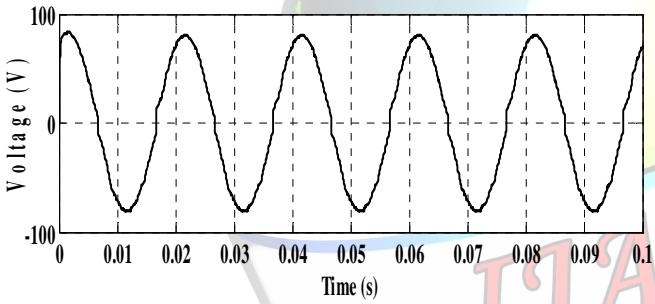

Fig. 37 Output voltage waveform of high inductive load for POD technique

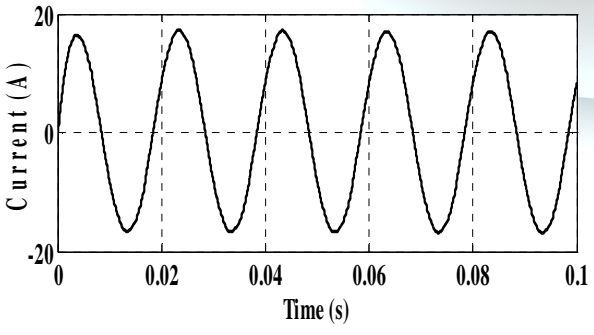

Fig. 38 Output current waveformof high inductive load for POD technique

The Fig. 39 and Fig. 40 shows FFT window of 31-level inverter output voltage and current using POD technique.

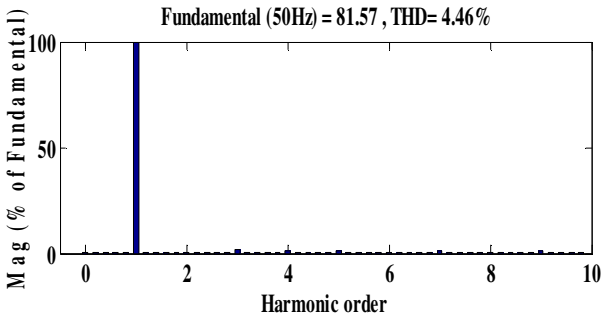

Fig. 39 THD of output voltage for high inductive load

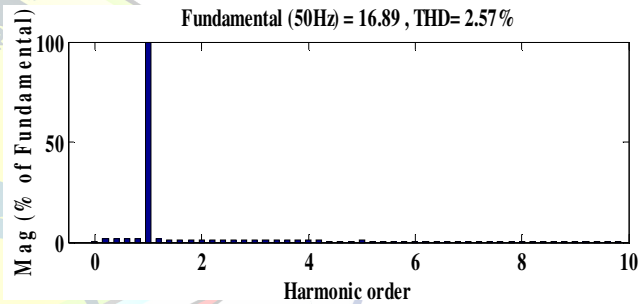

Fig. 40 THD of output current for high inductive load

3) *APOD technique*

In APOD technique, the voltage and current are in same phase and it produces 31 levels of output with low distortions for high inductive load which is satisfied IEEE standards.The output waveform is nearer to sine wave.The voltage and currentwaveformforproposed method is shown inFig. 41andFig. 42 for APOD technique.

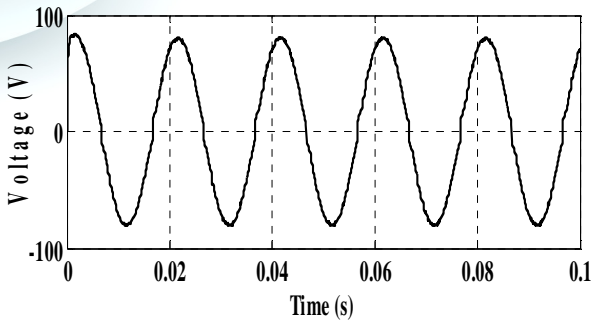

Fig. 41 Output voltage of high inductive loadfor APOD technique

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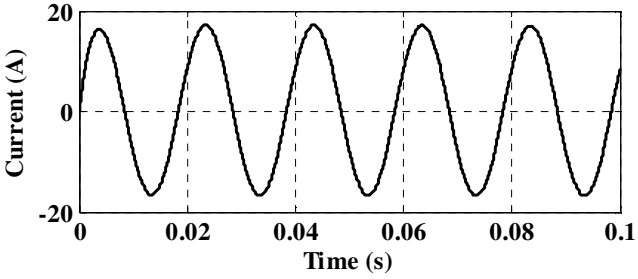

Fig. 42 Output current waveformof high inductive load for APOD technique

The Fig. 43 and Fig. 44 shows FFT window of 31-level inverter output voltage and current using APOD technique.

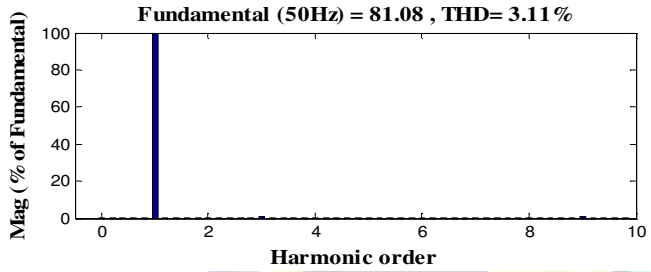

Fig. 43 THD of output voltage for high inductive load

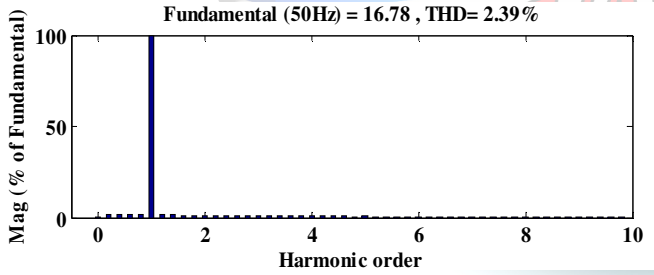

Fig. 44 THD of output current for high inductive load

VIII. THD COMPARISION

THD's of output voltage and current based on simulations results for different modulation techniques are shown in below table 4. According to it, the PD techniques gives THD% of voltage 3.86% and THD% of current 1.97%. The POD techniques gives THD% of voltage 4.09% and THD% of current 2.18%. The APOD techniques gives THD% of voltage 3.81% and THD% of current 1.89%.Based on this analysis, APOD technique gives minimum THD comparing with other two techniques. But all the techniques satisfy the IEEE519 harmonics standard.

TABLE VI

THD COMPARISON OF VOLTAGE AND CURRENT FOR DIFFERENT MODULATION TECHNIQUES

Modulation Technique	*THD Comparison*			
	Low inductive load		*High inductive load*	
	V (%)	*A (%)*	*V (%)*	*A (%)*
PD	*3.86*	*1.97*	*3.12*	*2.37*
POD	*4.09*	*2.18*	*4.46*	*2.57*
APOD	*3.81*	*1.89*	*3.11*	*2.39*

IX. CONCLUSION

In this paper, thirty one level asymmetric multilevel inverter with sinusoidal PWM technique for different modulation techniques are proposed. It also presents the comparison of the proposed asymmetric multilevel inverter with different techniques. By implementing various SPWM techniques, it is found that the APOD is the best technique that has less THD. It can be easily extended to higher number of level It can be used to form high voltage outputs with low stress on semiconductors switches and lowering the number of devices. The main advantage of proposed module is its ability to generate both positive and negative output voltage with H-bridge circuit at the output of the inverter. THD% of voltage is obtained 3.81% and THD% of current is obtained 1.89for low inductive load in simulation results.THD% of voltage is obtained 3.12% and THD% of current is obtained 2.37 for high inductive load

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in simulation results. According to IEEE, the maximum THD is 5%. It is satisfied by proposed method. Also module is applicable to simulated under different resistive – inductive loads.

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