



A Phase-Shifted Gating Technique With Simplified Current Sensing for the Semi-Bridgeless AC-AC Converter

Mr.M.Suresh¹ M.E., Mr.J.Megan David² M.E.,
Assistant Professor¹, Assistant Professor²
DMI College of Engineering, Chennai- 602-103,Tamil Nadu.
sureshmahalingam079@gmail.com, megan.starofdavid@gmail.com

Abstract

In this project, a phase-shifted simplified bridgeless boost power-factor-corrected (PFC) converter is proposed to ac grid interface application through inverter with easy arrangement of the current-sensing technique. The converter is applicable for automotive levels I and II but is ideally suited for level-I residential charging applications. A detailed converter description and steady-state operation analysis of this converter is presented inverter provided pure ac and also it's overcome the drawback of basic inverter. The converter features high efficiency at light loads and low ac input lines, which is critical to minimize the charger size, charging time, and amount and cost of electricity drawn from the utility.

Index Terms—AC-AC power converters, boost converter, semi-bridgeless power factor correction (PFC), current sensing, and plug-in hybrid electric vehicle (PHEV) charger.

Introduction

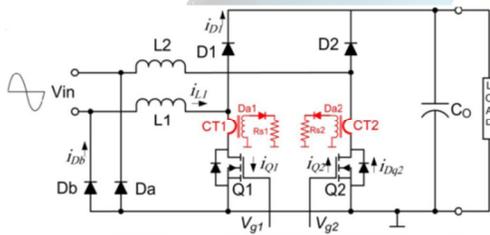
A PLUG-IN hybrid electric vehicle (PHEV) is a hybrid vehicle with a storage system that can be recharged by connecting a plug to an external electric power source. The charging ac outlet inevitably needs an onboard ac-dc charger with power factor correction (PFC). An onboard 3.3-kW charger could charge a depleted battery pack in PHEVs to 95% charge in about 4h from a 240-V supply for a 10-kWh battery pack.

A variety of circuit topologies and control methods has been developed for PHEV battery chargers. The two-stage approach with cascaded PFC ac-dc and dc-dc converters is the common architecture of choice for PHEV battery chargers, where the power rating is relatively high, and lithium-ion batteries are used as the main energy storage system. The single-stage approach is generally only suitable for lead acid batteries due to a large low-frequency ripple in the output current. In the two-stage architecture, the PFC stage rectifies the input ac voltage and transfers it into a regulated intermediate dc-link bus. At the same time, PFC is achieved. A boost-derived PFC topology operated in continuous conduction mode is used in this paper as the main candidate for the front-end ac-dc PFC converter for PHEV battery charging. The front-end candidate topologies in the boost-derived class include the following: the interleaved boost converter, the bridgeless boost converter, the semi-bridgeless boost converter, and the proposed phase-shifted semi-bridgeless (PSSB) boost converter.

Semi-Bridgeless PFC

The semi-bridgeless configuration, as shown in Fig. 6, includes the conventional bridgeless topology with two additional

slow diodes, namely, D_a and D_b that connect the input to the PFC ground. The slow diodes were added to address EMI related issues. The current does not always return through these diodes; therefore, their associated conduction losses are low. This occurs since the inductors exhibit low impedance at the line frequency; thus, a large portion of the current flows through the MOSFET intrinsic body diodes. The semi-bridgeless configuration also resolves the floating input line problem with respect to the PFC stage ground. The topology change enables input voltage sensing using a string of simple voltage dividers.



PSSB PFC boost topology with a simple current-sensing circuit

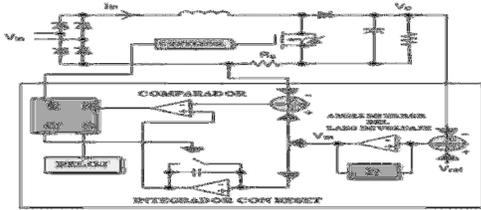
The PSSB topology shown in Fig. 8 is proposed as a solution to simplify current sensing in bridgeless PFC boost applications using the current synthesizer sensing method [27]. The inductor current synthesizer technique is used to predict the boost inductor current by sensing the MOSFET current [28]. The proposed topology power train incorporates the decoupled MOSFET gates, similar to that of the dual boost, and uses two slow diodes (D_a and D_b), similar to that of the semi-bridgeless boost, to link the ground of the PFC to the input line. The gating signals for the MOSFETs are 180° out of phase, as shown in Fig. 9. The phase-shifted gating enables the usage of the

advanced current synthesizing method, which cannot be used in either the bridgeless topology or the dual-boost topology because all controllers available for these topologies require full input current shape sensing. The proposed topology exploits the advantages of the bridgeless and semi-bridgeless boost PFC topologies. In particular, it features reduced EMI, high efficiency at light loads, and low lines, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility.

Proposed Phase-Shifted Semi-Bridgeless Converter

The One Cycle Control is a new technique that has shown the same results in performance and efficiency, comparing with the multiplier based approach, but the One Cycle Control has the advantages of less Complexity and reduction in component count. The basic schematic diagram of this control technique for a Boost converter.

A key aspect of the OCC control method is the fact that this ramp created by the integrator circuit is reset at the end of each switching cycle and the ramp starts again from zero at the beginning of the subsequent cycle. Accordingly, this method is apply termed, OCC, or “One Cycle Control”. The core of the One Cycle control is a resettable integrator. This block integrates the modulation voltage V_m and is reset at the end of every switching cycle.

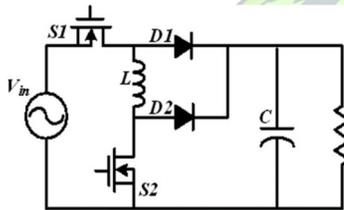


Circuit diagram for the proposed system

conduction mode (DCM) is provided along with the averaged large signal modeling.

The design procedures and guidelines are discussed in Section IV. Section V addresses the control schemes for DCM. Experiment results are reported to verify the previous theoretical analysis in Section VI. Section VII presents the conclusions.

Bridgeless AC TO DC



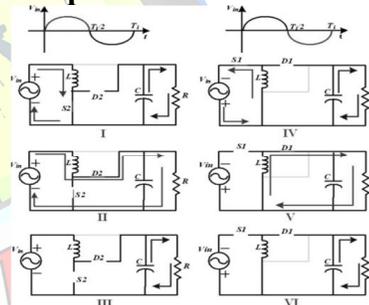
Bridgeless AC to DC

A new bridgeless boost rectifier, shown in Fig. 4, which is a unique integration of boost and buck-boost converters, is proposed in this paper. When the input voltage is positive, $S1$ is turned ON and $D1$ is reverse biased, the circuitry operates in the boost mode. As soon as the input voltage becomes negative, the buck-boost mode starts with turning ON $S2$ and reverse biasing $D2$.

MOSFETs with bidirectional conduction capability work as two-quadrant switches to ensure the circuitry functionality in both positive and negative voltage cycles. This topology was introduced in [25] for piezoelectric energy harvesting applications.

The circuit operation modes are described in Section II. In Section III, a detailed analysis of discontinuous

Mode of Operation



Mode of Operation

In electromagnetic energy harvesters, the internal oscillation between coils and magnet produces a periodically variable magnetic flux in the coil, which induces a corresponding output voltage. The power electronics interface (PEI) is employed to supply constant voltage and to deliver power to the load. In order to facilitate and simplify analyses, it is assumed that the input impedance of the PEI is significantly larger than the internal impedance of energy harvesting device.

The induced voltage could be assumed to be a low amplitude sinusoidal ac voltage source. As the frequency of vibration source and induced voltage



(usually less than 100 Hz) is much less in comparison to that of the switching frequency (around tens of kHz), the induced ac voltage can be assumed as a constant voltage source in each switching period. In this paper, a 0.4-V, 100-Hz sinusoidal ac voltage source is adopted to emulate the output of the electromagnetic energy harvester.

The DCM operating modes of the proposed boost rectifier are shown in Fig. 5. Each cycle of the input ac voltage can be divided into six operation modes. Modes I–III illustrate the circuit operation during positive input cycle, where $S1$ is turned ON while $D1$ is reverse biased. The converter operates as a boost circuit during Modes I–III, while switching $S2$ and $D2$. The operation during negative input cycle is demonstrated in Modes IV–VI, where $S2$ is turned ON while $D2$ is reverse biased. In these modes, the converter operates similar to a buck boost circuit.

Mode I: This mode begins when $S2$ is turned ON at t_0 . The inductor current is zero at t_0 . The turn on of $S2$ is achieved through zero current switching (ZCS) to reduce switching loss. Inductor L is energized by the input voltage as both $S1$ and $S2$ are conducting. Both diodes are reverse biased. The load is powered by the energy stored in the output filter capacitor C .

Mode II: $S2$ is turned OFF at t_1 , where $t_1 - t_0 = d_1 T_s$, d_1 is the duty cycle of the boost operation, and T_s is the switching period. The energy stored in the inductor during Mode I is transferred to the load. The inductor current decreases linearly. During this mode, switching loss occurs during the turn on of diode $D2$.

Mode III: $D2$ is automatically turned OFF as soon as the inductor current becomes zero at t_2 ($t_2 - t_1 = d_2 T_s$). This avoids the reverse recovery loss of diode. The load is again powered by the stored energy in the capacitor. The converter would return to Mode I as soon as $S2$ is turned ON, if the input voltage is still in positive cycle.

Mode IV: During the negative input cycle, Mode IV starts as soon as $S1$ is turned ON at t_0 . ZCS condition can also be achieved by ensuring the converter operation in DCM. The energy is transferred to the inductor L again, while the output filter capacitor C feeds the load.

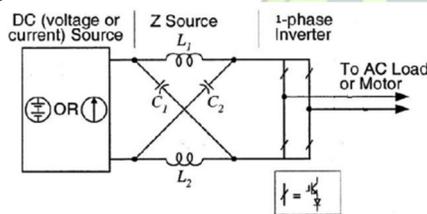
Mode V: At t_1 , $S1$ is turned OFF, where $t_1 - t_0 = d_1 T_s$, d_1 is the duty cycle of the buck-boost operation. The energy stored in the inductor during Mode IV is transferred to the load. The inductor current decreases linearly. During this mode, switching loss occurs during the turn on of the diode $D1$.

Mode VI: When the inductor current decreases to zero at t_2 ($t_2 - t_1 = d_2 T_s$), $D1$ is turned OFF at zero current. The load is continuously powered by the charge stored in the output capacitor. The converter would return to Mode IV as soon as $S1$ is turned ON, if the input voltage is still negative.

Z-Source Inverter

The new impedance-source power inverter has been recently invented, eliminates all problems of the traditional V-source and I-source inverters. It is being used in ac/dc power conversion applications. The power source can be either voltage source or current source. The Z-source inverter consists of a unique impedance network which couple the converter main

circuit to the power source, load, or other converter, for providing unique features that cannot be observed in the traditional VSI and CSI inverters. The impedance network consists of two inductors and two capacitors connected to each other as shown in the figure forms the second order filter network. The values of both inductor and both capacitor are equal. The two inductors can be two separate inductors or two inductors inductively coupled to each other on a single core. For size and cost reduction film capacitors of desired value and voltage rating can be selected.



Z-Source inverter structure

Power Factor Correction

For phase-controlled operation in both single phase full wave half and full controlled bridge converters as discussed in this module (#2), the displacement factor (or power factor, which is lagging) decreases, as the average value of output voltage (V_{dc}) decreases, with the increase in firing angle delay, α . This is also applicable for both three phase half wave and full wave (bridge) converters.

Filters

It is known that the output voltage waveform of a single phase full wave diode (uncontrolled) bridge converter (rectifier) fed from $f = 50$ Hz (fundamental) supply, contains harmonics of $2f = 100$ Hz. So, it is necessary to filter out this and other harmonics from the output voltage to obtain

dc component only. The harmonic frequency present in the output voltage waveforms of three-phase half-wave and full wave (bridge) diode converters are 150 Hz ($3f$) and 300 Hz ($6f$) respectively. The higher the harmonic frequency, it is easier to filter it. For phase-controlled thyristor converters, the harmonic frequency remains same, but magnitudes vary, as the firing angle delay, α is changed. It may also be noted that the harmonics present in the output current waveforms of the converters with resistive (R) load, remain same.

For simple filter, a capacitor (C) is connected in parallel across the output of the diode converters with resistive (R) load. The reactance of the capacitor should be low, such that harmonics currents pass through it. So, the harmonics in the output voltage decrease. The value of the capacitor chosen varies with the predominant harmonic frequency present. Thus, the capacitor of higher value is needed to filter lower

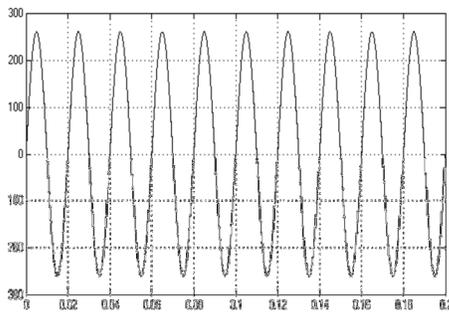
harmonic frequency, say 100 Hz, whereas a lower value of C could be chosen for say, three phase converters. The function of the capacitor may also be explained in the following way. The voltage across the capacitor changes as per the input voltage, which is the output voltage of the converter, fed to it and the capacitor voltage tries to stabilize at the average value of the output voltage, as the capacitor voltage decreases, load resistance being connected across it.

Same is the case with the filter used to reduce the harmonic content of the output current waveform for the above converters with resistive (R) load. Instead of a capacitor in parallel, an inductor (L) is connected in series with the load. The reactance of the inductor increases, thus reducing the harmonic component in the current waveform. Here, a smaller value of the

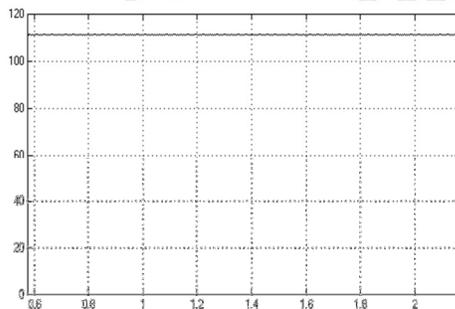


inductor is needed to filter higher harmonics, for example a three-phase bridge converter. Also, by Faraday's laws, induced voltage (emf) appears across the inductor, L , when the current through it changes, and the sign of it opposes the cause, thus opposing the changes in current. So, the current is not allowed to change much, as an inductor is placed in series with the load. In actual practice, a combination of L , C & R is needed to get an optimum filter needed to reduce or eliminate the harmonics in both output voltage and current waveforms.

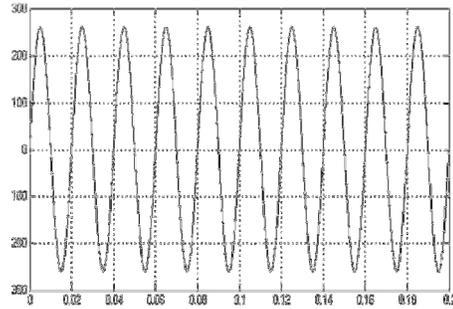
Experimental Results



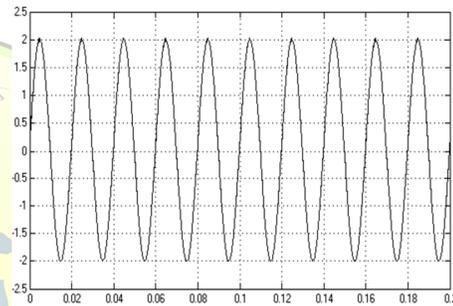
AC Input Voltage



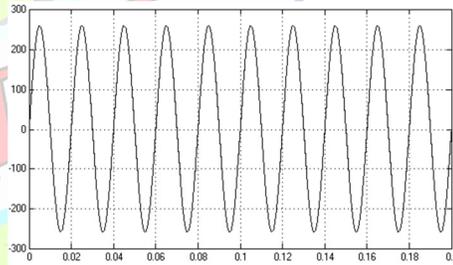
DC Output Voltage



AC Input Voltage



Power Factor Correction



AC Output Voltage

CONCLUSION AND FUTURE SCOPE

This thesis has demonstrated the state of the art of AC –DC-AC converter technology. Fundamental multilevel converter structures and modulation paradigms including the proposed and cons of each technique have been discussed. Most of the thesis focus has addressed modern and more practical industrial applications of multilevel converters. It should be noted that this thesis could not cover all multilevel power converter related applications; however the



basic principles of different converters have been discussed methodically. The main objective of this thesis is to provide a general notion about the multilevel power converters and various modulation strategies mainly PWM techniques and their applications. As a future work it is possible to develop an optimization of the PI controller implemented to the inverter system, with the purpose of increasing its output speed, since the natural sampling has a delay of approximately 8333 μ s in the sensed method. This can be improved using an instantaneous sampling of the signal, in other words, applying the predictive current control method.

References

- [1] B. Lu, R. Brown, and M. Oldano, "Bridgeless PFC implementation using one cycle control technique," in *Proc. IEEE Appl. Power Electron. Conf. Expo.* 2005, vol. 2, pp. 812–817.
- [2] L. Balogh and R. Redl, "Power-factor correction with interleaved boost converters in continuous-inductor-current mode," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1993, pp. 168–174.
- [3] W. Y. Choi, J. M. Kwon, E. H. Kim, J. J. Lee, and B. H. Kwon, "Bridgeless boost rectifier with low conduction losses and reduced diode reverse recovery problems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 769–780, Apr. 2007.
- [4] W. Frank, M. Reddig, and M. Schlenk, "New control methods for rectifier less PFC-stages," in *Proc. IEEE Int. Symp. Ind. Electron.* 2005, vol. 2, pp. 489–493.
- [5] Fang Zheng Peng, *Senior Member, IEEE*, Lihua Chen, and Fan Zhang, "Simple Topologies of PWM AC–AC Converters" *IEEE Power Electronics Letters*, Vol. 1, No. 1, March 2003.
- [6] Martin Glinka, *Member, IEEE*, and Rainer Marquardt, "A New AC/AC Multilevel Converter Family," *IEEE Transactions on Industrial Electronics*, Vol. 52, No. 3, June 2005.
- [7] M. Ramezani and S. M. Madani, "New zero-voltage-switching bridgeless, using an improved auxiliary circuit," *IET Power Electron.*, vol. 4, no. 6, pp. 732–741, Jul. 2011.
- [8] L. Petersen and M. Andersen, "Two-stage power factor corrected power supplies: The low component-stress approach," in *Proc. IEEE APEC*, 2002, vol. 2, pp. 1195–1201.
- [9] C. Petrea and M. Lucanu, "Bridgeless power factor correction converter working at high load variations," in *Proc. ISSCS*, 2007, vol. 2, pp. 1–4.
- [10] J. Zhang, B. Su, and Z. Lu, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electron.*, vol. 5, no. 3, pp. 358–365, Mar. 2012.