SPEED CONTROL OF DC MOTOR USING FPGA

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Abstract: In this paper we are presenting an over view of FPGA (Field Programmable Gate Array) based control of DC drive, over other control category like DSP, microcontroller etc. FPGA is a programmable logic device which is considered as an efficient hardware for rapid prototyping in which architecture is not fixed, & it can be programmed such a way that, we can develop flexible control architecture for necessary control of a DC drive in either open loop or closed loop. This paper gives necessary consideration & comparison for implementing FPGA as a controller over other control methods. This paper gives the design and implementation of a single-phase converter (H-Bridge) that produces a dc output voltage of desired magnitude and frequency. FPGA controller is used to take the digital form of input of different circuit controllable parameter like voltage, current, torque, speed etc generates the necessary command signals which in turn switches the converter to obtain necessary control. The driver circuit isolates the control circuit from power circuit.

Index terms: Introduction, FPGA, proposed Block diagram, PWM inverter & techniques, control algorithm, Hardware implementation

I. INTRODUCTION:

The primary function of any adjustable speed motor drive is to control the speed, torque, acceleration, deceleration and direction of rotation of machine. Unlike constant speed systems, the adjustable drive permits the selection of infinite number of speeds within its operating range. Most multipurpose production machines benefit from adjustable speed control, since frequently their speed must change to optimize the machine process or adapt it to various tasks for improved product quality, production speed or safety. The controller circuit should be flexible so that any change required to control is done without replacing the hardware. Hence from the flexibility point, FPGA can be preferred & implemented as a controller for DC drive control application.

II. FPGA AN OVERVIEW: A Field Programmable Gate Array is a reconfigurable digital integrated circuit that can be programmed to do any type of digital function. The FPGA has logic elements arranged in rows and columns as shown. Each logic element has certain hardware resources, which will be utilized to realize the user logic. The choice of an FPGA device for a given application is based on the size required (number of logic elements), clock speed and number of I/O pins. XILINX & ALTERA are the leading, FPGA manufacturers industries.

The FPGA consists of three major configurable elements as shown in figure 1

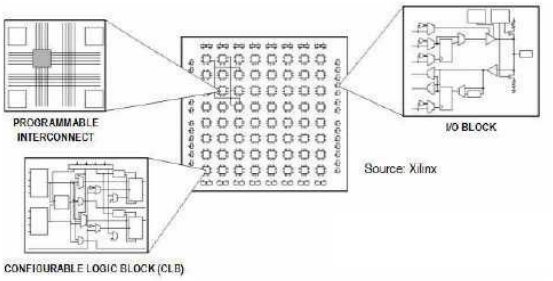

Figure 1. Internal structure of FPGA

Configurable Logic Blocks (CLBs) arranged in an array that provides the functional elements and implements most of the logic in a FPGA. Input-output blocks (IOBs) that provide the interface between the package pins and internal signal lines. Programmable interconnects that provide routing path to connect inputs and outputs of CLBs and IOBs to the appropriate network .FPGA supports hardware that is upwards of one million gates, which can be re programmed to upgrade the design & re use the same hardware , which can decrease E-waste to environment .

Once they are programmed, they can be disconnected from the computer and will retain their functionality until the power is removed from the chip.

The FPGAs can be programmed while they run, because they can be reprogrammable in the order of microseconds. FPGAs are programmed using support software and a download cable connected to a host computer. Once they are programmed, they can be disconnected from the computer and will retain their functionality until the power is removed from the chip. The FPGAs can be programmed while they run, because they can be reprogrammable in the order of microseconds.

VERILOG & VHDL are hardware description language used to describe electronic circuits and digital systems. In practice it is generally used for simulating, testing, and programming PLD's (programmable logic devices) or FPGA s other similar hardware. We have chosen Verilog over VHDL because it is easier to learn and use for most people because it looks like the C language in syntax.

Verilog is a language that includes special features for circuit modeling and simulation.

WHY FPGA?

DSP & Micro-controllers technology offering increasing performance you might wonder how FPGAs could be the next stage in the evolution of motor control. FPGAs has no fixed architecture , hence its architecture can be designed & implemented to match required control process , at any instant , without changing existing hardware.FPGAs give designers the freedom to create custom functions completely adapted to their specific application requirements by enabling both hardware and software customization. An FPGA-based motor controller offers completely deterministic performance and enhanced product reliability compared to the serial instruction-execution approaches of MCUs or DSPs.

Why it is better option to go for FPGA? , can be understood well from its following advantages.

Unlike an **ASIC (Application Specific Integrated Circuit)** which can perform a single specific function for the lifetime of the chip, an FPGA can be reprogrammed to perform different function in a matter of microseconds.

DSP processor/ microcontrollers are sequential machines i.e. tasks are executed sequentially which take longer processing time, whereas FPGA can be configured to

perform independent functions simultaneously.

DSP processor/ microcontrollers **architecture & hardware is fixed**, so **software is the only option**, where designer can change control logic or control characteristic. Whereas in FPGA hardware is flexible & reconfigured.

Bit length of the digital word is limited in DSP processor/ microcontrollers but not in FPGA.

Control technique cost of FPGA is low compared to DSP processor/ microcontrollers.

FPGA can be **re-programmed when they are running in real time**.

FPGA has ability to **operate faster, higher processing power, & supports hardware** i.e. Upwards of one million gates.

III. BLOCK DIAGRAM PROPOSED:

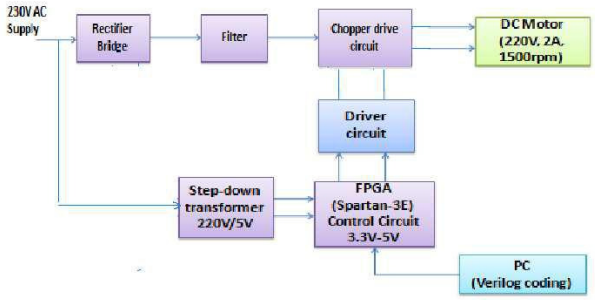

Figure 2. Overall Block Diagram

Power supply: DC drive, FPGA chip & other instrumentation devices needs sufficient & compactable power for their working and it's fulfilled by power supply block. In case of self contained unit power requirements can be fulfilled directly by battery systems.

Rectifier with capacitive filter: if the available power source is AC then, AC power required to run a DC drive, initially converted to DC by rectifier circuit designed for motor applications. Purpose of DC link is to limit the current & to provide pure DC output.

Drive circuit Isolation: The Driver circuit isolates FPGA & H-Bridge circuit & gives the required gate signals to switching devices (MOSFET) depending on output of the FPGA, which in turn controls the operation of the DC motor.

PWM Converter & Techniques: The basic full bridge MOSFET or IGBT based converter is shown in figure 3. The PWM signals are applied to gate of power switch with the help of driver circuit through isolation circuit.

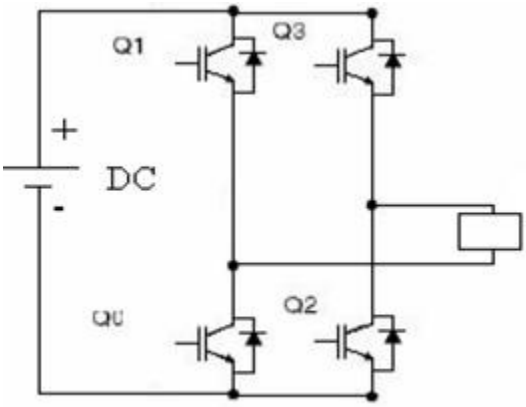

Figure 3. Full Bridge Converter

PWM techniques are of two types Analog & Digital Techniques. In analog techniques there is a **carrier signal** and a **modulating signal**. These two signals are compared using comparator. The output of this comparator is the desired PWM output. Disadvantages of these analog methods are, that they are prone to noise and they change with voltage and temperature change. They suffer changes due to component variation. They are less flexible as compared to digital

methods. Digital methods are the most suited form for designing PWM Generators. They are very flexible and less sensitive to environmental noise. Also they are simple to construct and can be implemented very fast and can be implemented easily using DSP, MCU, FPGAs

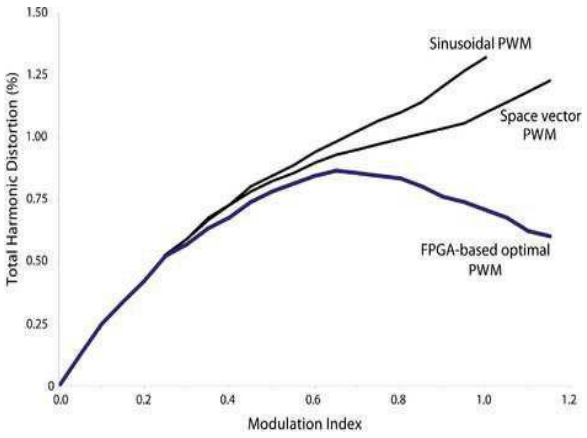

Figure 4. THD v/s Modulation INdex

FPGA can reduce **THD (Total Harmonic Distortion)** by 30% to 50% at high modulation index as shown in figure 4, so that less audible noise .Hence FPGA can be selected.

IV. HARDWARE IMPLEMENTATION & RESULT

An AC power supply of 220V, 50Hz is converted into DC with the help of a rectifier bridge with filter. The Rectifier Bridge used in this paper is BR68 (800V, 6A) and a capacitor bus of about 1000µF.

The power switch used is n-Channel MOSFET (IRFP450) with a Vdss of 500V. The power switch is driven with the help of a driver circuit as showh in figure 5.

A half-bridge driver IC IR2110 is used to drive both the high side and low side of the bridge. The low side is implemented either with two N-Channel MOSFETs or with an N-Channel and a P-Channel CMOS inverter stage. Each MOSFET can sink or source gate currents from 0.25 to 2A. The high side has been built into an "isolation tub" capable of floating from 500 or 600V to -5V with respect to power ground (COM). Typically this pin is connected to the source of the high side device, and swings with it between the two rails. If an isolated supply is connected between this pin and Vs , the high side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command. If the high side channel is driving one such device, the isolated supply can be replaced by a capacitor. The gate charge for the high side MOSFET is provided by the bootstrap capacitor which is charged by the 15V supply through the bootstrap diode during the time when the device is off.

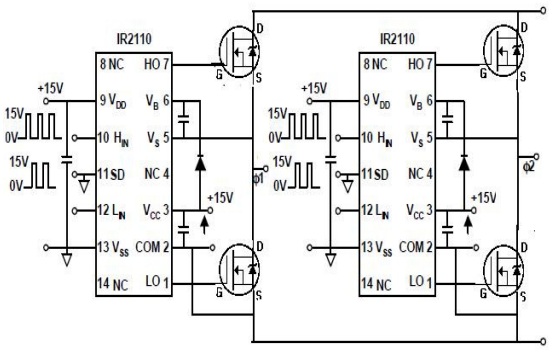

Figure 5. H-Bridge Implementation using driver IR2110

Isolation is provided between the power circuit and controller to protect the FPGA controller from power section. 4N25 opto-coupler is used here where the grounds are separated, and Voltage spikes are suppressed. The isolator is followed by a npn transistor which is used for amplification which provides inverted signal to the driver circuit.

The gate pulses to trigger the MOSFETs are given from the control circuit i.e., FPGA

controller (SPARTAN 3E family). The control algorithm is shown in figure 6. A Verilog code for generating a PWM pulses are generated in which the internal crystal oscillator frequency is reduced to our requirement and required PWM pulses to trigger the switch is generated.

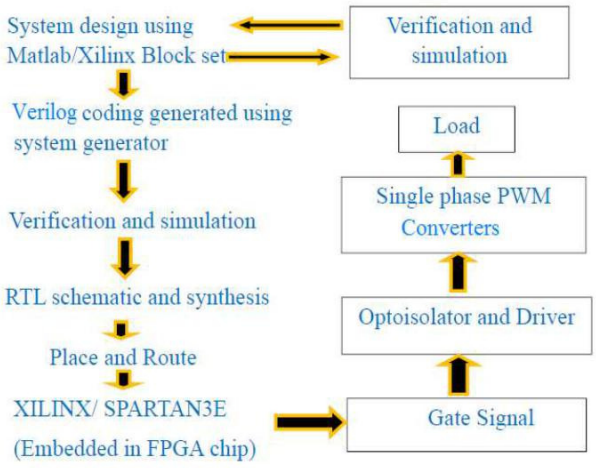

Figure 6. Control algorithm

The verilog program is written in Xilinx ISE software. The program is transferred from PC to the SPARTAN 3E kit through JTAG or RS323 port. After the program is executed and run, it is interfaced with the circuit which in turn will run the DC motor..

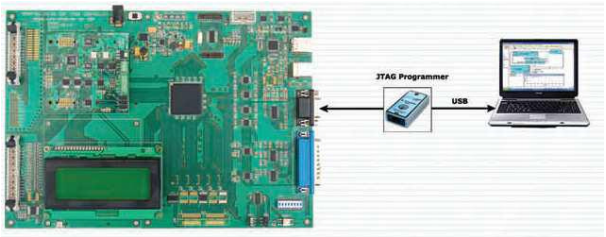

Figure 7. Interface between PC and FPGA

The program is written for a four set values of duty cycle. The figure 8 shows an output for 40% duty cycle and a switching frequency of about 10kHz. When the duty cycle is increased, the voltage to trigger the switch will increase and this in turn will increase the speed of the dc motor.

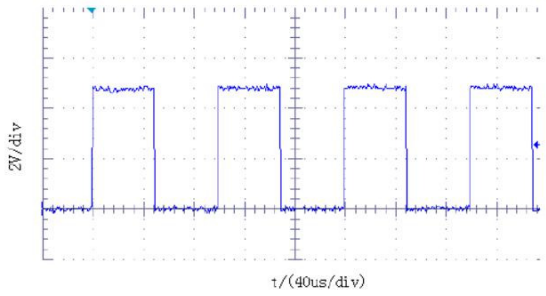

Figure 8. 10 KHz PWM signal generated by FPGA

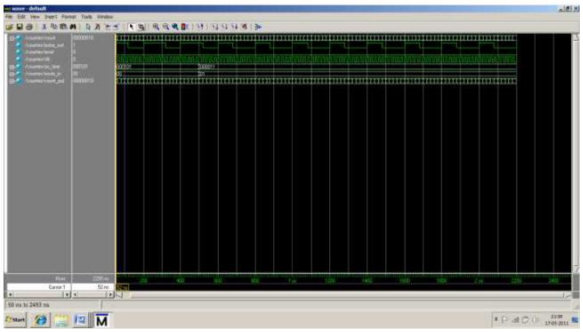

Figure 9

V. CONCLUSION

FPGA based digital platform is more suitable for the control applications in Power electronic systems. The use of FPGAs in control applications not only increases the performance of the system but also reduces the cost and size of the controller.

FPGA platform can also be used for many Applications such as Front-end converters, uninterrupted power supplies, Inverters and phase-controlled rectifiers.

As a conclusion, the design of the switching pulses using FPGA technology shall produce better control signal for converter switches. With the high programming flexibility, the design of the switching pulse can be further altered easily without any further changes on the hardware.

Choosing the correct devices for the heart of any system is very difficult and is made even harder by the emergence of new technologies such as Field Programmable Gate Arrays (FPGA). The only certainties are that the system will invariably have a processing engine of some type, some memory, and logic. We also know with some certainty that choices made in the design phase impact heavily on the total life cycle costs of the end product, so this decision is key to any major project. This decision will be based on time-to-market, costs, cost of change, obsolescence concerns (and the costs associated with this), and cost to service and maintain in the field.

FPGAs are a viable alternative to custom microprocessors as they can offer a shorter Time cycle to market, can offer re-usable options, can be used across many platforms/PCBs to reduce inventory costs, and when using them in conjunction with a soft core embedded processor, can solve the Device obsolescence problem. The following table gives clear picture , for selecting FPGA controller over other control methods from different points like cost, speed, reprogram time, reusability etc

VI. REFERENCES:

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