

MODELLING AND SIMULATION OF NEW COUPLED INDUCTOR BASED CIRCUIT BREAKER FOR DC APPLICATIONS

¹PUTTAPATI PRAVEEN KUMAR, ²VENKATA PADMAVATHI.S, ³DR.P.VASUDEVA NAIDU

¹Student, M.Tech GITAM (DEEMED TO BE UNIVERSITY) Hyderabad, Telangana India.

² Assistant Professor, M.E (AU TN), (Ph.D) GITAM (DEEMED TO BE UNIVERSITY) Hyderabad, Telangana India.

³ Head of EEE Department, Ph.D, GITAM (DEEMED TO BE UNIVERSITY) Hyderabad Telangana India.

ABSTRACT: According to the paper we are developing the new type of DC circuit breaker. In order to reduce the power conversion step for future micro grid with the renewable energy source which is best for the DC power system. Therefore according to the system components like source, load and the power conversion which can identify easy and ready to use. there the main limitation is to interrupting a current which does not have a zero crossing will sustain an arc. Here we are utilizing the short conduction path between the breaker and load along with mutual coupling to automatically and rapidly switch OFF in response to a fault. Therefore here the proposed circuit breaker which is crowbar type switch at the output and it is utilized as the dc switch. By using the simulation result and also by Mathematical analysis of the new dc switch.

Index Terms—Circuit breaker, fault location, fault protection, thyristor switch.

INTRODUCTION

According to the DC electric power which have various beneficial in the modern applications, such as electric ships, data centers, micro grids with renewable energy, and future applications such as the dc home. As researchers consider design of dc power systems, fault protection, and the circuit breaker are of significant interest. Along these lines mechanical breakers for ac systems can be used [1], but with limited range. Hybrid mechanical/solid-state breakers have been introduced [2]–[5] with the benefit of low losses. Another protection method that has been suggested is to utilize converters and associated control [6]–[9]. Alternatively, solid-state dc circuit breakers have been considered [10]. These breakers offer rapid response to faults, but tend to have higher power losses.

There are various advantages of circuit breaker such as very rapid operation and automatic disconnection of faulty loads. Therefore in this paper we are implementing a new concept in dc circuit

breakers which is closely related to the z-source dc breaker, but with utilization of transformer coupling. Only recently have researchers suggested coupled inductors not only for fault detection, but for automatic isolation. As shown below, the breaker introduced herein has advantages over the z-source breaker in terms of requiring fewer components. It also has a settable level for fault current; that is through breaker design the transformer turns ratio can be selected to specify how much fault current is needed for the breaker to operate.

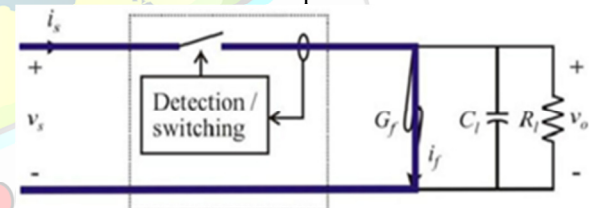
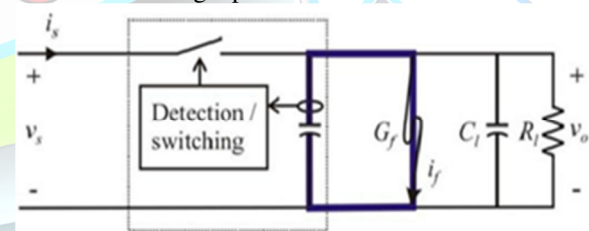


Fig. 1. Fault sensing techniques (a) Fault sensing using a path from the source.



(b) Fault sensing using a path from the breaker

According to the Fig. 1(a) which shows a typical arrangement of a circuit breaker inserted between a source and load. In this circuit, the source current is monitored for fault current detection. Alternatively, a capacitor can be connected to ground within the breaker as shown in Fig. 1(b). This method is good for detecting transient currents and is used in motor drives for detection of shoot through. That is, a small capacitor in series with some type of current sensor can be connected to the dc bus of a drive. Shoot through faults create an impulse of current in

this capacitor and the detection can immediately switch OFF the drive's gate signals.

PROPOSED DC PROTECTION CIRCUIT

Now, the abovementioned technique is admirable but, in addition, the short path can be used as a means of switching the breaker off in response to a fault. Consider the proposed dc circuit breaker shown in Fig. 2. During the normal steady-state operation, current flows from the source to the load through the SCR and coupled inductors. A fault on the load side will cause an impulse current i_c in the short path containing the capacitor

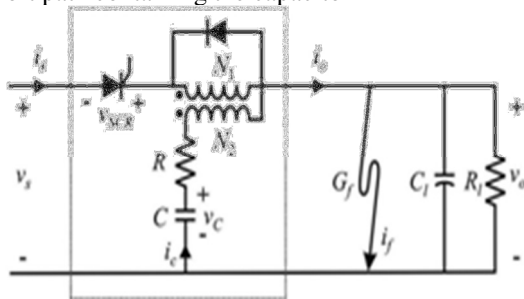


Fig. 2. Proposed dc circuit breaker

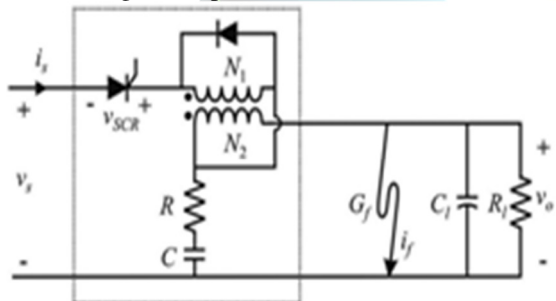


Fig. 3. Variation of the proposed dc circuit breaker. and secondary winding of the coupled inductors. With a turn's ratio, this current is reflected to the primary and essentially pushes the SCR current to zero; at which time the SCR switches OFF. It should be noted that the turn's ratio N_1/N_2 can also be set so that the breaker does not identify a large change in load as a fault.

An alternate approach to the proposed breaker is the variation shown in Fig. 3. In this circuit, the main path current flows through the primary and secondary windings. As with the circuit of Fig. 2, the fault current flows through the secondary winding and causes the SCR current to go to zero.

A. Step Load Analysis

One of the main features of the proposed dc switch is its ability to remain on during a step change

in load. Therefore, it is helpful to know how to design the transformer component and know exactly what type of step in load will cause the breaker to switch OFF. From Fig. 1 and neglecting transformer magnetizing current

$$i_o = i_s - \frac{N_2}{N_1} i_c \quad (1)$$

For steady-state operation, the capacitor current is zero and the source current is equal to the output current. Assuming that a sudden change in output current is entirely represented by a change in capacitor current, that is

$$\Delta i_o \approx \Delta i_c \quad (2)$$

By transformer action

$$\Delta i_c \approx -\frac{N_2}{N_1} \Delta i_o \approx -\frac{N_2}{N_1} \Delta i_o \quad (3)$$

Now, with an initial output current of

$$i_o = i_o \quad (4)$$

the response of the source current to a change in output current will be

$$i_s = i_o - \frac{N_2}{N_1} \Delta i_o \quad (5)$$

This source current, and, thus, the SCR current, will go to zero when the change in output meets the condition

$$\Delta i_o > \frac{N_1}{N_2} i_o \quad (6)$$

Therefore, (6) can be used to determine the amount of change in output current that will result in the breaker switching OFF. This can also be used to select a turn's ratio to ensure that the breaker will not switch OFF during expected load transients.

B. **Circuit Design** :The breaker designs starts with choosing a wire size and carrying out a design for the transformer primary winding. In this case, the wire size has a cross-sectional area of 0.82 mm². For this design, the transformer is going to be an air-core type wound around a square capacitor having dimensions of 70 mm × 57.5 mm. A number of turns are selected and 5% leakage inductance is assumed. The resulting parameters are displayed in Table I.

Table I
Parameters Of The Test System

$N_1 = 70$	$r_1 = 0.373 \Omega$	$L_{l1} = 51 \mu\text{H}$	$L_{m1} = 960 \mu\text{H}$
$N_2 = 24$	$r_2 = 0.128 \Omega$	$L_{l2} = 6 \mu\text{H}$	$L_{m2} = 116 \mu\text{H}$
$R = 0.2 \Omega$	$C = 100 \mu\text{F}$		
$V_{RRM} = 400 \text{ V}$	$I_{TRMS} = 40 \text{ A}$	$t_q = 35 \mu\text{s}$	

In this case, a turns ratio of approximately three is selected so that the transient load current can

step by about 300%, as per (6), without switching the breaker off. Using the same wire size as the primary, the secondary parameters are computed and shown in Table I. In this design, the SCR total turn-off time t_q is taken into account and the resonance formed by L_{m2} and C is set that so a quarter cycle [18] is three times the turn-off time. This results in the value of capacitance in listed Table I. Finally, the resistance is set to a low value as not to interfere with the breaker performance, but still provide damping of the oscillations which occur when the breaker is switched OFF. The last row of Table I shows the SCR ratings. A laboratory test system operating with a 100-V 6-A dc load would be within the ratings of the SCR.

C. Circuit Analysis : according to the Fig. 4 shows the equivalent circuit of the proposed breaker with the SCR conducting. In this circuit, the transformer resistance and leakage inductance are neglected.

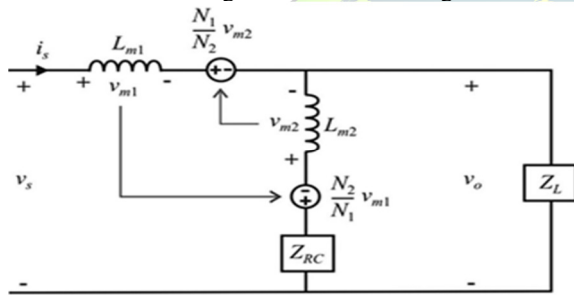


Fig. 4. Equivalent circuit of the proposed dc breaker.

In the equivalent circuit, Z_{RC} is the series combination of R and C and Z_L is the parallel combination of R_L and C_L . Furthermore, L_{m1} and L_{m2} are the primary and secondary magnetizing inductances of the transformer, respectively. From the equivalent circuit, it can be determined that the voltage transfer function is

$$\frac{V_o}{V_s} = \frac{N_1(N_{m2} - N_{m1}) + N_{m1}N_{m2}}{N_1(N_{m2} - N_{m1}) + N_{m1}N_{m2} + N_{m1}N_{m2} - 2N_{m1}N_{m2}} \quad (7)$$

and the impedance as seen from the source is

$$\frac{Z_{in}}{Z_L} = \frac{N_1(N_{m2} - N_{m1}) + N_{m1}N_{m2} + N_{m1}N_{m2} - 2N_{m1}N_{m2}}{N_1(N_{m2} - N_{m1}) + N_{m1}N_{m2} + N_{m1}N_{m2} - 2N_{m1}N_{m2}} + 1 \quad (8)$$

Where

$$N_{m1} = \sqrt{L_{m1}L_{m2}} \quad (9)$$

Fig. 5 shows the voltage transfer function according to (7) for the proposed breaker with parameters in Table I. In this example, $R_L = 50 \Omega$ and $C_L = 0$. At low frequencies, it has unity gain. There is a resonance around 800 Hz and the breaker attenuates signals of higher frequency. The transfer function is

similar to that of a notch filter with attenuation at high frequencies. It is instructive to look at the proposed circuit in terms of its Thevenin equivalent. With the device open-circuited, the Thevenin voltage can be seen to be v_s . Based on mathematical circuit analysis, the Thevenin impedance is seen to be

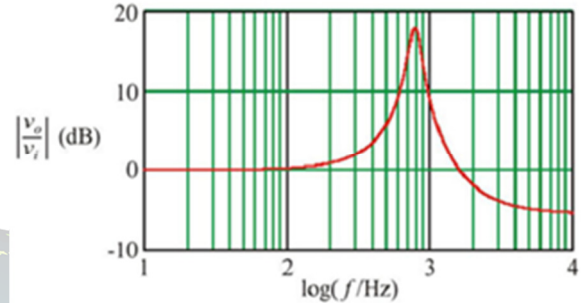


Fig. 5. Voltage transfer function of the proposed breaker.

$$Z_{in} = \frac{N_1(N_{m2} - N_{m1}) + N_{m1}N_{m2}}{N_1(N_{m2} - N_{m1}) + N_{m1}N_{m2} + N_{m1}N_{m2} - 2N_{m1}N_{m2}} \quad (10)$$

Using the parameters from before, the plot of Thevenin impedance is shown in Fig. 6. At low frequencies, this is seen as inductive and has the value L_{m1} . This is seen from (10) and that Z_{RC} is an open-circuit at low frequencies. At high frequencies, the Thevenin impedance becomes a negative resistor. Thus, considering the Thevenin equivalent, applying a transient or high-frequency fault results in current flow back to the source which causes the source (or SCR) current to go to zero.

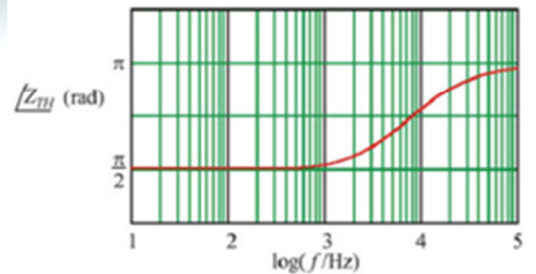
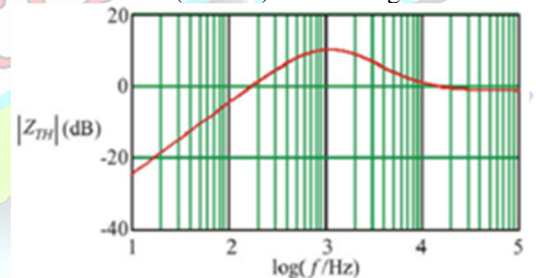


Fig. 6. Thevenin impedance of the proposed breaker.

A number of researchers have produced variations of the z-source breaker. Herein, these are

denoted as the classic z source breaker the series z-source breaker the modified series z-source breaker [20], [25], and the new series breaker [23]. For clarity, these are depicted in Fig. 7. A comparison the various dc breaker topologies is shown in Table II. The “+” symbol in a column indicates where that circuit has an advantage, the “-” indicates a disadvantage, and the “0” represents a neutral comparison. As can be seen, the classic z-source breaker had a number of limitations. A common ground between the source and load was established with the series design but then the source current would ring after the SCR switched OFF. This is an inconvenience since the source current can ring up to a large value and inductance must be increased to limit this ringing. The modified series design also addressed the common ground and further has the

Table II
Comparison To Z-Source Breaker Variants

	Classic	Series	Modified series	New series	Proposed
Common source/load ground	-	+	+	+	+
Low-pass filter transfer function	-	-	+	+	0
Invariant to load steps	-	-	-	+	+
No ringing in source current	+	-	-	-	+

desirable property that its transfer function has a low-pass form. Up to this point, all the designs could mistake a step change in load of more than 100% as a fault. The new series design eliminated this by providing an additional branch for the fault current. However, the source current ringing was still there. The proposed breaker can be seen to have all of the advantages listed in Table II. Furthermore, the proposed breaker has much fewer components. The only questionable property of the proposed breaker is the voltage transfer function. From Fig. 5, it can be seen that the proposed breaker does attenuate high frequencies, but not at the rate of a traditional low-pass filter.

D. Transient Analysis : An approximate transient analysis in response to a step change in load can be carried out using the circuit of Fig. 4. First, the following approximations are made. The fault is assumed to be an ideal short-circuit at the output. The resistance in the impedance ZRC is assumed to be negligible. The turn's ratio is such that only a negligibly small voltage is induced in the transformer secondary. With these assumptions, the capacitor current is found to be

$$i_c \approx i_o \sqrt{\frac{L}{C}} \sin(\omega t) \quad (11)$$

where

$$i_o = (i_{o2}^2)^{-\frac{1}{2}} \quad (12)$$

From the circuit in Fig. 4 and (11), one can arrive at

$$i_c = \frac{i_o}{\omega L} \left[1 - \frac{\omega L}{2} \sin(2\omega t) \right] \quad (13)$$

From which it is seen that the source (thus SCR) current is

$$i_s = i_o + \frac{i_o}{\omega L} \sin(\omega t) - i_o \sqrt{\frac{L}{C}} \sin(\omega t) \quad (14)$$

where i_o is the steady-state source current before the fault occurred; as defined above. Much insight into the operation of the proposed circuit can be obtained from the above analysis. First, (11) suggest a sinusoidal pulse in current, which, along with the source current, will flow to the breaker output. Therefore, the fault current will have roughly the shape of (11) and its peak value and pulse duration can be predicted. it can be determined exactly when the source current will reach zero; thus, a prediction of how fast the breaker can switch OFF can be made.

E. Detailed Simulation: Based on the parameters of Table I, a detailed simulation was carried out. In this study, the source voltage is 100 V and the load is purely resistive. Fig. 7 shows the source and load currents when the load is stepped from 50 to 16.7 Ω . The variables are the same as those labeled in Fig. 2. As can be seen, the load current steps from 2 to 6 A. This causes a step in capacitor current which reflects back to the source current causing it to dip, but not quite to zero. In fact, applying the criteria (6) with $i_o = 2$ A and the turns ratio given in Table I, states that a change of output current by $\Delta i_o > 5.83$ A would cause the breaker to switch OFF. This says that the output current can step from 2 up to 7.83 A without switching the breaker off.

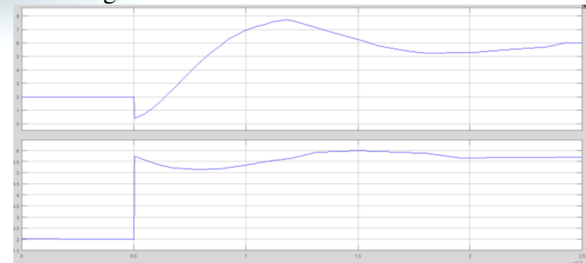


Fig. 7. Breaker response to a step change in load.

Therefore, the SCR stays on and the source current goes to 6 A after the transient. Fig. 8 shows the response of the proposed breaker to a fault. In this

study, the source voltage is 100 V and the load resistance is 16.7Ω . A bolted fault occurs at the output which is represented by a $10\text{-m}\Omega$ resistance. As the output current starts to rise, the current reflected in the transformer causes the source current to directly go to zero in microseconds.

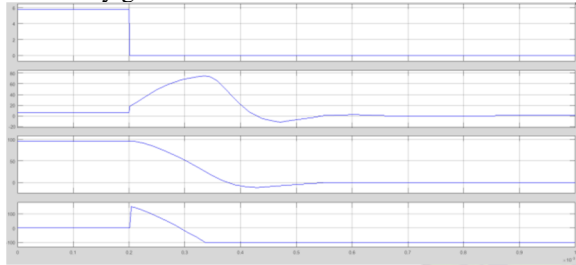


Fig.8.Breaker response to a fault

After the SCR switches OFF, the load current goes up to over 100 A as the capacitor discharges. Incidentally, the approximate analysis of (11) predicts a peak fault current of 99 A. The SCR voltage first goes positive, and it is, thus, reverse biased for about $100 \mu\text{s}$; allowing the SCR to completely turn off. When the SCR voltage goes negative and is equal in magnitude to the source voltage, the diode switches ON stopping the resonance.

In this circuit, the transformer connections are wound around the capacitor (seen in the bottom left) for better volume density. The magnetic field will be unaffected by the capacitor and the effective air-core inductor will not experience saturation during transients. The SCR is seen at the right and the resistor is seen at the bottom of the board. The top half of the board contains voltage and current transducers which are used only for obtaining waveforms.

V. PRACTICAL CONSIDERATIONS

In this section, a medium-voltage design will be carried out to show how the proposed breaker may practically fit into a power system, such as an electric ship. Topology modifications, effect

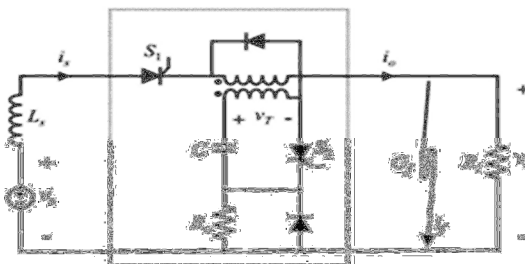


Fig. 9. Power system with modified dc switch. of transformer leakage inductance, effect of source impedance, and rate of fault inception will be considered.

A. Topology Modifications : according to the Fig. 9 which show the proposed dc breaker inserted into a medium voltage dc (MVDC) system. Two modifications to the breaker have been made. First, the RC impedance in the previous design has been replaced with a pure capacitance. In addition, a charging resistor R_c with an accompanying diode has been placed in series. The purpose of the charging resistor is to initially charge the capacitor. That is, when starting (or reenergizing) the breaker, the source voltage is established then the SCR, labeled S1, is gated on.

The next modification to the breaker is a switch-OFF SCR, labeled S2. This adds an important feature to the breaker in that it allows the circuit to be used as a dc switch. During steady-state operation, with the capacitor charged, gating on S2 discharges the capacitor into the secondary winding causing the breaker to switch OFF. Therefore, the breaker can be purposely switched OFF by gating S2. Then, switched ON again by gating S1.

B. Medium-Voltage Design: The MVDC system has a source voltage of $v_s = 1000\text{V}$ and a power level of 100 kW ($R_l = 10 \Omega$). The source has an inductance of $L_s = 10 \mu\text{H}$. The design of the breaker was carried out by selecting a number of turns, turns ratio, and wire diameter that supports full current (in this case, the wire cross sectional area is 0.42 cm^2). In this case, a leakage inductance of 10% is assumed. The transformer is made as an air core with a

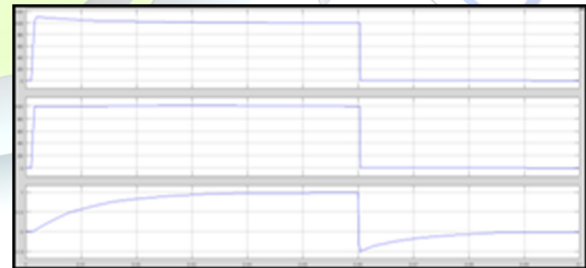


Fig. 10. Simulation demonstrating switch-OFF capability.

solenoid structure with a radius of about 10 cm which has a mass of 13 kg and a volume of 16 L. Table III shows the transformer parameters. The breaker capacitance is set to $100 \mu\text{F}$ and the charging resistance is set to 100Ω . This seems quite reasonable since the capacitor charging current will have a peak value of 10 A (based on $v_s = 1000 \text{ V}$



and $R_c = 100 \Omega$). Furthermore, the charging time constant will be (based on $C = 100 \mu\text{F}$ and $R_c = 100 \Omega$). The SCR is a fast turn-off type with a total turn off time of $t_q = 25 \mu\text{s}$.

According to Fig. 10 which shows simulation results of the proposed breaker demonstrating closing and opening ability. First, S1 is fired and the capacitor is charged through R_c . Since the time constant here is 10 ms, the capacitor can be seen to be fully charged at 50 ms. At this point, the breaker is supporting a 100-kW load. At 60 ms, S2 is gated causing the capacitor to discharge in the transformer secondary and causing the proposed circuit to switch OFF. Thus, this added SCR can be used to purposely switch OFF the load. Fig. 11 shows results of a simulation where the breaker switches OFF in response to a fault.

Initially, the breaker is supporting a 30-kW load when the load is suddenly increased to 100 kW. As can be seen, the source and output current step to rated load and the breaker does not switch OFF. This could be predicted using the turns ratio. Also note that the voltage across the transformer v_T spikes to about 500 V.

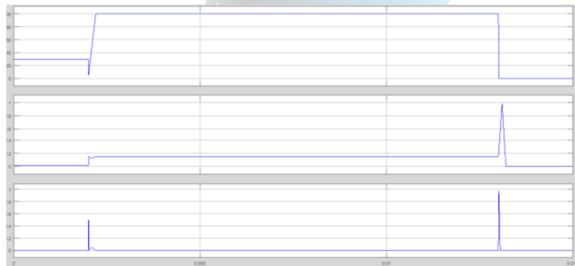


Fig. 11. Simulation demonstrating fault handling.

A measurement of this voltage could be used to differentiate between a step change in load and a fault. The fault is applied at the end of the simulation and the output current surges, causing the breaker to switch OFF and the source current simply goes to zero. Note that the transformer voltage v_T spikes to about 1 kV when the fault is applied. Thus, the voltage v_T may be of some use in indicating faults.

C. Effect of Grid Impedance and Leakage Inductance :In traditional breaker circuits, there is a limit to the amount of grid impedance that can exist for the breaker to work which is sometimes expressed as the L/R ratio of source inductance to fault resistance. The source inductance was illustrated in Fig. 9, and can be included in the transient analysis. First, using (13), it is seen that the source current is a minimum when

$$I_{s, \min} = \sqrt{\frac{L_{l1}}{L_{l2}}} I_{s1}^{-1} \left(\frac{I_{s2}^2}{I_{s1}} \right) \quad (15)$$

Now, by including the source inductance, (14) becomes

$$I_{s0} + \left(\frac{I_{s1}}{I_{s1} + I_{s2}} \right) I_{s1} - \left(\frac{I_{s2}}{I_{s1} + I_{s2}} \right) \sqrt{\frac{L_{l1}}{L_{l2}}} I_{s1}^{-1} (I_{s0} I_{s2}) \quad (16)$$

Substituting (15) into (16) and requiring that the source current go to zero in order for the SCR to switch OFF, the source inductance is

$$L_{s, \min} = \frac{I_{s1}}{I_{s0}} \left[\sqrt{\frac{L_{l1}}{L_{l2}}} I_{s1} (I_{s0} I_{s2}) - I_{s1} I_{s2} \right] - I_{s1} \quad (17)$$

Essentially, the breaker will not switch OFF if the source inductance is greater than that predicted. In this case, the fault current will continue to be drawn from the source; a phenomenon noted in the literature. For the medium voltage design in Table III, predicts a maximum allowable source inductance of 600 μH . According to detailed simulation, the source inductance can be raised to 700 μH before the breaker fails; the slight difference owed to the approximation in. Considering the circuit of Fig. 9 and the equivalent circuit of Fig. 4, it can be seen that including leakage inductance in the primary winding has the same effect as adding source inductance. Also, note that the calculation of $L_{s, \max}$ for this design is much less than the leakage inductances shown in Table III.

Table III
Parameters Of The MVDC Breaker Design

$N_1 = 40$	$r_1 = 10.3 \text{ m}\Omega$	$L_{l1} = 69 \mu\text{H}$	$L_{m1} = 625 \mu\text{H}$
$N_2 = 14$	$r_2 = 3.62 \text{ m}\Omega$	$L_{l2} = 85 \mu\text{H}$	$L_{m2} = 77 \mu\text{H}$
$R_c = 100 \Omega$	$C = 100 \mu\text{F}$		
$V_{RRM} = 1200 \text{ V}$	$I_{TRMS} = 275 \text{ A}$	$t_q = 25 \mu\text{s}$	

Furthermore, a relatively large value of 10% leakage inductance was used in this design. Considering these facts, the effect of leakage inductance on the breaker operation is negligible compared to the effect of source inductance.

C. Fault Inception :The proposed circuit, along with the z-source breaker, rely on fast fault inception [18]. Consider the medium-voltage design in Table III operating from an ideal source. Using detailed simulation, it was determined that if the fault conductance is ramped from 0 to 100 S in a time greater than 17.2 ms, the breaker fails to isolate the fault. That is, in this case, the breaker will not automatically respond to a fault that ramps its conduction slower than 5814 S/s.



In this case, what is recommended is monitoring the output current and comparing it to a threshold. When the threshold is reached, S2 can be fired so that the fault is cleared. Using this method, the proposed circuit operates much like a traditional solid-state circuit breaker. Therefore, the proposed breaker will always operate in a similar way to other breakers, but will have the added capability of automatically and quickly responding to faults with rapid inception.

CONCLUSION

In this paper we are implementing a DC switch which is utilized for the variation in the solid-state breaker with the addition feature such as automatically switch OFF in response to faults. Therefore according to the turn's ratio in the circuit's transformer which allow the determine the amount of transient current which is used to identify the fault and also to opposed the proposed change in load. By using the matlab simulation we can analysis the proposed breaker which is used to response to the step change in the load and to fault. There the circuit breaker will be place between the source and load through the common ground and it will invariant to step change in load and it will not produce the resonance in the current.

REFERENCES

- [1] R. Cuzner, D. MacFarlin, D. Clinger, M. Rumney, and G. Castles, "Circuit breaker protection considerations in power converter fed dc systems," in Proc. IEEE Electr. Ship Technol. Symp., Apr. 2009, pp. 360–367.
- [2] B. Bolanowski and F. Wojcik, "A fast dc hybrid circuit breaker," presented at the IEEE Colloq. Electronic-Aided Current-Limiting Circuit Breaker Developments Applications, London, U.K., Nov. 1989.
- [3] A. Pokryvailo and I. Ziv, "A hybrid repetitive opening switch for inductive storage systems and protection of dc circuits," in Proc. IEEE Power Modulator Symp. High-Voltage Workshop, 2002, pp. 612–615.
- [4] C. Meyer, M. Kowal, and R. W. De Doncker, "Circuit breaker concepts for future high-power dc-applications," in Proc. IEEE Ind. Appl. Soc. Conf., 2005, vol. 2, pp. 860–866. 1418 IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 32, NO. 2, FEBRUARY 2017
- [5] A. Shukla and G. D. Demetriades, "A survey on hybrid circuit-breaker topologies," IEEE Trans. Power Del., vol. 30, no. 2, pp. 627–641, Apr. 2015.

[6] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage dc microgrids," IEEE Trans. Power Del., vol. 24, no. 3, pp. 1045–1053, Jul. 2009.

[7] J. Candelaria and J. D. Park, "VSC-HVDC system protection: A review of current methods," in Proc. IEEE Power Energy Soc. Power Syst. Conf., Mar. 2011, pp. 1–7. [8] P. Nuutinen, P. Peltoniemi, and P. Silventoinen, "Short-circuit protection in a converter-fed low-voltage distribution network," IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1587–1597, Apr. 2013.

[9] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability," IEEE Trans. Power Electron., vol. 30, no. 1, pp. 108–123, Jan. 2015.



PUTTAPATI PRAVEEN KUMAR

Completed B.Tech in Electrical & Electronics Engineering in 2014 from JNTUH, Hyderabad and Pursuing M.Tech from GITAM (DEEMED TO BE UNIVERSITY) Hyderabad, Telangana India. Area of interest includes Electrical Power Systems.

E-mail id: praveenreddy498@gmail.com



MRS.VENKATA PADMAVATHI,S,

Completed B.Tech in Electrical & Electronics Engineering from JNTUH, Hyderabad and M.E in Power System from Anna University Chennai. Working as Assistant Professor at GITAM (DEEMED TO BE UNIVERSITY), Hyderabad Telangana India. Area of interest includes Electrical Power System and FACTS.



ISSN 2394-3777 (Print)

ISSN 2394-3785

(Online)

Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 5, Special Issue 5, March 2018

E-mail id: sv.padmavathi@gmail.com



DR.P.VASUDEVA NAIDU, PH.D

Completed B.Tech in Electrical & Electronics Engineering from Bapatla Engineering College Guntur and Ph.D from Acharya Nagarjuna University, Guntur. Working as Head of EEE Department at GITAM (DEEMED TO BE UNIVERSITY), Hyderabad Telangana India. Area of interest includes Power Quality, Power Electronics and Electrical Power System.

E-mail id: pvdnaidu@gitam.in

